PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC4052P/FP/DP

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION

The M74HC4052 is a semiconductor integrated circuit consisting of two multiplexer/demultiplexers capable of selecting between 4 analog switches with 2-input digital signal.

FEATURES

- Low on-state registance
- High off-state resistance: more than $10^9\Omega$, typ.
- Excellent conductance linearity
- Enable input
- High-speed: 28ns typ. (C_L = 50pF, V_{CC} = 4.5V, V_{EE} = GND)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, V_{EE}=GND, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Wide operating voltage range: $V_{CC}-V_{EE}$=2~12V
  V_{CC}−GND=2~12V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

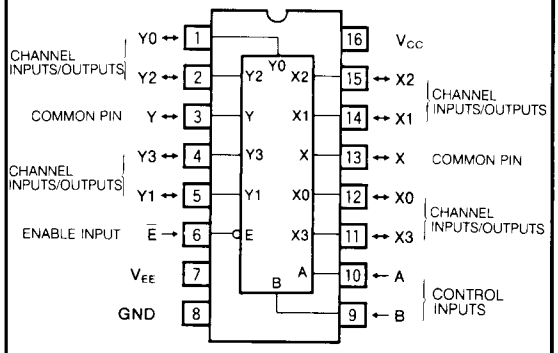
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC4052 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the LSTTL.

When a two-bit binary code is applied at control inputs A and B, the impedance between common pin X and the selected channel X0 through X3 will become low, and the other channels will become high-impedance state. The impedance between common pin Y and channels Y0 through Y3 is controlled in the same way. In this case, when enable input $\overline{E}$ is high, all channels X0 through X3 and Y0 through Y3 will become high-impedance state, irrespective of other inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N
16P2P

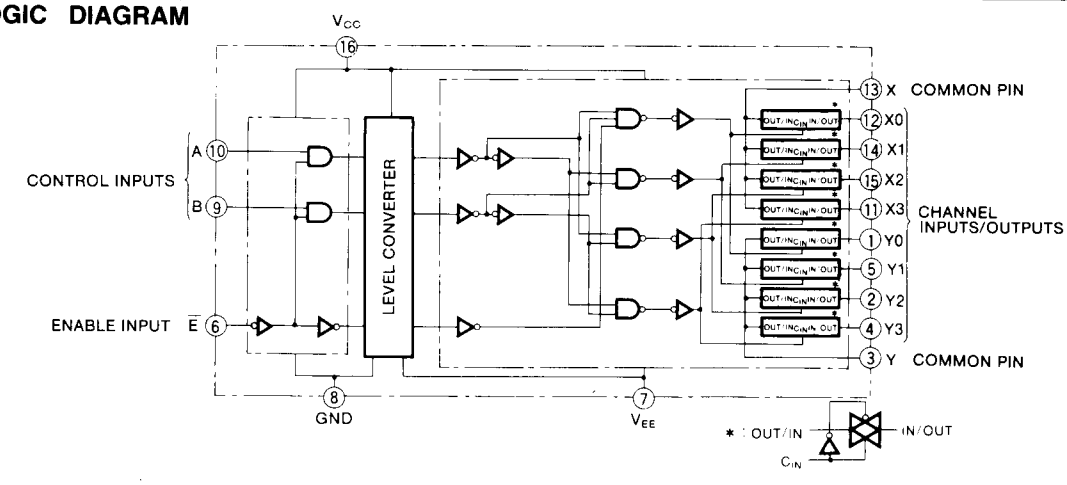
Analog signals of amplitude $V_{CC}-V_{EE}$ greater than logic amplitude V_{CC}−GND at A and B can be switched.

FUNCTION TABLE (Note 1)

Enable input	Control inputs		Switch between channel input/output and common pin			
$\overline{E}$	B	A	X0, Y0	X1, Y1	X2, Y2	X3, Y3
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

Note 1 : X : Irrelevant
ON : Impedance between Xn and X, and between Yn and Y is low. (n : 0~3)
OFF : Impedance between Xn and X, and btween Yn and Y is high. (n : 0~3)

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_{EE}			−7.0∼+0.5	V
V_I	Input voltage	Control inputs, enable inputs	−0.5∼V_{CC}+0.5	V
		I/O channels, common pins	V_{EE}−0.5∼V_{CC}+0.5	
$V_{I/O}$	Input to output voltage		±0.5	V
V_O	Output voltage		V_{EE}−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_O	Output current per gate		±25	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±50	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature		−65∼+150	℃

Note 2 : M74HC4052FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −6mW/℃.
M74HC4052DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2.0		6.0	V
V_{EE}			0		−6.0	V
V_I	Input voltage	Control input, enable input	0		V_{CC}	V
		Channel input/output, common pin	V_{EE}		V_{CC}	
V_O	Output voltage		V_{EE}		V_{CC}	V
T_{opr}	Ambient operating temperature		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits					Unit
					25℃			−40∼+85℃		
			V_{EE}(V)	V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	Refer to R_{ON} specification	—	2.0	1.5			1.5		V
			—	4.5	3.15			3.15		
			—	6.0	4.2			4.2		
V_{IL}	Low-level input voltage	Refer to R_{ON} specification	—	2.0			0.5		0.5	V
			—	4.5			1.35		1.35	
			—	6.0			1.8		1.8	
R_{ON}	On-state resistance	V_I = V_{IH} V_{IL}, I_S = 0.1mA V_{IS} = GND∼V_{CC} (Test circuit 1)	GND	4.5			170		215	Ω
			−4.5	4.5			85		106	
			−6.0	6.0			50		63	
		V_I = V_{IH} V_{IL}, I_S = 0.1mA V_{IS} = GND, V_{CC} (Test circuit 1)	GND	2.0						Ω
			GND	4.5			85		106	
			−4.5	4.5			63		78	
			−6.0	6.0			37		47	
ΔR_{ON}	On-state resistance variation (switch-to-switch in the same package)	V_I = V_{IH}, V_{IL} V_{IS} = GND∼V_{CC}	GND	4.5						Ω
			−4.5	4.5						
			−6.0	6.0						
$I_{IZ(OFF)}$	Switch-off leakage current	V_I = V_{IH}, V_{IL}, V_{IS} = GND, V_{CC} V_{OS} = V_{CC}, GND	GND	6.0			±0.1		±1.0	μA
			−6.0	6.0			±0.2		±2.0	
$I_{IZ(ON)}$	Switch-on leakage current	V_I = V_{IH}, V_{IL}, V_{IS} = GND, V_{CC}	GND	6.0			±0.2		±2.0	μA
			−6.0	6.0			±0.4		±4.0	
I_{IH}	High-level input current	V_I = 6V	—	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V	—	6.0			−0.1		−1.0	μA
I_{CC}	Quiescent power dissipation	V_I = V_{CC}, GND, I_O = 0μA	GND	6.0			4.0		40.0	μA
			−6.0	6.0			8.0		80.0	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

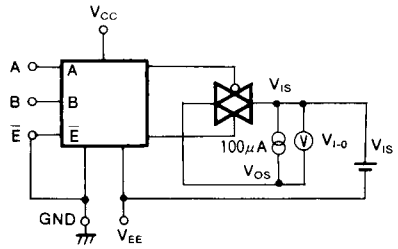
Symbol	Parameter	Test conditions	V_{EE}(V)	V_{CC}(V)	Limits 25℃ Min	Limits 25℃ Typ	Limits 25℃ Max	Limits −40~+85℃ Min	Limits −40~+85℃ Max	Unit
f_{max}	Maximum propagation frequency R_L = 1kΩ, V_{IS} = 1.6VRMS	C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (X0~X3−X, X−X0~X3 Y0~Y3−Y, Y−Y0~Y3)	R_L = 1kΩ C_L = 50pF (Test circuit 3)	GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			60		75	ns
			GND	4.5			12		15	
			−4.5	4.5						
			−6.0	6.0						
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A, B − X, Y)	R_L = 1kΩ C_L = 50pF (Test circuit 8)	GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PHL}			GND	2.0			370		465	ns
			GND	4.5			74		93	
			−4.5	4.5						
			−6.0	6.0						
t_{PLZ}	Low-level and high-level output disable time (A, B−X0~X3,Y0~Y3 $\bar{E}$−X, X0~X3, Y, Y0~Y3)	R_L = 1kΩ C_L = 50pF (Test circuit 4)	GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PHZ}			GND	2.0			290		365	ns
			GND	4.5			58		73	
			−4.5	4.5						
			−6.0	6.0						
t_{PZL}	Low-level and high-level output enable time (A, B−X0~X3, Y0~Y3 $\bar{E}$−X, X0~X3, Y, Y0~Y3)		GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
t_{PZH}			GND	2.0			345		435	ns
			GND	4.5			69		87	
			−4.5	4.5						
			−6.0	6.0						
	Sine wave propagation distortion	V_{IS} = 1.6VRMS R_L = 10kΩ (Test circuit 5)	−4.5	4.5						%
	Feedthrough (switch off)	V_{IS} = 1.6VRMS R_L = 10kΩ C_L = 50pF (Test circuit 2)	−4.5	4.5						MHz
	Crosstalk (control input, enable input-to-switch outputs)	R_L = 10kΩ R_I = 1kΩ C_L = 50pF (Test circuit 6)	−4.5	4.5						mV_{P-P}
	Crosstalk (switch-to-switch)	R_L = 1kΩ, C_L = 50pF (Test circuit 7)	−4.5	4.5						MHz
C_I	Input capacitance — Control input						10		10	pF
	Input capacitance — Channel input/output									
	Input capacitance — Common pin									
C_I	Feedthrough capacitance									pF
C_{PD}	Power dissipation capacitance (Note 2)									pF

Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions.
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

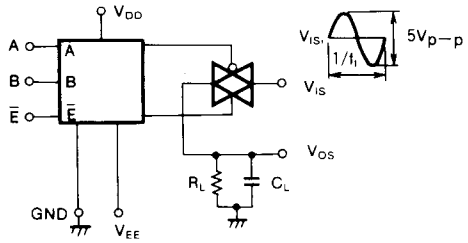
Test Circuit

1. On-state resistance

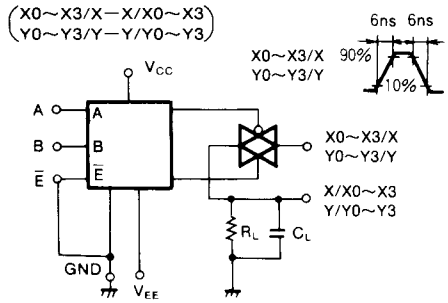


$$R_{ON} = \frac{V_{I-O}}{10^{-4}} (\Omega)$$

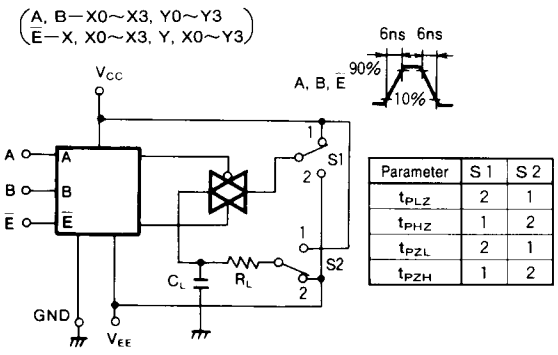
2. Maximum propagation frequency, fieldthrough (switch off)



3. Low-level to high-level and high-level to low-level propagation time

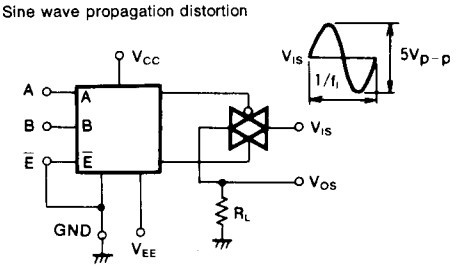


4. Low-level to high-level and high-level to low-level output propagation time, output enable, disable time

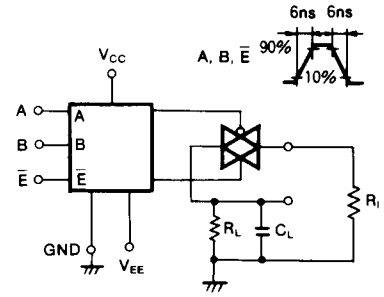


Parameter	S1	S2
t_{PLZ}	2	1
t_{PHZ}	1	2
t_{PZL}	2	1
t_{PZH}	1	2

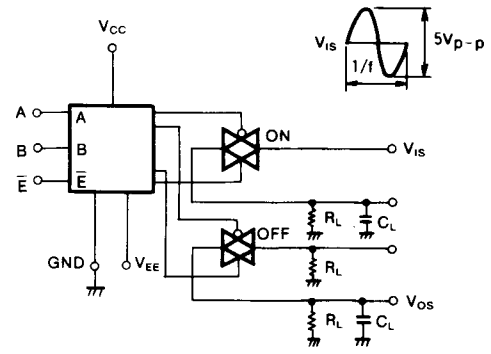
5. Sine wave propagation distortion



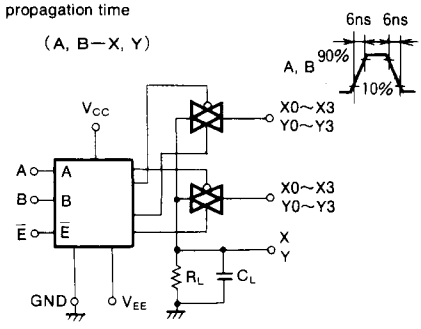
6. Crosstalk (control input, enable input)



7. Crosstalk (switch-to-switch)



8. Low-level to high-level and high-level to low-level propagation time



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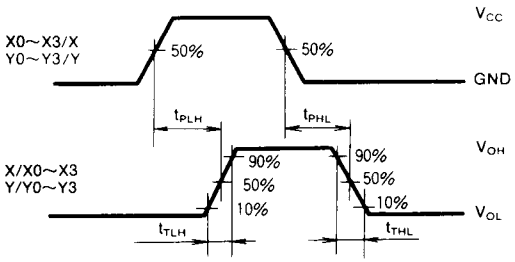
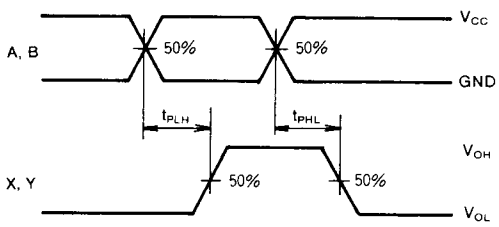
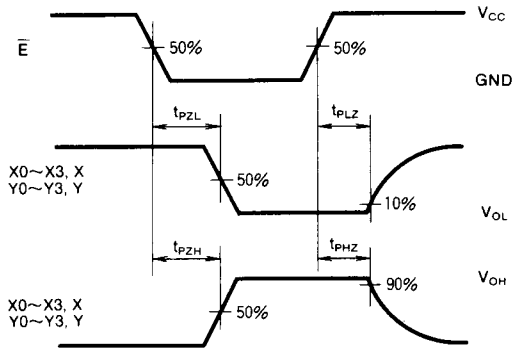
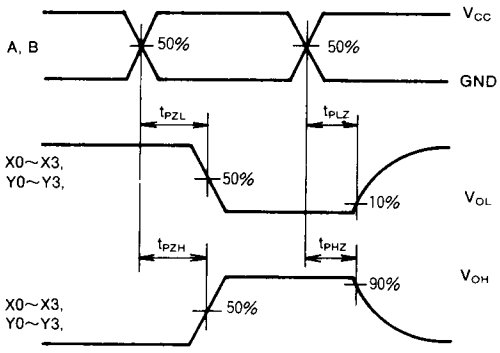
TIMING DIAGRAM







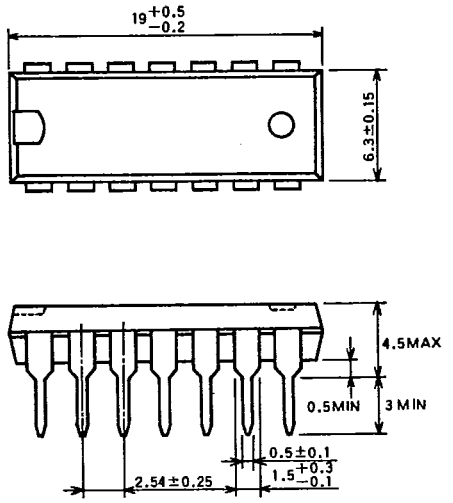


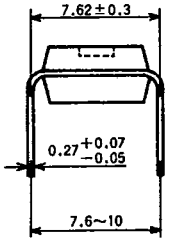
MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

TYPE 14P4 14-PIN MOLDED PLASTIC DIP

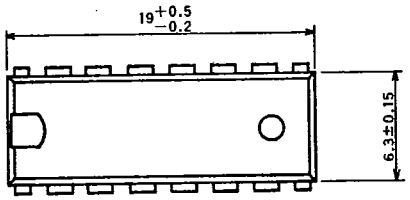
Dimension in mm

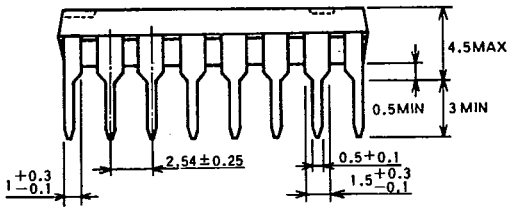


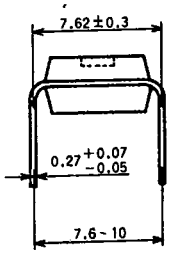


TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm





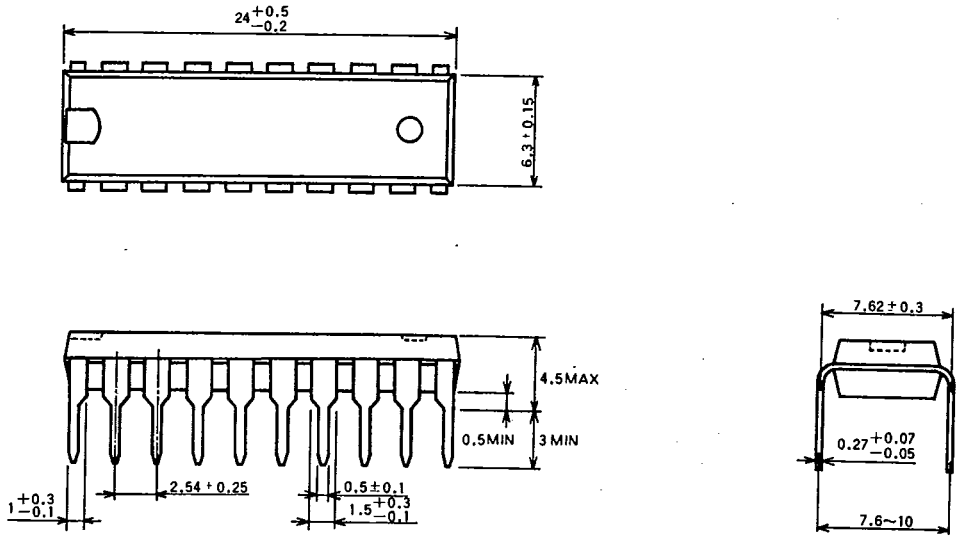


MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

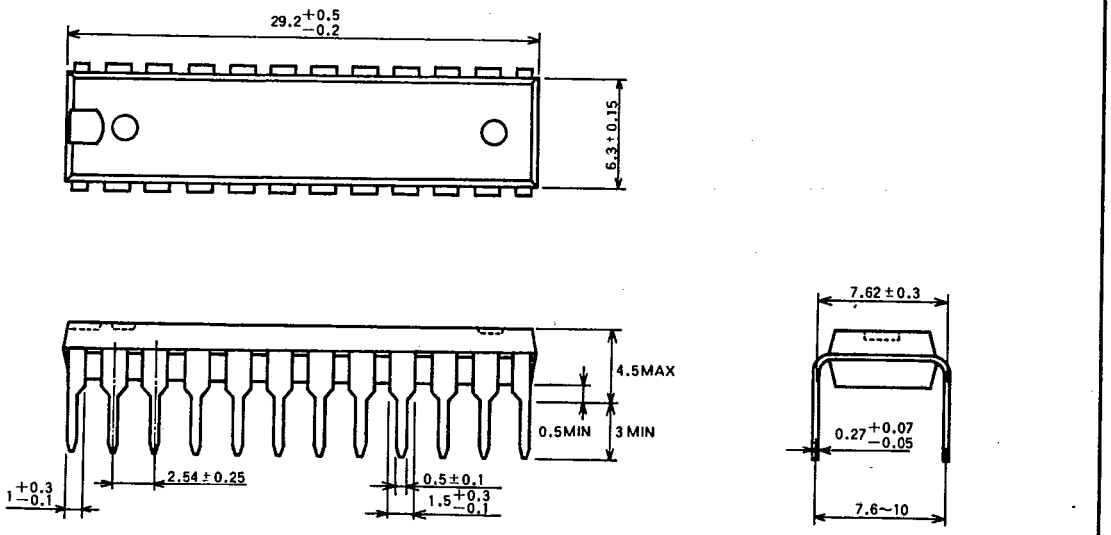
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



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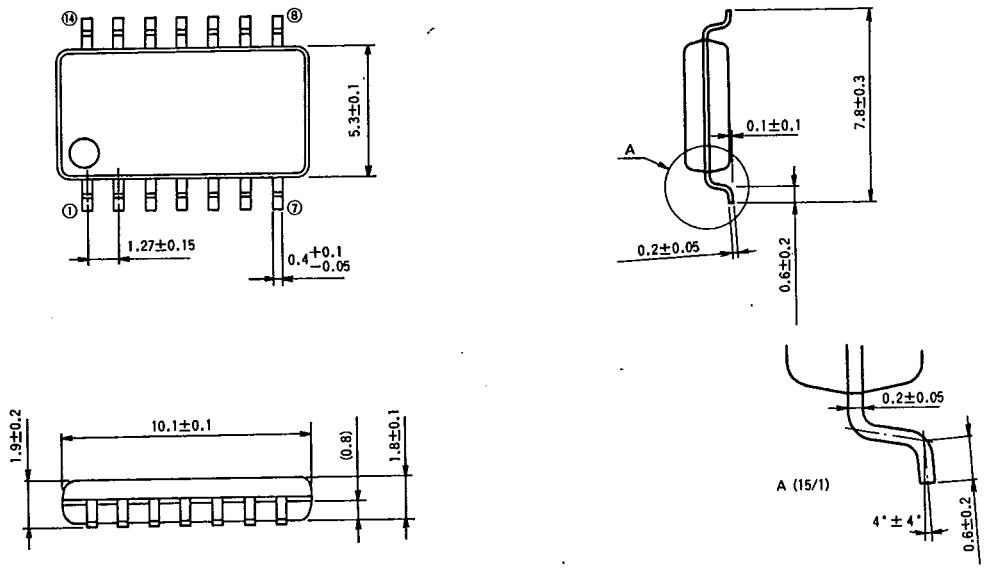
PACKAGE OUTLINES

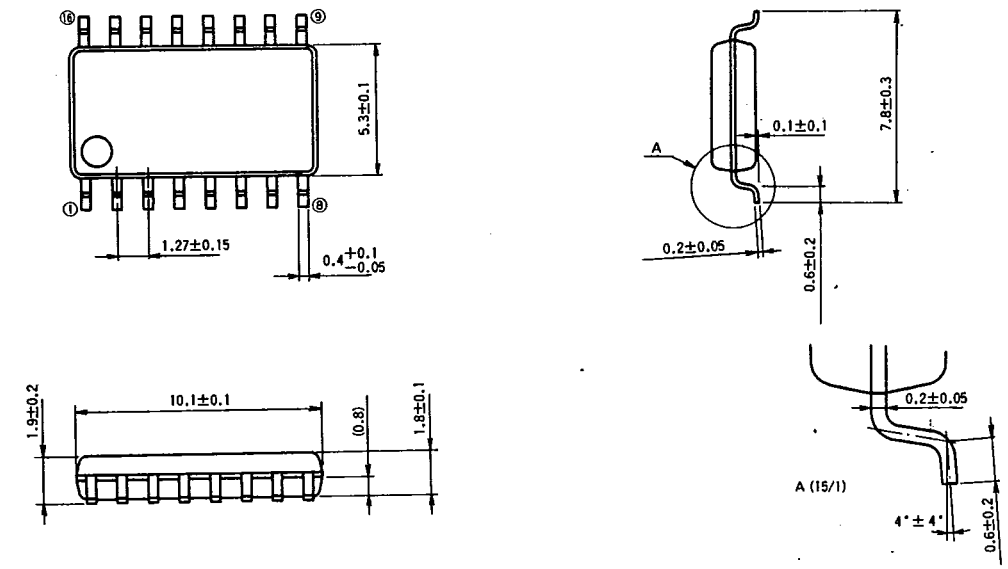
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

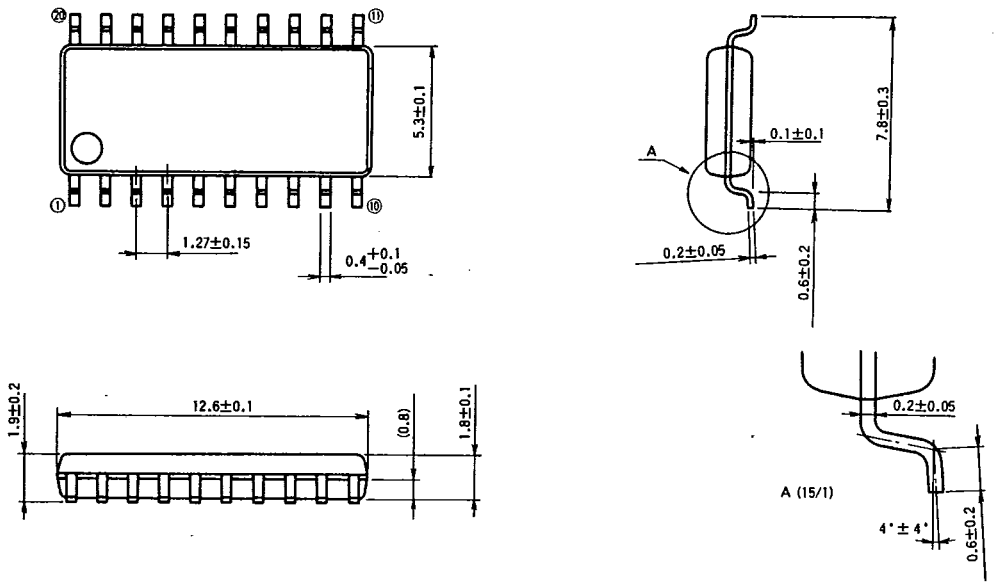
Dimension in mm



PACKAGE OUTLINES

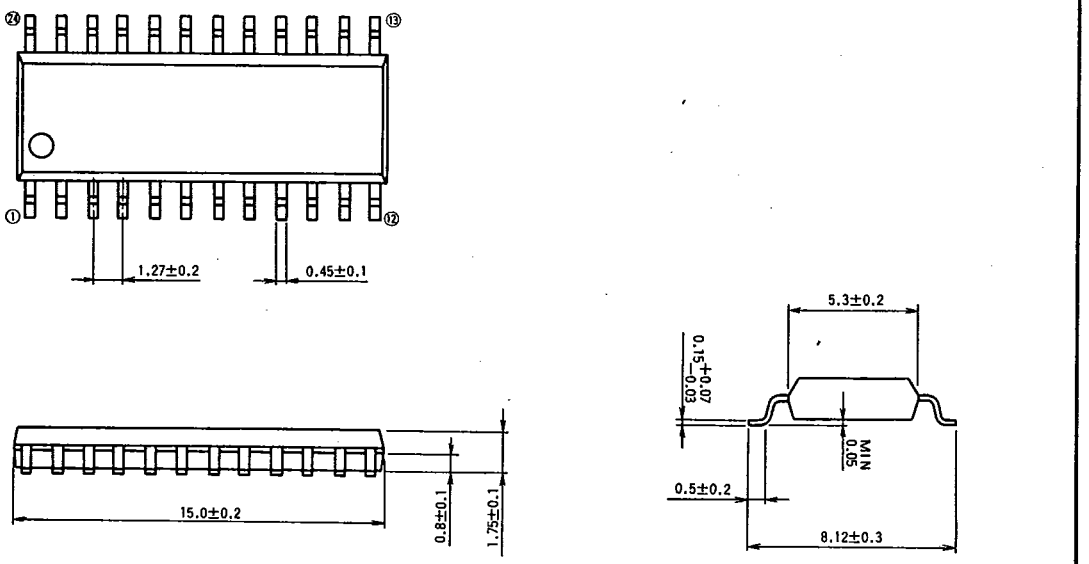
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm

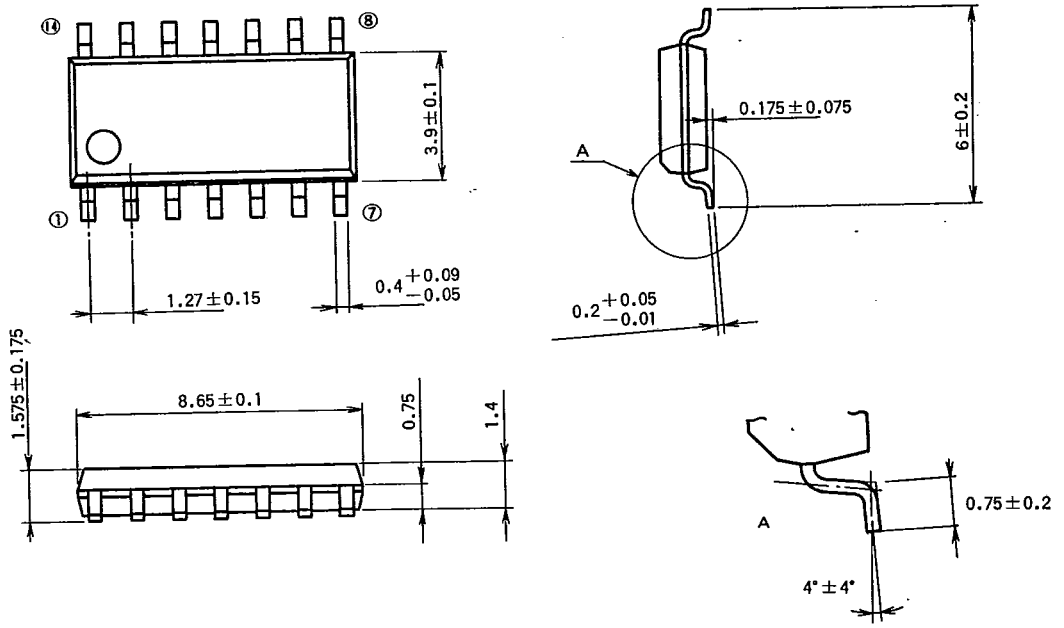


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

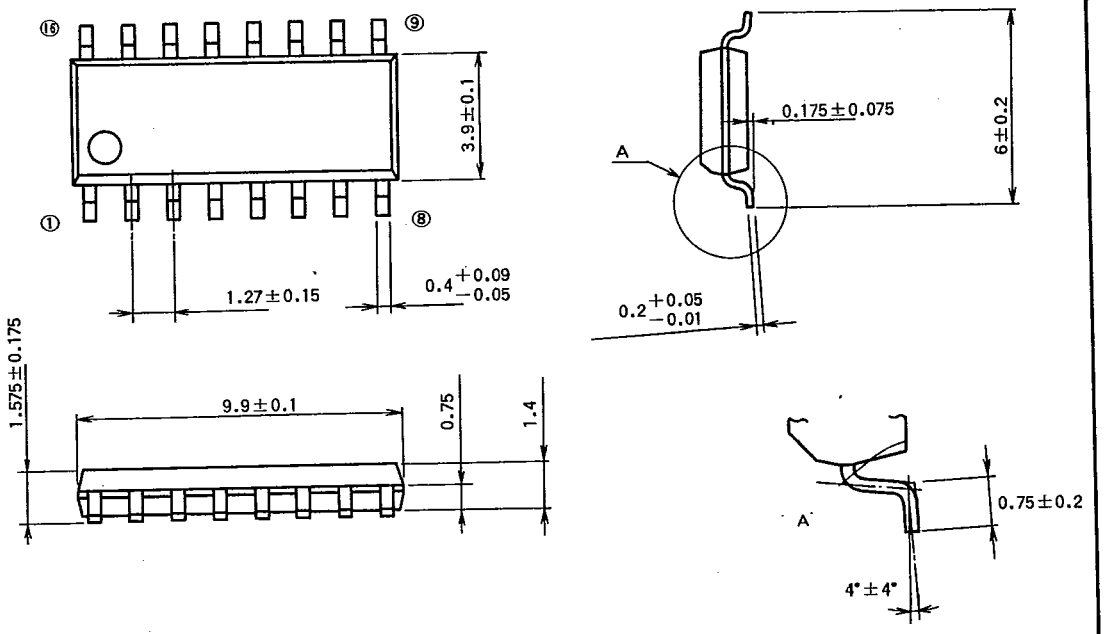
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm