54F/74F574

Octal D-Type Flip-Flop With 3-State Outputs

Description

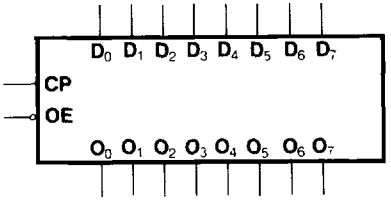
The 'F574 is a high-speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'F374 except for the pinouts.

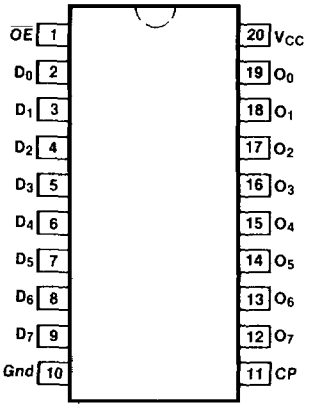
- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'F374**
- **3-State Outputs for Bus Oriented Applications**

Ordering Code: See Section 5

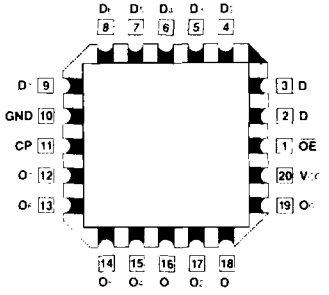
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active LOW)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Outputs	75/15 (12.5)

Functional Description

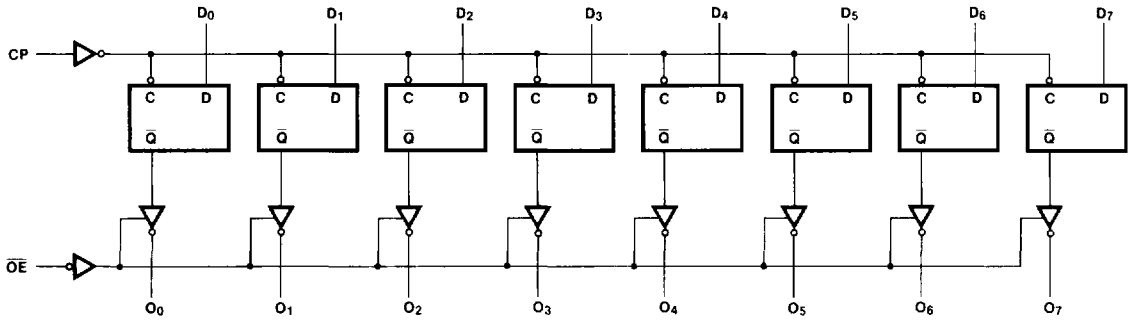
The 'F574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↑	L	L	Z	Load
H	↑	H	H	Z	Load
L	↑	L	L	L	Data Available
L	↑	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current (Outputs OFF)		55	86	mA	V_{CC} = Max, $\overline{OE}$ = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		7.5 9.5						ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time		11.5 7.5						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time		7.0 5.5							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Set-up Time, HIGH or LOW D_n to CP	2.0 2.0							ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to CP	2.0 2.0								
t_w(H) t_w(L)	CP Pulse Width HIGH or LOW	5.0 5.0							ns	3-7