

Am2920

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

Am2920

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops

GENERAL DESCRIPTION

The Am2920 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

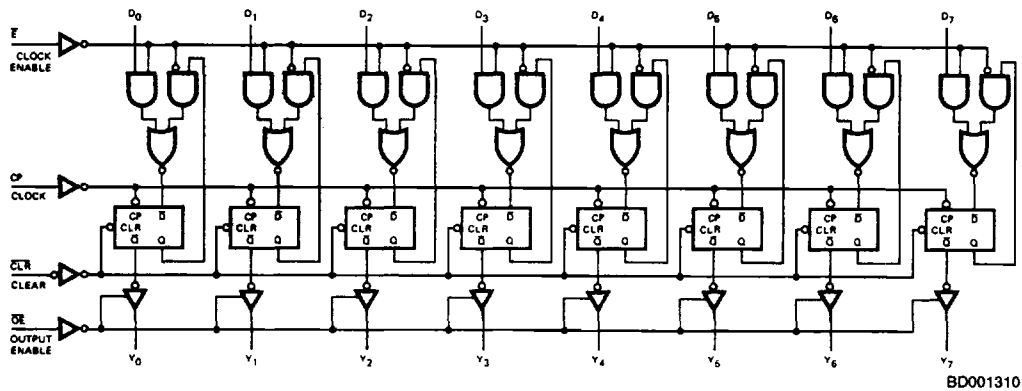
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable (\overline{OE}) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable (\overline{OE}) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input (\overline{E}) is used to selectively load data into the register. When the \overline{E} input is HIGH, the register will retain its current data. When the \overline{E} is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

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BLOCK DIAGRAM

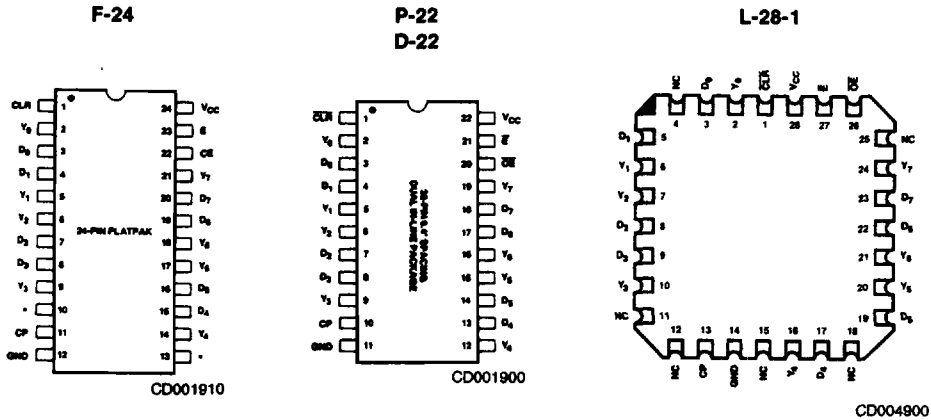


RELATED PRODUCTS

Part No.	Description
Am25LS2520	Octal D-type Flip-Flop
Am2918	Quad D-Registers
Am2954/55	Octal D-Registers
Am29821-26	8, 9, 10-Bit Registers

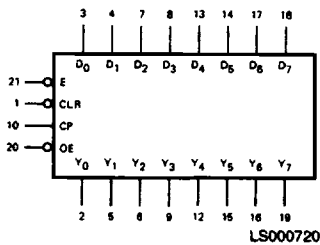
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**CONNECTION DIAGRAM
Top View**

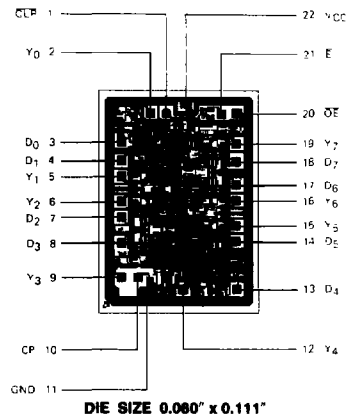


Note: Pin 1 is marked for orientation
*RESERVED — do not use.

LOGIC SYMBOL

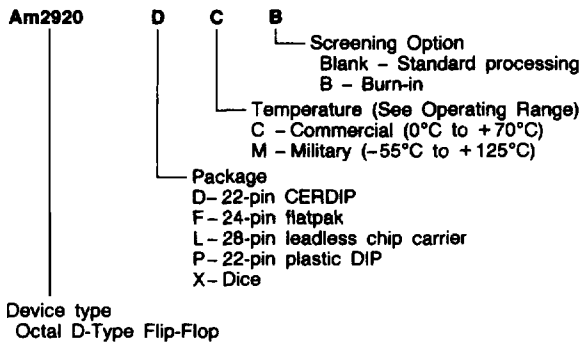


METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am2920	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
1	CLR	I	When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.
10	CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
	Y_i	O	The register three-state outputs.
21	E	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.
20	\overline{OE}	I	Output Control. When the \overline{OE} input is HIGH, the Y_i outputs are in the high impedance state. When the \overline{OE} input is LOW, the TRUE register data is present at the Y_i outputs.

**GUARANTEED LOADING RULES
OVER OPERATING RANGE (In Unit Loads)**

A Low-Power Schottky TT2 Unit Load is defined as 20 μ A measured at 2.7V HIGH and -0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Am2920			
		Input Load	Output HIGH MIL	Output LOW COM'L MIL	Output LOW COM'L MIL
1	CLR	1	-	-	-
2	Y_0	-	50	130	22
3	D_0	1	-	-	-
4	D_1	1	-	-	-
5	Y_1	-	50	130	22
6	Y_2	-	50	130	22
7	D_2	1	-	-	-
8	D_3	1	-	-	-
9	Y_3	-	50	130	22
10	CP	1	-	-	-
11	GND	-	-	-	-
12	Y_4	-	50	130	22
13	D_4	1	-	-	-
14	D_5	1	-	-	-
15	Y_5	-	50	130	22
16	Y_6	-	50	130	22
17	D_6	1	-	-	-
18	D_7	1	-	-	-
19	Y_7	-	50	130	22
20	\overline{OE}	1	-	-	-
21	E	1	-	-	-
22	V_{CC}	-	-	-	-

FUNCTION TABLE

Function	Inputs					Internal	Outputs
	\overline{OE}	CLR	E	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	\uparrow	L	Z
	H	H	L	H	\uparrow	H	Z
	L	H	L	L	\uparrow	L	L
	L	H	L	H	\uparrow	H	H

H = HIGH

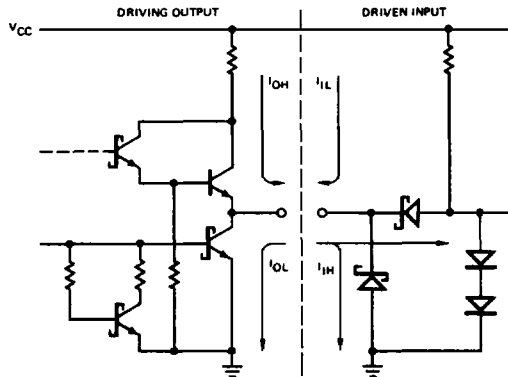
L = LOW

X = Don't Care

NC = No Change

 \uparrow = LOW-to-HIGH transition

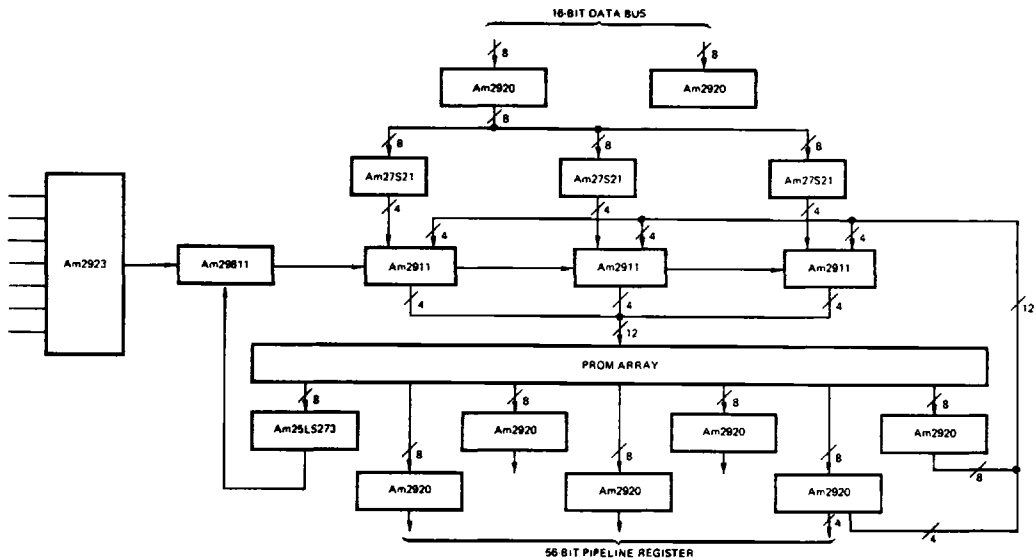
Z = High-Impedance

**LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS**


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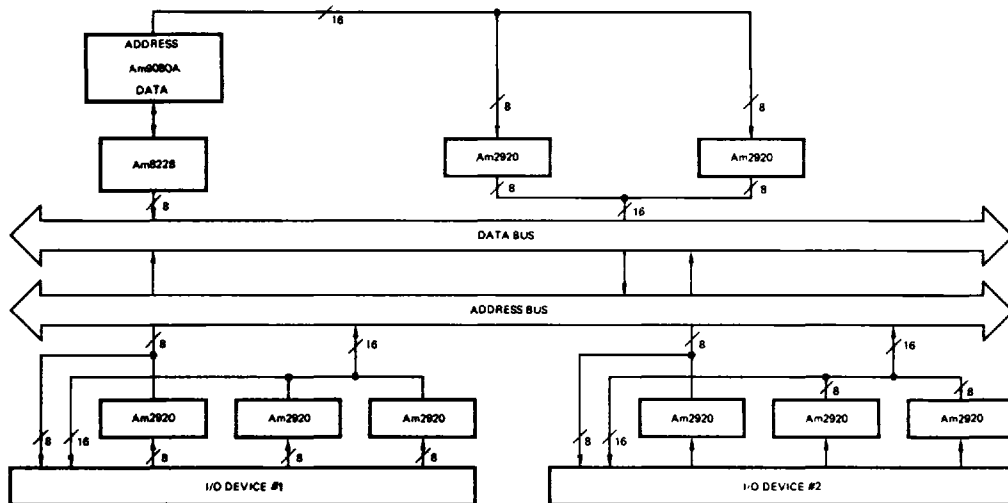
Note: Actual current flow direction shown.

APPLICATIONS



AF001940

A typical Computer Control Unit for a microprogrammed machine.



AF001930

The Am2920 is a useful device in interfacing with the Am9080A system buses.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
(Ambient) Temperature Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential	
Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs For	
High Output State	-0.5V to +V _{CC} max
DC Input Voltage	-0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V

Military (M) Devices

Temperature	-55°C to +125°C
Supply Voltage	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	MIL, I _{OH} = -1.0mA	2.4	3.4		Volts
			COM'L, I _{OH} = -2.6mA	2.4	3.4		
V _{OL}	Output LOW Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0mA			0.4	Volts
			I _{OL} = 8.0mA			0.45	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA				-1.5	Volts
V _{IL}	Input LOW Current	V _{CC} = MAX, V _{IN} = 0.4V				-0.36	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.7V				20	μA
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 7.0V				0.1	mA
I _O	Off-State (High-Impedance) Output Current		V _O = 0.4V			-20	μA
			V _O = 2.4V			20	
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX		-15		-85	mA
I _{CC}	Power Supply Current (Note 4)	V _{CC} = MAX			24	37	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. All outputs open, E = GND, D_i inputs = CLR OE = 4.5V. Apply momentary ground, then 4.5V to clock input.

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units	
t _{PLH}	Clock to Y _i ($\overline{\text{OE}}$ LOW)	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$		18	27	ns	
t _{PHL}				24	36		
t _{PHL}	Clear to Y			22	35	ns	
t _s	Data (D _i)			10	3	ns	
t _h	Data (D _i)			10	3	ns	
t _s	Enable ($\overline{\text{E}}$)		Active		15	10	ns
			Inactive		20	12	
t _h	Enable ($\overline{\text{E}}$)			0	0	ns	
t _s	Clear Recovery (In-Active) to Clock			11	7	ns	
t _{pw}	Clock		HIGH		20	14	ns
			LOW		25	13	
t _{pw}	Clear			20	13	ns	
t _{ZH}	$\overline{\text{OE}}$ to Y _i		$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		9	13	ns
t _{ZL}					14	21	
t _{HZ}	$\overline{\text{OE}}$ to Y _i			20	30	ns	
t _{LZ}				24	36		
f _{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am2920		MILITARY Am2920		Units	
			Min	Max	Min	Max		
t _{PLH}	Clock to Y _i ($\overline{\text{OE}}$ LOW)	$C_L = 50\text{pF}$ $R_L = 2.0\text{k}\Omega$		33		39	ns	
t _{PHL}				45		54		
t _{PHL}	Clear to Y			43		51	ns	
t _s	Data (D _i)			12		15	ns	
t _h	Data (D _i)			12		15	ns	
t _s	Enable ($\overline{\text{E}}$)		Active		17		20	ns
			Inactive		20		23	
t _h	Enable ($\overline{\text{E}}$)			0		0	ns	
t _s	Clear Recovery (In-Active) to Clock			13		15	ns	
t _{pw}	Clock		HIGH		25		30	ns
			LOW		30		35	
t _{pw}	Clear			22		25	ns	
t _{ZH}	$\overline{\text{OE}}$ to Y _i		$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		19		25	ns
t _{ZL}					30		39	
t _{HZ}	$\overline{\text{OE}}$ to Y _i			35		40	ns	
t _{LZ}				39		42		
f _{max}	Maximum Clock Frequency (Note 1)			25		20	MHz	

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.