National Semiconductor

PRELIMINARY

NM93C06LZ/C46LZ/C56LZ/C66LZ 256-/1024-/2048-/4096-Bit Serial EEPROM with Zero Power and Extended Voltage (2V to 6V) (MICROWIRE™ Bus Interface)

General Description

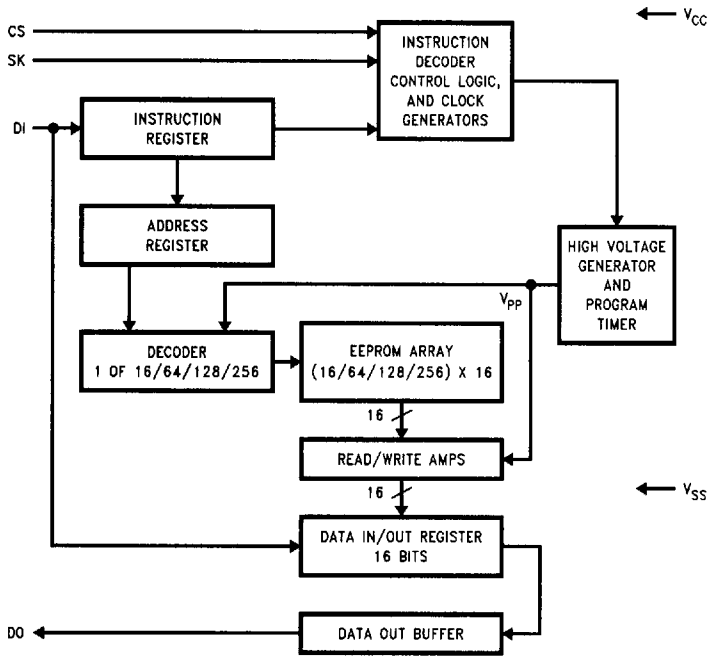
The NM93C06LZ/C46LZ/C56LZ/C66LZ devices are 256/1024/2048/4096 bits respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- **2.0V to 6.0V operation in all modes**
- **Less than 1.0 μA standby current**
- Typical active current of 400 μA
- Direct write: no erase before program
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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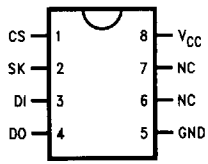
Connection Diagrams

Dual-in-Line Package (N) and 8-Pin SO (M8)



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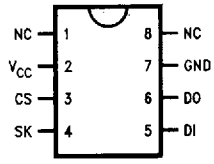
Top View

See NS Package Number N08E and M08A

Alternate SO Pinout (TM8)



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NS Package Number M08A

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM93C06LZN/NM93C46LZN/NM93C56LZN/NM93C66LZN
NM93C06LZM8/NM93C46LZM8/NM93C56LZM8/NM93C66LZM8
NM93C06LZTM8/NM93C46LZTM8/NM93C56LZTM8/NM93C66LZTM8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM93C06LZEN/NM93C46LZEN/NM93C56LZEN/NM93C66LZEN
NM93C06LZEM8/NM93C46LZEM8/NM93C56LZEM8/NM93C66LZEM8
NM93C06LZTEM8/NM93C46LZTEM8/NM93C56LZTEM8/NM93C66LZTEM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06LZ/46LZ/56LZ/66LZ	0°C to +70°C
NM93C06LZE/46LZE/56LZE/66LZE	−40°C to +85°C
Power Supply (V_{CC}) Range:	
ERAL/WRALL Operation	3.0V to 6.0V
All Other Modes (Note 6)	2.0V to 6.0V

DC and AC Electrical Characteristics: 2V < V_{CC} < 4.5V

Symbol	Parameter	Part Number	Conditions	Min	Typ	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250 kHz		0.4	1	mA
I_{CCS}	Standby Current		CS = 0V		0.5	1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)			±200	nA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 0.8 V_{CC}		0.15 V_{CC} V_{CC} + 1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}		0.2	V
f_{SK}	SK Clock Frequency		(Note 5)	0		250	kHz
t_{SKH}	SK High Time			1			μs
t_{SKL}	SK Low Time			1			μs
t_{SKS}	SK Setup Time			0.2			μs
t_{CS}	Minimum CS Low Time		(Note 2)	1			μs
t_{CSS}	CS Setup Time			0.2			μs
t_{DH}	DO Hold Time			70			ns
t_{DIS}	DI Setup Time			0.4			μs
t_{CSH}	CS Hold Time			0			μs
t_{DIH}	DI Hold Time			0.4			μs
t_{PD1}	Output Delay to "1"					2	μs
t_{PD0}	Output Delay to "0"					2	μs
t_{SV}	CS to Status Valid					1	μs
t_{DF}	CS to DO in TRI-STATE®		CS = V_{IL}			0.4	μs
t_{WP}	Write Cycle Time	NM93C06LZ NM93C46LZ NM93C56LZ	V_{CC} = 2.0V V_{CC} = 2.5V V_{CC} = 3.0V		15 10 8	25 15 10	ms ms ms
		NM93C06LZE NM93C46LZE NM93C56LZE NM93C66LZE	V_{CC} = 2.0V V_{CC} = 2.5V V_{CC} = 3.0V		40 12 10	50 15 15	ms ms ms

DC and AC Electrical Characteristics: 4.5V ≤ V_{CC} ≤ 6.0V

Symbol	Parameter	Part Number	Conditions	Min	Typ	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1 MHz		0.4	1	mA
I_{CCS}	Standby Current		CS = 0V		0.4	1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)			±200	nA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		(Note 7)	−0.1 2		0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OL} = −400 μA	 2.4		0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}		0.2	V
f_{SK}	SK Clock Frequency		(Note 5)	0		1	MHz
t_{SKH}	SK High Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE		250 300			ns
t_{SKL}	SK Low Time			250			ns
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	50			ns
t_{CS}	Minimum CS Low Time		(Note 2)	250			ns
t_{CSS}	CS Setup Time			50			ns
t_{DH}	DO Hold Time			70			ns
t_{DIS}	DI Setup Time			100			ns
t_{CSH}	CS Hold Time			0			ns
t_{DIH}	DI Hold Time			20			ns
t_{PD1}	Output Delay to "1"					500	ns
t_{PD0}	Output Delay to "0"					500	ns
t_{SV}	CS to Status Valid					500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}			100	ns
t_{WP}	Write Cycle Time				6	10	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 3)

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

Note 6: LOW VOLTAGE OPERATION: All functional modes are guaranteed over the specified V_{CC} range (as shown in the **Operating Conditions** and **DC/AC Electrical Characteristics**) EXCEPT the ERAL and WRALL bulk programming modes. These bulk programming commands, which reprogram the entire array, are only guaranteed for the V_{CC} range shown on page 3.

Note 7: For operation at V_{CC} levels greater than 5.5V, V_{IH} must conform to EXTENDED VOLTAGE levels where $V_{IH} = V_{CC} - 0.2V$.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.0V ≤ V_{CC} < 4.5V (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10 μA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/ 0.4 mA
5.5V < V_{CC} ≤ 6.0V (Extended Voltage Levels)	0.3V/5.8V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/ 0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The NM93C06LZ/C46LZ/C56LZ/C66LZ devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10 bits carry the op code and the 8-bit address for register selection. All data in signals are clocked into the device on the low-to-high SK transition.

Read (READ): The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN): When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (WEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or until V_{CC} is completely removed from the part.

Erase (ERASE): The ERASE instruction will program all bits in the selected register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE): The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL): The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL): The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS): To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: NSC CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" or "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06LZ and NM93C46LZ

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Read data stored in memory, at selected address
WEN	1	00	11XXXX		Enable all programming modes
ERASE	1	11	A5–A0		Erase selected register
WRITE	1	01	A5–A0	D15–D0	Writes selected register
ERAL	1	00	10XXXX		Erases all registers
WRALL	1	00	01XXXX	D15–D0	Writes all registers
WDS	1	00	00XXXX		Disables all programming modes

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06LZ.

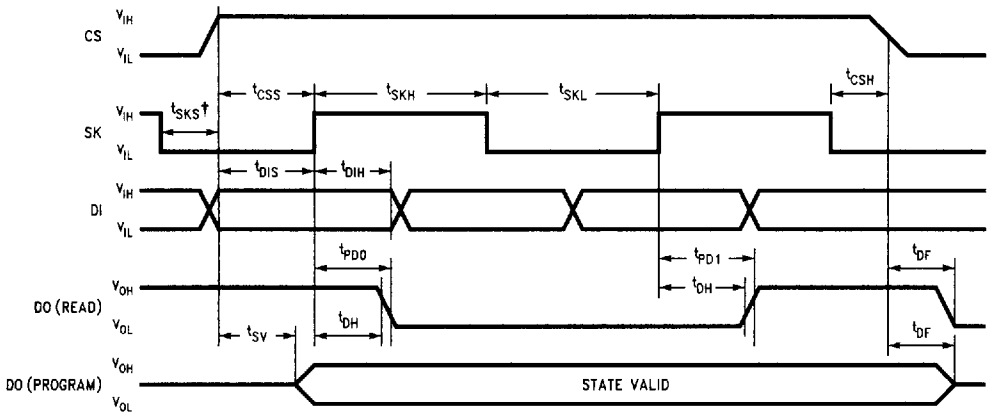
Instruction Set for the NM93C56LZ and NM93C66LZ

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Read data stored in memory, at specified address
WEN	1	00	11XXXXXX		Enable all programming modes
ERASE	1	11	A7–A0		Erase selected register
ERAL	1	00	10XXXXXX		Erases all registers
WRITE	1	01	A7–A0	D15–D0	Write selected registers
WRALL	1	00	01XXXXXX	D15–D0	Writes all registers
WDS	1	00	00XXXXXX		Disables all programming modes

Note: Address bits A7 becomes "Don't Care" for the NM93C56LZ.

Timing Diagrams

Synchronous Data Timing



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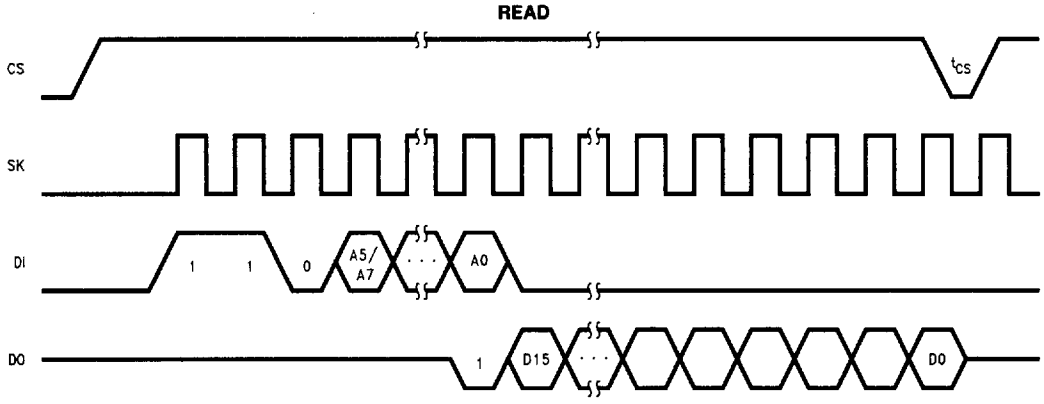
READ



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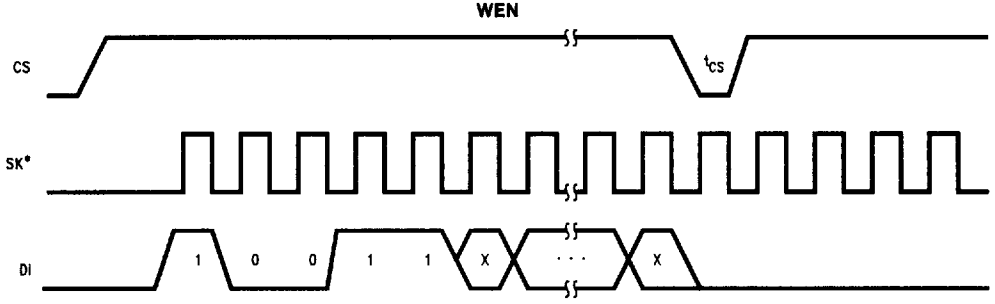
WEN



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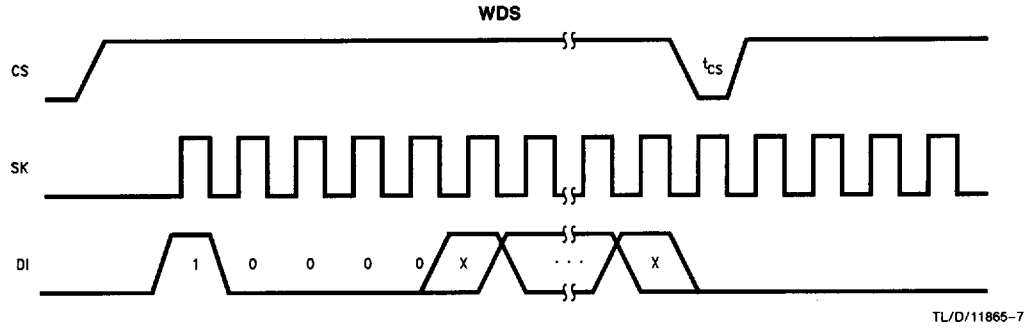
Timing Diagrams (Continued)



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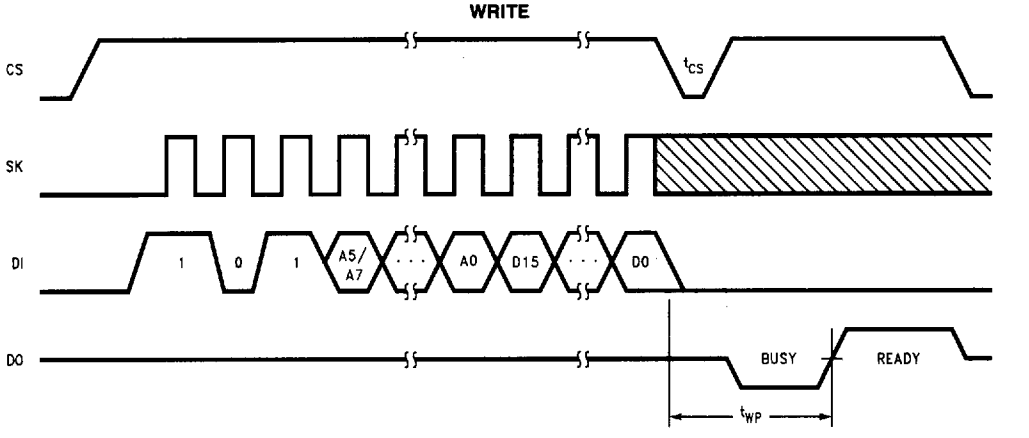

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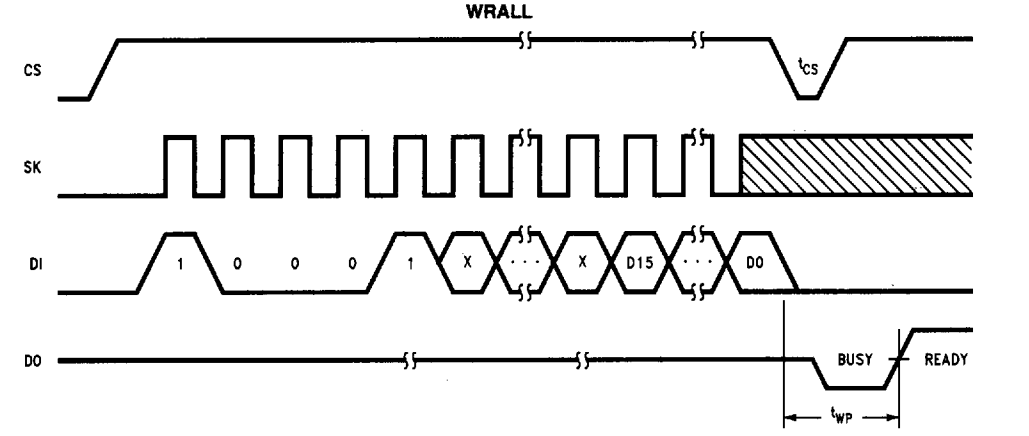

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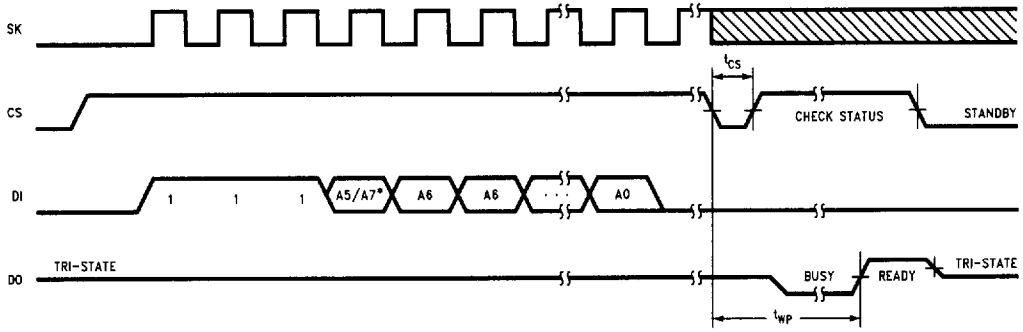
Timing Diagrams (Continued)

ERASE



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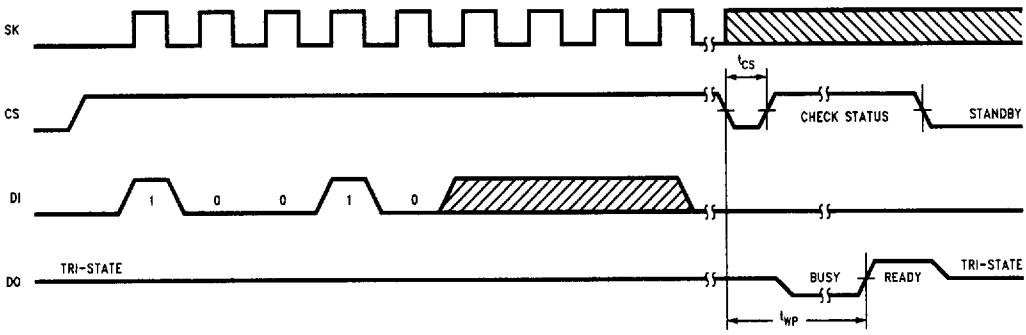
ERAL



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