T-46-23-12

CY7C128A

CYPRESS SEMICONDUCTOR

2048 x 8 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 15 ns
- Low active power
  - 440 mW (commercial)
  - 550 mW (military)
- Low standby power
  - 110 mW
- SOJ package
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- V_{IH} of 2.2V

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

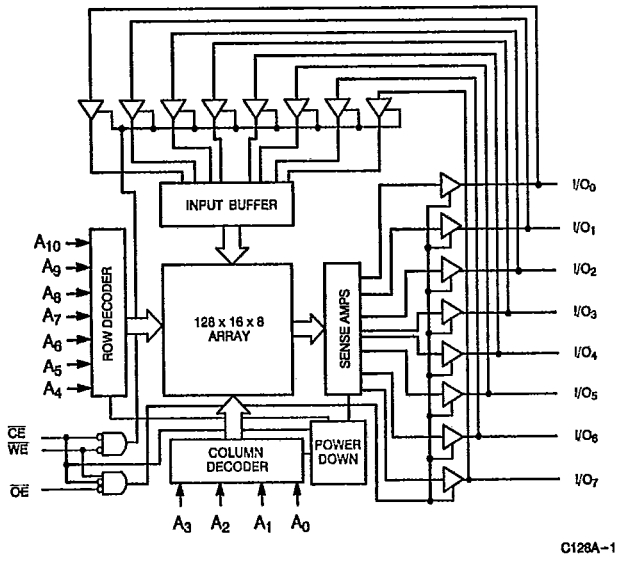
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C128A utilizes a die coat to insure alpha immunity.

Logic Block Diagram



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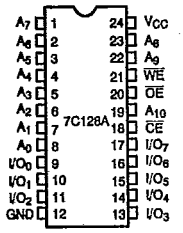
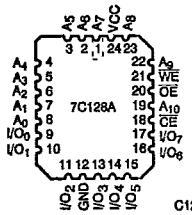
Pin Configurations

DIP/SOJ
Top View



C128A-2

LCC
Top View



C128A-3

Selection Guide

		7C128A-15	7C128A-20	7C128A-25	7C128A-35	7C128A-45	7C128A-55
Maximum Access Time (ns)		15	20	25	35	45	55
Maximum Operating Current (mA)	Commercial	120	100	100	100	100	80
	Military		125	125	100	100	100
Maximum Standby Current (mA)	Commercial	40/40	40/20	20	20	20	20
	Military		40/20	40	20	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to + 150°C

Ambient Temperature with Power Applied ..... − 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to + 7.0V

DC Input Voltage ..... − 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

SRAMs

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C128A-15		7C128A-20		7C128A-25, 35, 45		7C128A-55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		100		100		80	mA
			Mil 25				125		125		125	
			Mil 35,45				125		100		100	
I_{SB1}	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%	Com'l		40		40		20		20	mA
			Mil 25				40		40		20	
			Mil 35,45				40		20		20	
I_{SB2}	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V or $V_{IN} \leq$ 0.3V	Com'l		40		20		20		20	mA
			Mil				20		20		20	

Notes:

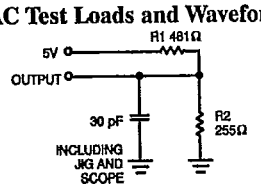
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance[5]

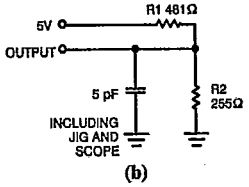
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		10	pF

5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

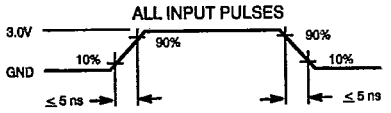


(a)



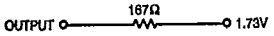
(b)

C128A-4



C128A-5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2,6]

Parameters	Description	7C128A-15		7C128A-20		7C128A-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address to Data Valid		15		20		25	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		8		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7,8]		8		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	15		20		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		ns
t_{AW}	Address Set-Up to Write End	12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns

Switching Characteristics Over the Operating Range (continued)

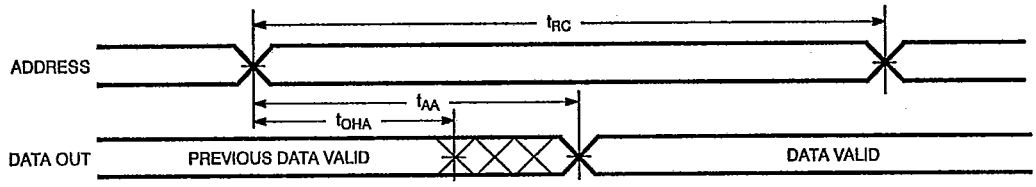
Parameters	Description	7C128A-35		7C128A-45		7C128A-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7,8]		15		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		25		25	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	25		40		50		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		30		40		ns
t_{AW}	Address Set-Up to Write End	25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		20		25		ns
t_{SD}	Data Set-Up to Write End	15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns

Notes:

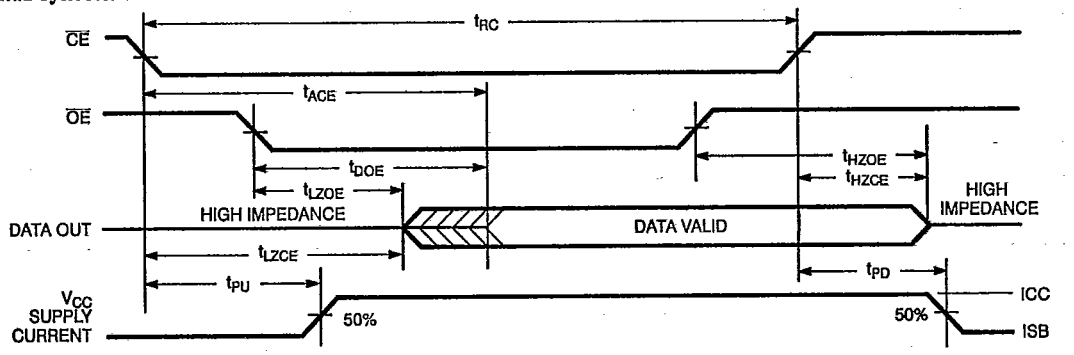
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

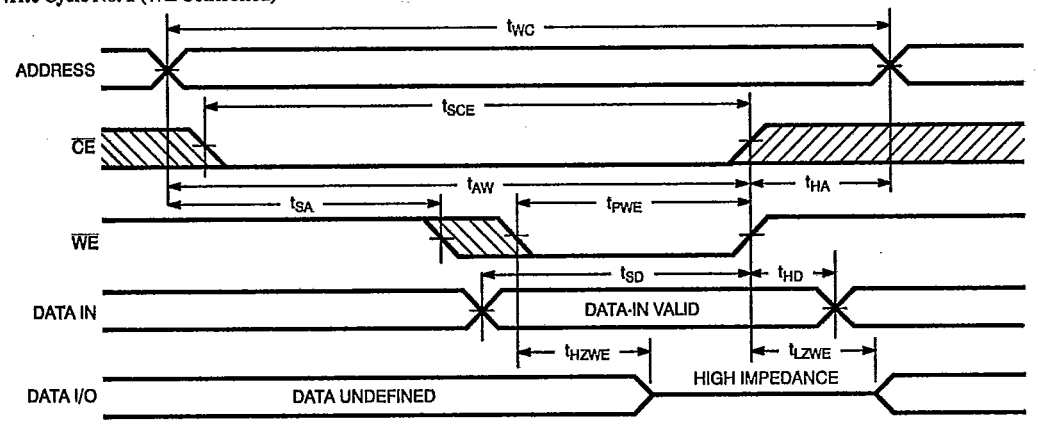
Read Cycle No. 1[10,11]



Read Cycle No. 2[10, 12]

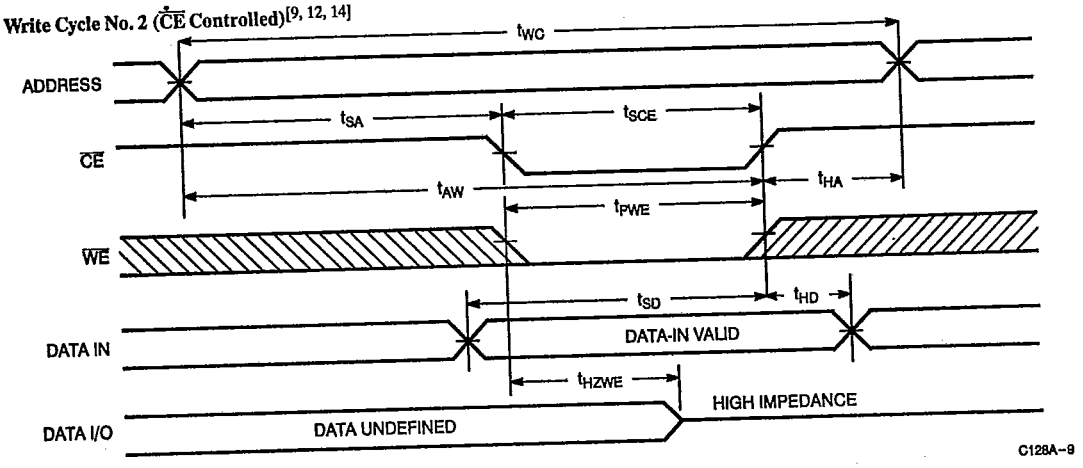


Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]

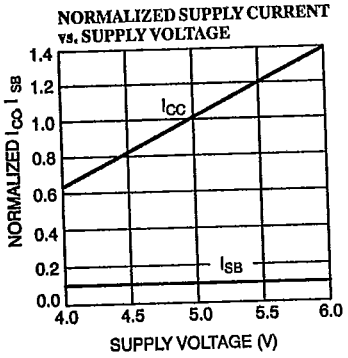


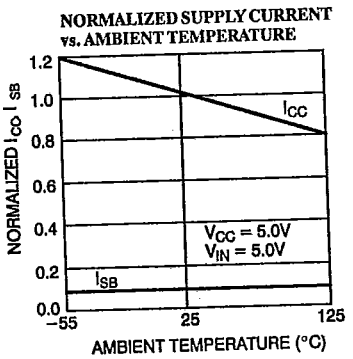
Switching Waveforms (continued)

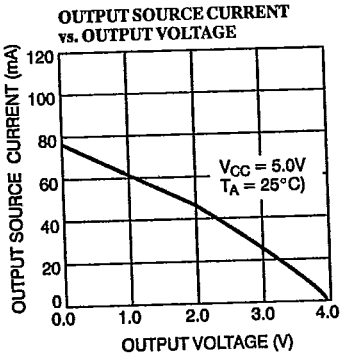
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 12, 14]

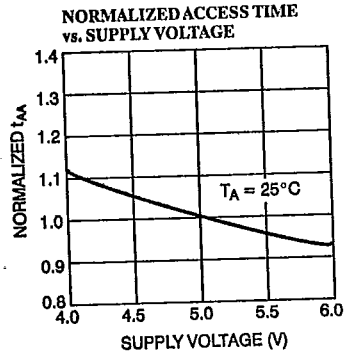


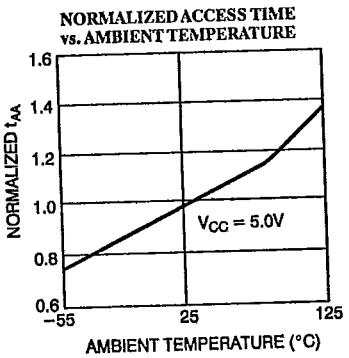
Typical DC and AC Characteristics

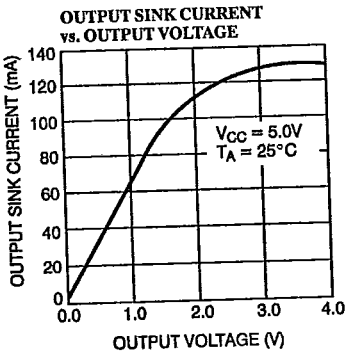






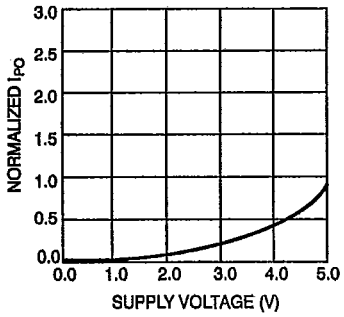




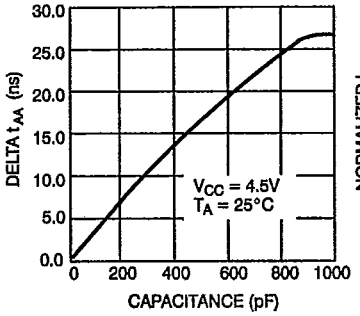


Typical DC and AC Characteristics (continued)

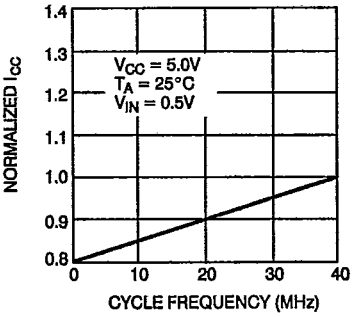
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C128A–15PC	P13	Commercial
	CY7C128A–15VC	V13	
	CY7C128A–15DC	D14	
	CY7C128A–15LC	L53	
20	CY7C128A–20PC	P13	Commercial
	CY7C128A–20VC	V13	
	CY7C128A–20DC	D14	
	CY7C128A–20LC	L53	
	CY7C128A–20DMB	D14	Military
	CY7C128A–20LMB	L53	
	CY7C128A–20KMB	K73	
25	CY7C128A–25PC	P13	Commercial
	CY7C128A–25VC	V13	
	CY7C128A–25DC	D14	
	CY7C128A–25LC	L53	
	CY7C128A–25DMB	D14	Military
	CY7C128A–25LMB	L53	
	CY7C128A–25KMB	K73	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C128A–35PC	P13	Commercial
	CY7C128A–35VC	V13	
	CY7C128A–35DC	D14	
	CY7C128A–35LC	L53	
	CY7C128A–35DMB	D14	Military
	CY7C128A–35LMB	L53	
	CY7C128A–35KMB	K73	
45	CY7C128A–45PC	P13	Commercial
	CY7C128A–45VC	V13	
	CY7C128A–45DC	D14	
	CY7C128A–45LC	L53	
	CY7C128A–45DMB	D14	Military
	CY7C128A–45LMB	L53	
	CY7C128A–45KMB	K73	
55	CY7C128A–55PC	P13	Commercial
	CY7C128A–55VC	V13	
	CY7C128A–55DC	D14	
	CY7C128A–55LC	L53	
	CY7C128A–55DMB	D14	Military
	CY7C128A–55LMB	L53	
	CY7C128A–55KMB	K73	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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