

**Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs; damping resistor; 3-state**
**74LVC2245A  
74LVCH2245A**
**FEATURES**

- 5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 2.7 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when  $V_{CC} = 0$  V
- Bushold on all data inputs (LVCH245A only).
- Integrated  $30\Omega$  damping resistor.

**DESCRIPTION**

The 74LVC(H)2245A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V/5 V environment

The 74LVC(H)2245A is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '245' features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) input for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated.

The '2245' is identical to the '2640' but has true (non-inverting) outputs.

**FUNCTION TABLE**

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	$A_n$	$B_n$
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

**QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	$C_L = 50$ pF $V_{CC} = 3.3$ V	4.1	ns
$C_I$	input capacitance		5.0	pF
$C_{IO}$	input/output capacitance		10	pF
$C_{PD}$	power dissipation capacitance per buffer	notes 1 and 2	40	pF

**Notes to the quick reference data**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;

$f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. The condition is  $V_i = \text{GND to } V_{CC}$ .

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)2245AD	20	SO20	plastic	SOT163-1
74LVC(H)2245ADB	20	SSOP20	plastic	SOT339-1
74LVC(H)2245APW	20	TSSOP20	plastic	SOT360-1

**PINNING**

PIN	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	$A_0$ to $A_7$	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$B_0$ to $B_7$	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	$V_{CC}$	positive supply voltage

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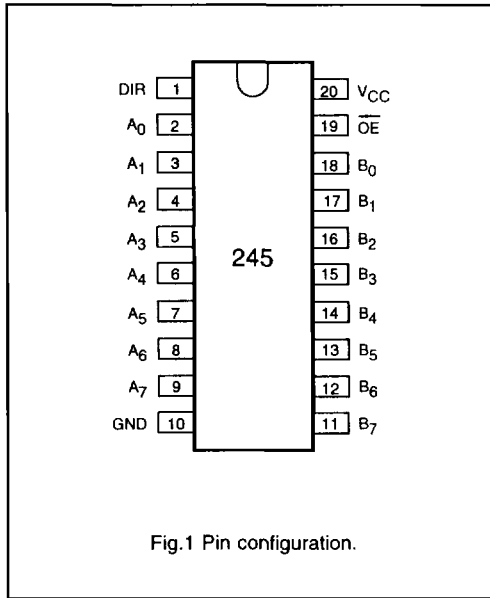


Fig.1 Pin configuration.

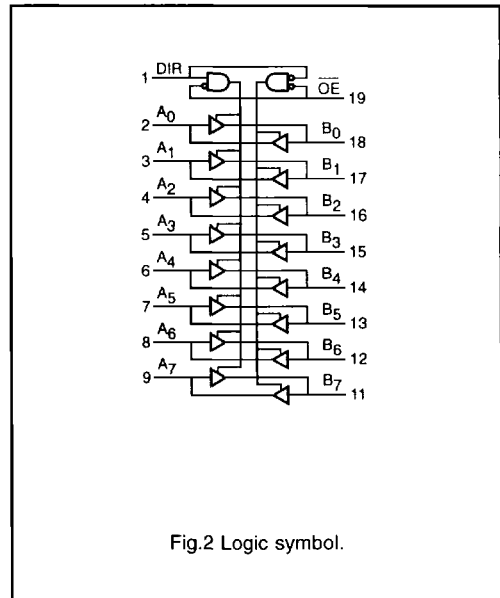


Fig.2 Logic symbol.

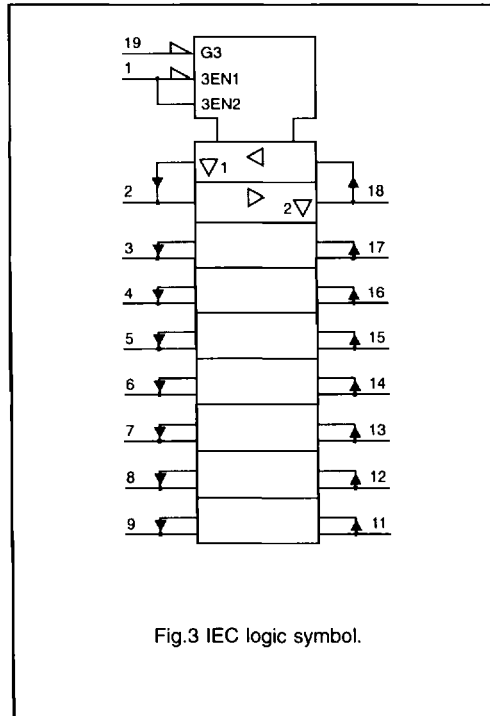


Fig.3 IEC logic symbol.

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#### DC CHARACTERISTICS FOR 74LVC(H)2245A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

$I_{CC}$  category: MSI

#### AC CHARACTERISTICS FOR 74LVC(H)2245A

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				$V_{CC}$ (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
$t_{PHL}/t_{PLH}$	propagation delay	–	–	–	ns	1.2 2.7 3.0 to 3.6	Figs 4, 6
	$A_n$ to $B_n$ ; $B_n$ to $A_n$	1.5	–	9.5			
$t_{PZH}/t_{PZL}$	3-state output enable time	–	–	–	ns	1.2 2.7 3.0 to 3.6	Figs 5, 6
	$\overline{OE}$ to $A_n$ ; $\overline{OE}$ to $B_n$	1.5	–	10.5			
$t_{PHZ}/t_{PLZ}$	3-state output disable time	–	–	–	ns	1.2 2.7 3.0 to 3.6	Figs 5, 6
	$\overline{OE}$ to $A_n$ ; $\overline{OE}$ to $B_n$	1.5	–	8.0			
		1.5	–	7.0			

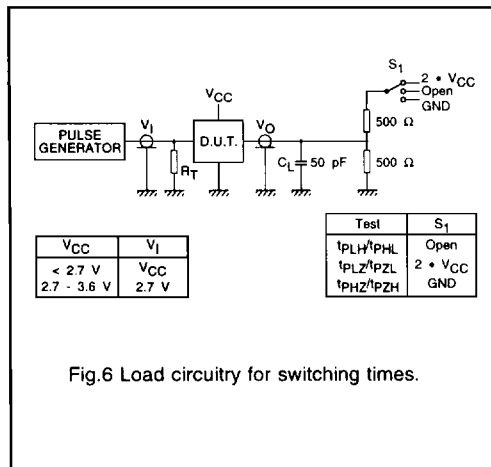
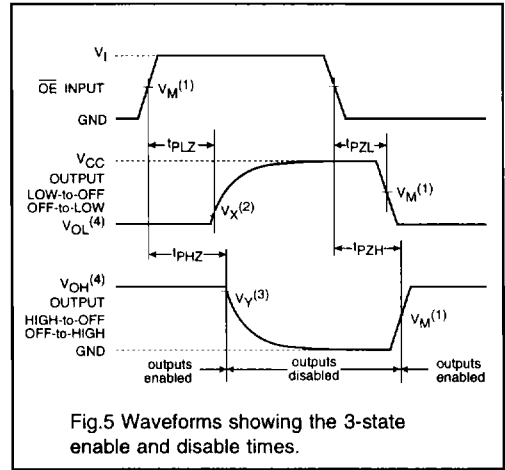
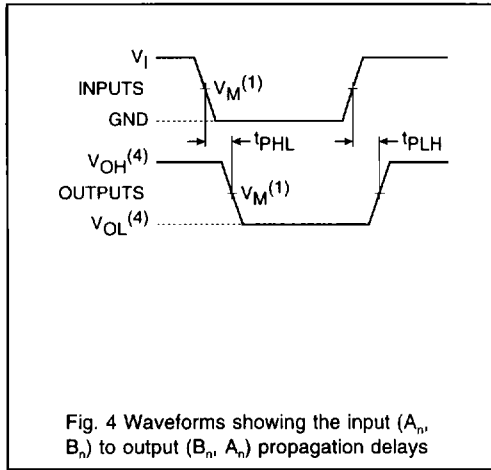
**Notes:** All typical values are measured at  $T_{amb} = 25$  °C.

\* Typical values are measured at  $V_{CC} = 3.3$  V.

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AC WAVEFORMS



- Notes:
- (1)  $V_M = 0.5 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V  
 $V_M = 1.5$  V at  $V_{CC} \geq 2.7$  V
  - (2)  $V_X = V_{OL} + 0.3$  V at  $V_{CC} \geq 2.7$  V  
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V
  - (3)  $V_Y = V_{OH} - 0.3$  V at  $V_{CC} \geq 2.7$  V  
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V
  - (4)  $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.