



FAST CMOS OCTAL TRANSPARENT LATCH

IDT74FCT373A/C

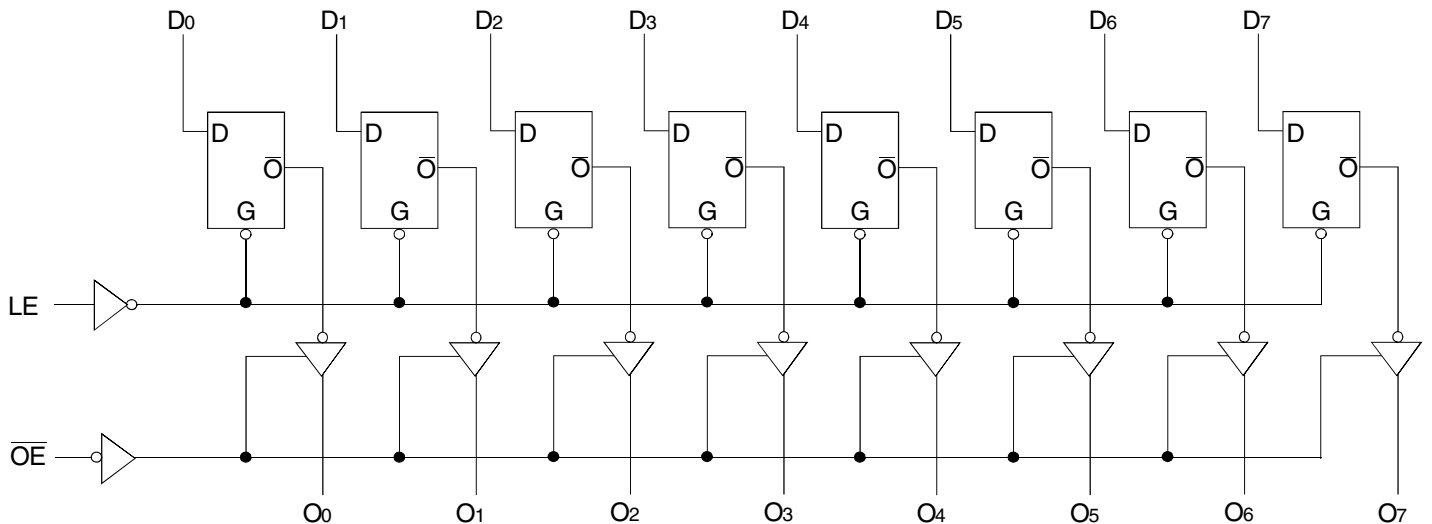
FEATURES:

- IDT74FCT373A up to 30% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- $I_{OL} = 48\text{mA}$
- CMOS power levels (1mW typ. static)
- Octal transparent latch with 3-state output control
- Available in SOIC package

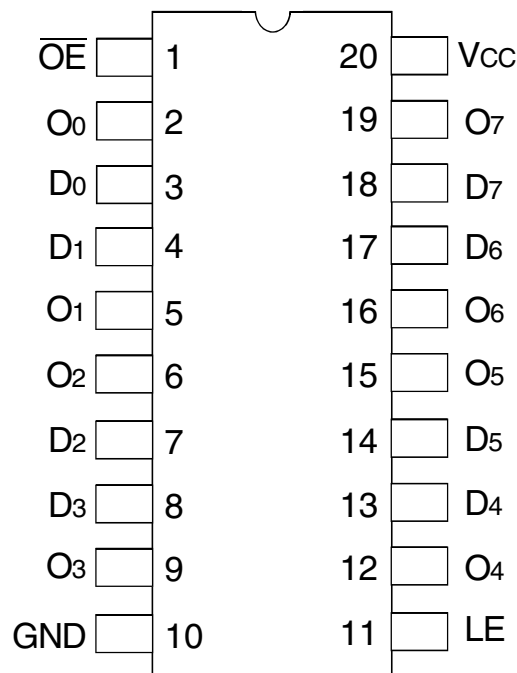
DESCRIPTION:

The IDT74FCT373 is an octal transparent latch built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is high. When LE is low, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is low. When \overline{OE} is high, the bus output is in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature under BIAS	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	0.5	W
I _{OUT}	DC Output Current	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
Dx	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
Ox	3-State Outputs
\overline{Ox}	Complementary 3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
Dx	LE	\overline{OE}	Ox
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

1. H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	5	μA
			$V_i = 2.7V$	—	—	5 ⁽⁴⁾	
I_{IL}	Input LOW Current		$V_i = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_i = GND$	—	—	-5	
I_{OZH}	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_o = V_{CC}$	—	—	10	μA
			$V_o = 2.7V$	—	—	10 ⁽⁴⁾	
I_{OZL}			$V_o = 0.5V$	—	—	-10 ⁽⁴⁾	
			$V_o = GND$	—	—	-10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18mA$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = GND$ ⁽³⁾	-60	-120	—	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	V_{HC}	V_{CC}	—	V	
		$V_{CC} = \text{Min}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}		—
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -15mA$	2.4	4.3		—
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	V_{LC}	V	
		$V_{CC} = \text{Min}$	$I_{OL} = 300\mu A$	—	GND		V_{LC} ⁽⁴⁾
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48mA$	—	0.3		0.5

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE} = GND$ One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle $\overline{OE} = GND$ LE = V _{CC} One Bit Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2	5	
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle $\overline{OE} = GND$ LE = V _{CC} Eight Bits Toggling	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	5.2	14.5 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V_{CC} = 5.0V, +25°C ambient.

3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for register devices (zero for non-register devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

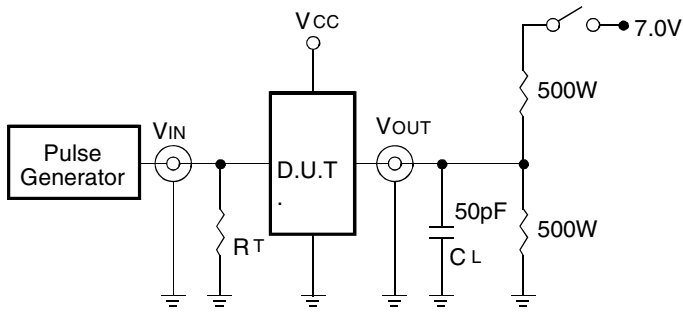
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT373A		FCT373C		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Dx to Ox	CL = 50pF RL = 500Ω	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay LE to Ox		2	8.5	2	5.5	ns
tPZH tPZL	Output Enable Time		1.5	6.5	1.5	5.5	ns
tPHZ tPLZ	Output Disable Time		1.5	5.5	1.5	5	ns
tSU	Set-up Time HIGH or LOW, Dx to LE		2	—	2	—	ns
tH	Hold Time HIGH or LOW, Dx to LE		1.5	—	1.5	—	ns
tW	LE Pulse Width HIGH		5	—	5	—	ns

NOTES:

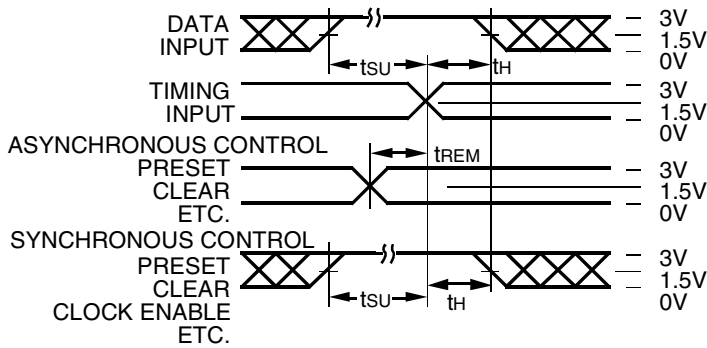
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS



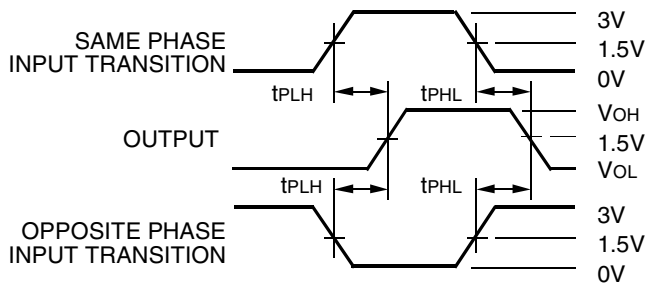
Octal Link

Test Circuits for All Outputs



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Set-Up, Hold, and Release Times



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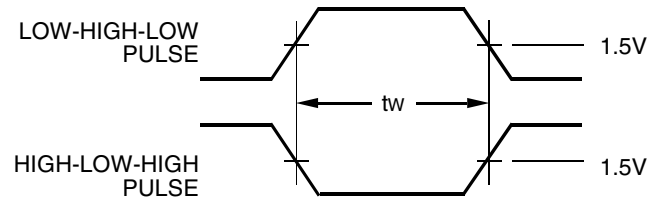
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

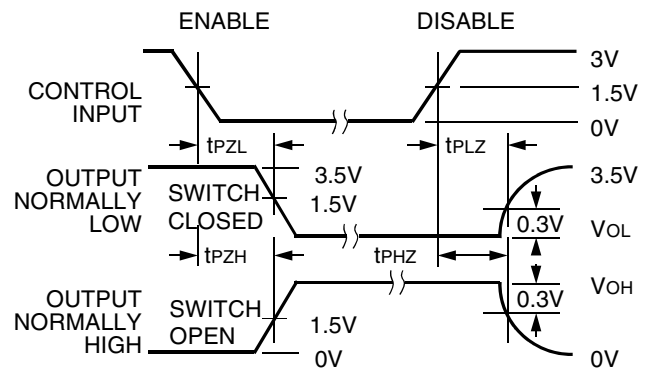
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

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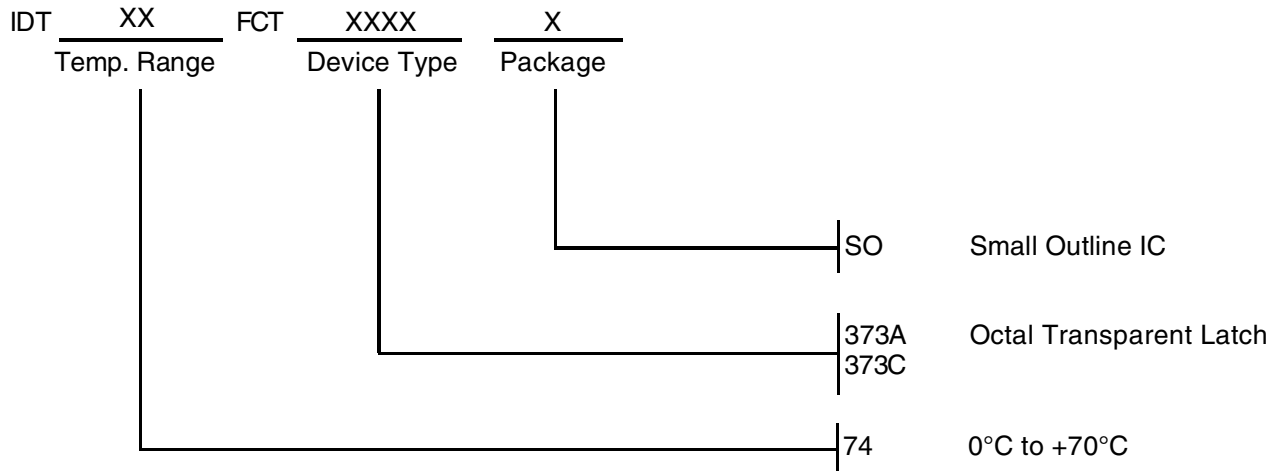
Octal Link

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION



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