NKK

HIGH SPEED CMOS SRAM 1M-BIT(256K X 4)

PRELIMINARY

N341028

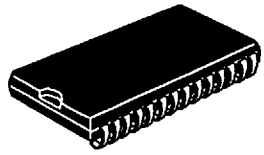
A12, A15

This document contains preliminary information, and is subject to change without notice.

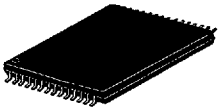
■ Features

- CMOS SRAM organized as 262,144 x 4bits
- Single+5.0V (±10%) Power Supply
- High Speed Access time : 12/15ns
- Low power operation
  - Active : 160mA (Max.)
  - Standby : 10mA (Max.)

- Packages
  - -28pin Plastic SOJ(300mil)
  - -28pin Plastic SOJ(400mil)
  - (Standard Pin Configuration)
  - -28pin Plastic TSOP(Type I)



28pin Plastic SOJ(300mil/ 400mil)



28pin Plastic TSOP(Type I)

■ Description

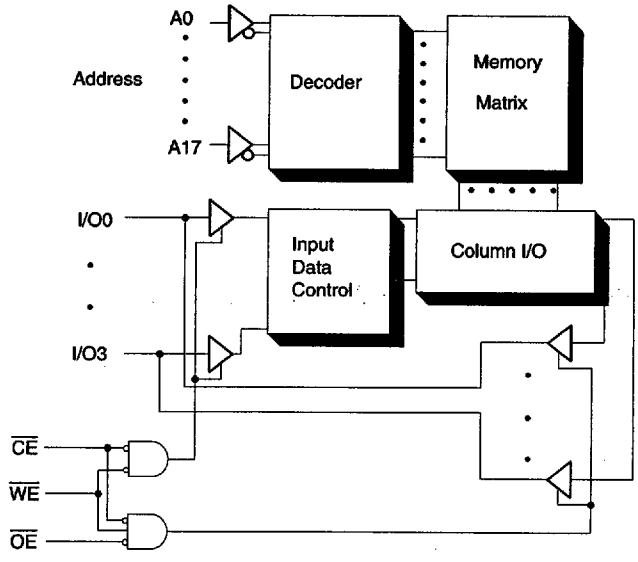
The N341028 is a high performance CMOS static RAM organized as 262,144 x 4bits.

Writing is accomplished when the $\overline{WE}$ and $\overline{CE}$ inputs are both Low.

Reading is accomplished when the $\overline{WE}$ input is High and the $\overline{CE}$ and $\overline{OE}$ inputs are both Low.

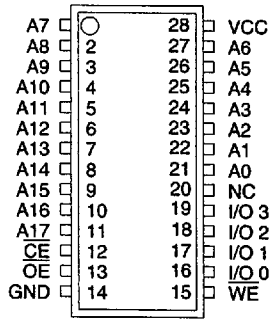
The N341028 operates from a single +5.0V power supply and all inputs and outputs are fully TTL compatible.

■ Functional Block Diagram

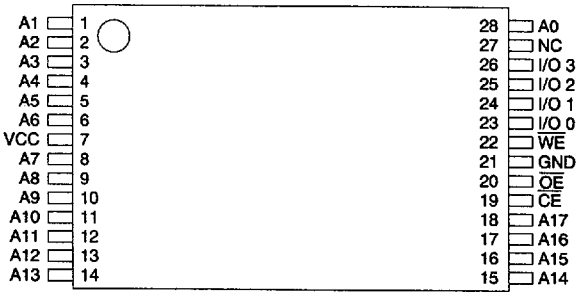


■ Pin Configuration

28 pin Plastic SOJ



28 pin Plastic TSOP (Type I)



Pin Description

SYMBOL	PIN NAME
A0-A17	Address input
I/O0-I/O3	Data input/output
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input
VCC	Power Supply Pin(+5V)
GND	Ground Pin

■ Mode Selection Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	High	High-Z	Standby
Low	High	Low	Data out	Read Cycle
X	Low	Low	Data in	Write Cycle
High	High	Low	High-Z	Output disable

Note : X = don't care.

■ Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to V_{CC}+0.5 (Max. 7.0)	V
T_{OPR}	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
P_D	Power Dissipation	1.0	W

NOTICE

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ Recommended Operating Conditions

Recommended Operating Temperature and Supply Voltage

Ambient Temperature	GND	V_{CC}
0 to 70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	-	0.8	V

Note : V_{IL}(min) = -3.0V for pulse width less than 20ns.

■ Capacitance

(T_{OPR}=25°C, f=1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	8	pF

Note : These parameters are sampled and not 100% tested.

■ DC Electrical Characteristics

Power Supply Currents (VCC=5.0V ± 10%, TOPR=0 to 70°C)

Symbol	Parameter	N341028 A12	N341028 A15	Unit
ICC	Dynamic Operating Current $\overline{CE}$ ≤ VIL, VCC = max, f = fmax, IOUT = 0mA, VIN ≥ VIH or ≤ VIL	160	155	mA
ISB	Standby Power Supply Current (TTL level) $\overline{CE}$ ≥ VIH, VCC = max, f = fmax, VIN ≥ VIH or ≤ VIL	35	35	mA
ISB1	Full Standby Power Supply Current (CMOS level) $\overline{CE}$ ≥ VCC-0.2V, VCC = max, f = 0, VIN ≥ VCC-0.2V or ≤ 0.2V	10	10	mA

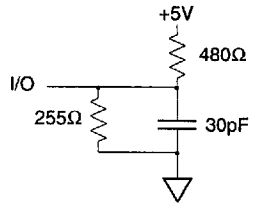
Note : All values are the maximum guaranteed values.

DC Characteristics (VCC=5.0V ± 10%, TOPR=0 to 70°C)

Symbol	Parameter	Condition	N341028		Unit
			Min.	Max.	
ILI	Input Leakage Current	VCC = max, VIN = GND to VCC	-5	5	µA
ILO	Output Leakage Current	VCC = max, $\overline{CE}$ ≥ VIH, VOUT = GND to VCC	-5	5	µA
VOL	Output Low Voltage	IOL =8mA, VCC = min	-	0.4	V
		IOL =10mA, VCC = min	-	0.5	V
VOH	Output High Voltage	IOH =-4mA, VCC = min	2.4	-	V

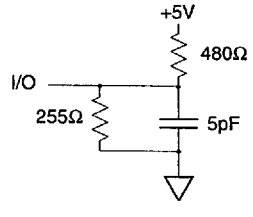
■ AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See Figure 1 and 2



(Including scope and jig)

Figure 1. Output Load Equivalent



(Including scope and jig)

Figure 2. Output Load Equivalent
(for tLZCE, tHZCE, tLZWE, tHZWE, tLZOE, tHZOE)

■ AC Electrical Characteristics

Read Cycle (VCC=5.0V ± 10%, TOPR=0 to 70°C)

Description	Symbol	N341028A12		N341028A15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle time	tRC	12		15		ns
Address access time	tAA		12		15	ns
Chip enable access time	tACE		12		15	ns
Output hold from address change	tOH	4		4		ns
Chip enable to output in Low-Z (1),(2)	tLZCE	3		3		ns
Chip disable to output in High-Z (1),(2)	tHZCE		6		7	ns
Chip enable to power up time (1)	tPU	0		0		ns
Chip disable to power down time (1)	tPD		12		15	ns
Output enable access time	tAOE		6		6	ns
Output enable to output in Low-Z (1),(2)	tLZOE	0		0		ns
Output disable to output in High-Z (1),(2)	tHZOE		5		5	ns

Write Cycle (VCC=5.0V ± 10%, TOPR=0 to 70°C)

Description	Symbol	N341028A12		N341028A15		Unit
Write Cycle		Min.	Max.	Min.	Max.	
Write Cycle time	tWC	12		15		ns
Chip enable to end of write	tCW	10		12		ns
Address valid to end of write	tAW	10		12		ns
Address set-up time	tAS	0		0		ns
Address hold from end of write	tAH	0		0		ns
Write pulse width (3)	tWP	9		11		ns
Data set-up time	tDS	6		7		ns
Data hold time	tDH	0		0		ns
Write disable to output in Low-Z (1),(2)	tLZWE	0		0		ns
Write enable to output in High-Z (1),(2)	tHZWE		5		5	ns

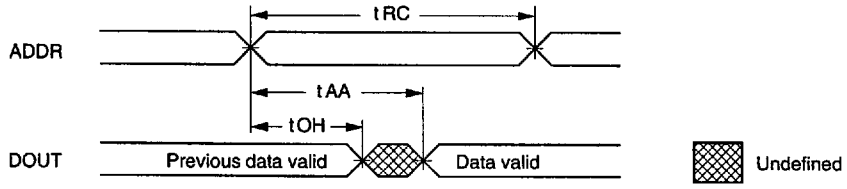
Note : (1) These parameters are sampled and not 100% tested.

(2) Transition is measured ± 200mV from steady state voltage.

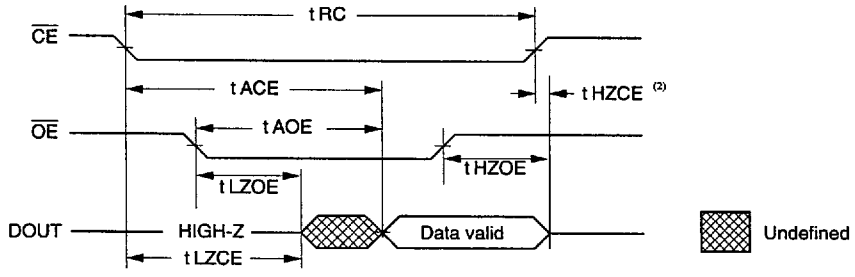
(3) $\overline{OE}$ is continuously High. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ Low, tWP must be greater than or equal to tHZWE + tDS to allow the I/O drivers to turn off and data to be placed on the bus for the required tDS. If $\overline{OE}$ is High during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP.

■ AC Timing Waveforms

Read Cycle No.1[1]



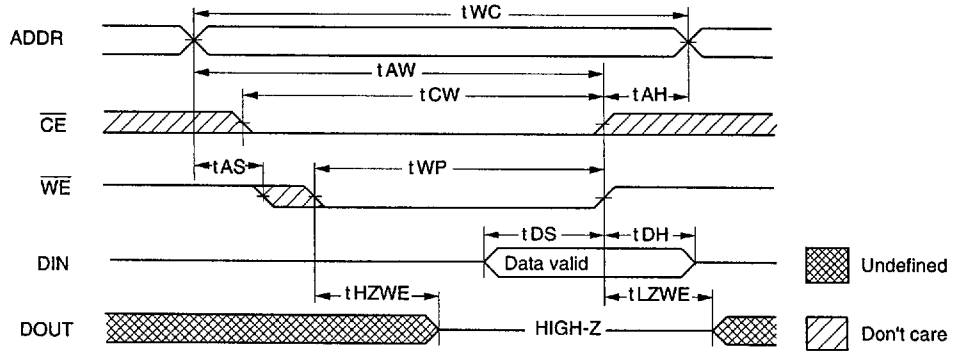
Read Cycle No.2 [1]



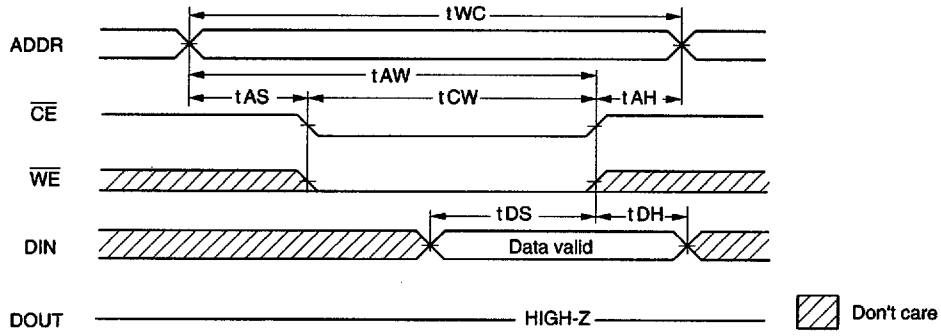
Note : (1) $\overline{WE}$ is High for READ cycle.

(2) At any given temperature and voltage condition, tHZCE is less than tLZCE.

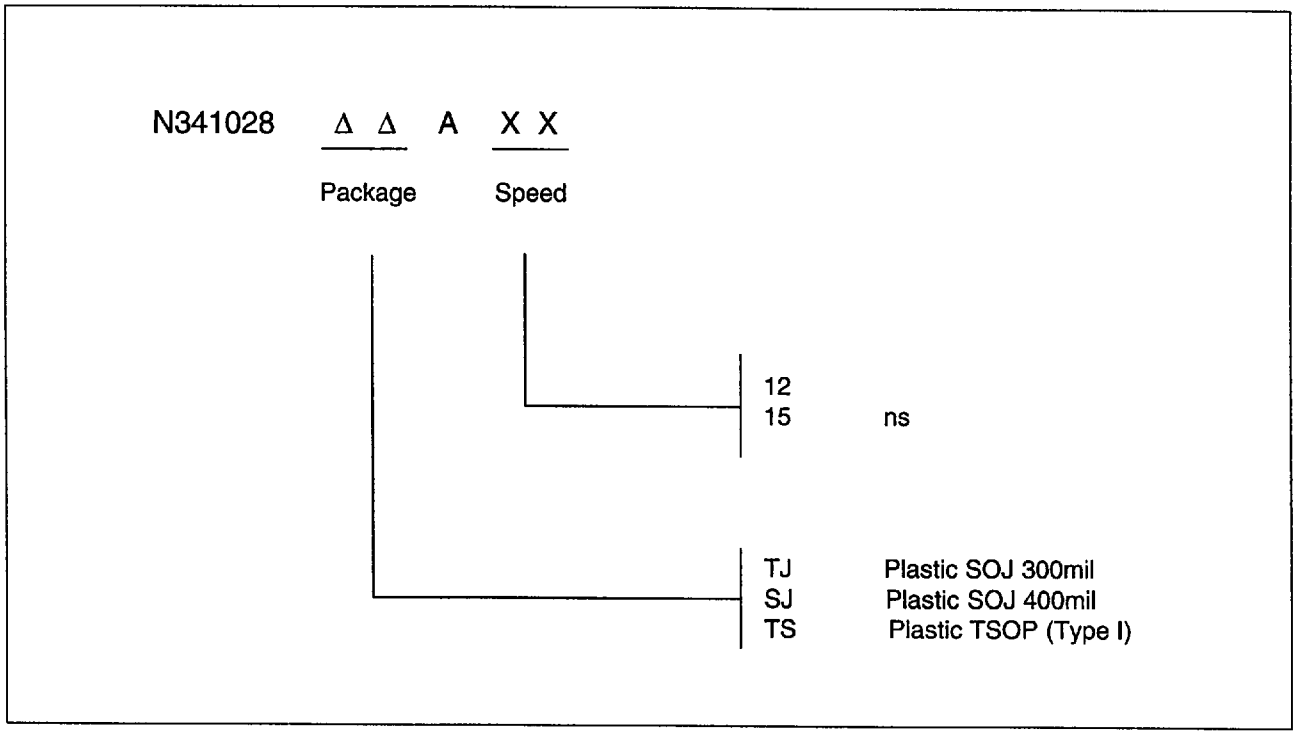
Write Cycle No.1(Write Enable Controlled)



Write Cycle No.2(Chip Enable Controlled)



■ Ordering Information



PART NO.	Access Time (ns)	Operating Current (mA)	Package
N341028TJA12	12	160	28Pin Plastic SOJ (300mil)
N341028SJA12	12	160	28Pin Plastic SOJ (400mil)
N341028TSA12	12	160	28Pin Plastic TSOP (Type I)
N341028TJA15	15	155	28Pin Plastic SOJ (300mil)
N341028SJA15	15	155	28Pin Plastic SOJ (400mil)
N341028TSA15	15	155	28Pin Plastic TSOP (Type I)