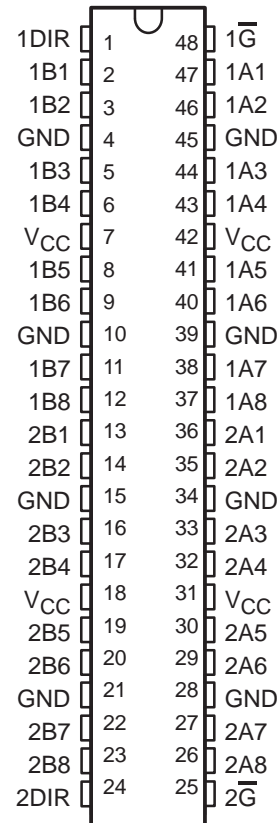


SN54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS097B – DECEMBER 1989 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus™* Family
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configuration to Minimize High-Speed Switching Noise
- *EPIC™* (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, Thin Shrink Small-Outline (DGG) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

SN54ACT16245 . . . WD PACKAGE
74ACT16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The SN54ACT16245 and 74ACT16245 are 16-bit bus transceivers organized as dual-octal noninverting 3-state transceivers and designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The enable (\overline{G}) input can be used to disable the devices so that the buses are effectively isolated.

The SN54ACT16245 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT16245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

CONTROL INPUTS		OPERATION
\overline{G}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

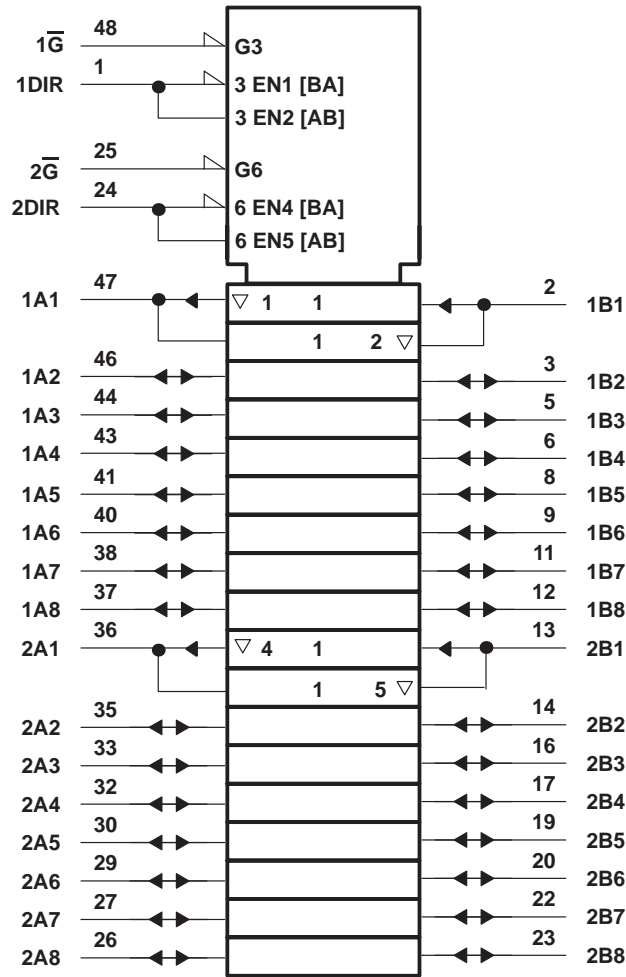
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SN54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

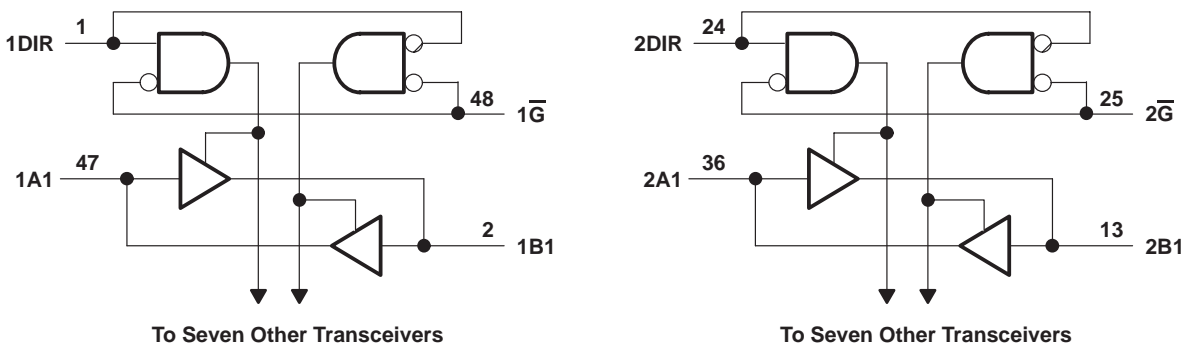
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

	SN54ACT16245		74ACT16245		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage (see Note 4)	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–24	mA
I_{OL} Low-level output current		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	0	10	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

- NOTES: 3. Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater to keep them from floating.
 4. All V_{CC} and GND pins must be connected to the proper voltage power supply.



SN54ACT16245, 74ACT16245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCAS097B – DECEMBER 1989 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT16245		74ACT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4	V	
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.94		3.8		
		5.5 V	4.94			4.94		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
I _{OH} = -75 mA†	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1	0.1	V	
		5.5 V			0.1		0.1	0.1		
	I _{OL} = 24 mA	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I _{OL} = 50 mA†	5.5 V					1.65			
I _{OL} = 75 mA†	5.5 V						1.65			
I _I	Control inputs	V _I = V _{CC} or GND			±0.1		±1	±1	μA	
I _{OZ}	A or B ports‡	V _O = V _{CC} or GND			±0.5		±10	±5	μA	
I _{CC}		V _I = V _{CC} or GND, I _O = 0			8		160	80	μA	
ΔI _{CC} §		One input at 3.4 V, Other inputs at GND or V _{CC}			0.9		1	1	mA	
C _i	Control inputs	V _I = V _{CC} or GND			4.5				pF	
C _{io}	A or B ports	V _O = V _{CC} or GND			16				pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

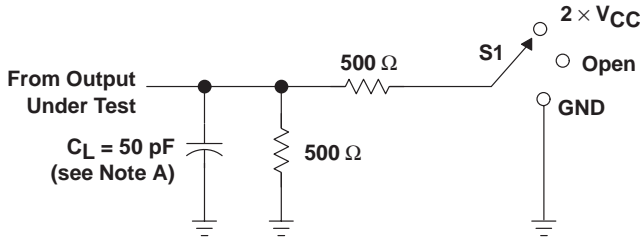
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54ACT16245		74ACT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	3.2	6.9	9.3	3.2	11.5	3.2	10.5	ns
t _{PHL}			2.6	6.4	9.2	2.6	11.1	2.6	10.2	
t _{PZH}	\bar{G}	B or A	2.7	6.4	9.1	2.7	10.9	2.7	10	ns
t _{PZL}			3.4	7.4	10.5	3.4	12.6	3.4	11.6	
t _{PHZ}	\bar{G}	B or A	5.8	9.2	11.6	5.8	13.4	5.8	12.6	ns
t _{PLZ}			5.5	8.5	10.8	5.5	12.7	5.5	11.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	52	pF
		Outputs disabled	10	

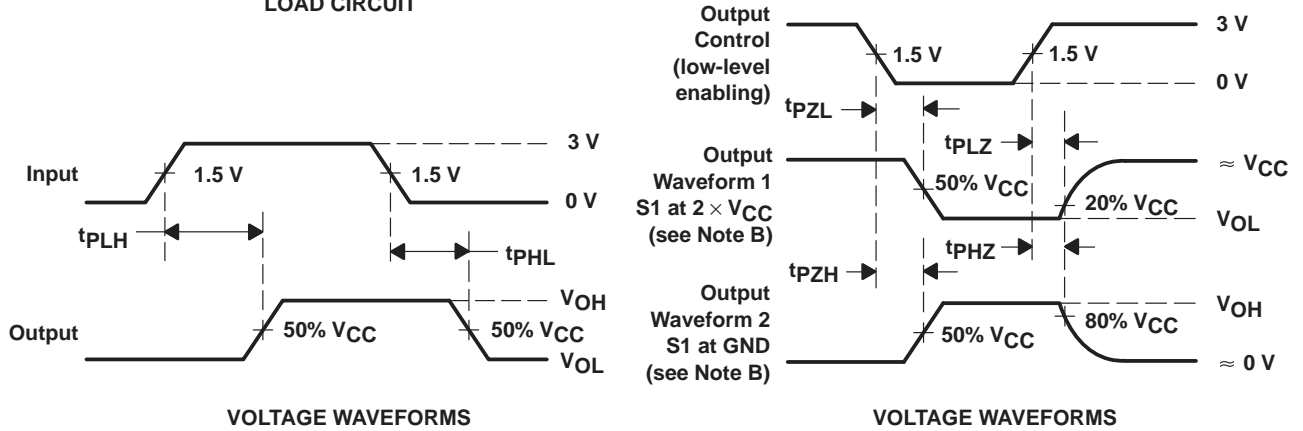


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN54ACT16245, 16-Bit Bus Transceivers With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ACT16245	SN74ACT16245-EP
Voltage Nodes (V)	5	5
Vcc range (V)		4.5 to 5.5
Input Level		TTL
Output Level		CMOS
No. of Outputs		16
Logic		True
Static Current		160 uA
tpd max (ns)		9.3

FEATURES

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DESCRIPTION

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DATASHEET[▲Back to Top](#)Full datasheet in Acrobat PDF: [sn54act16245.pdf](#) (100 KB, Rev.B) (Updated: 04/01/1996)**APPLICATION NOTES**[▲Back to Top](#)View Application Notes for [Digital Logic](#)

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
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- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sheet \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG[▲Back to Top](#)**DEVICE INFORMATION**

Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY
5962-9202301MXA	ACTIVE	CFP (WD) 48	-55 TO 125		View Contents	1KU 22.39	1
SNJ54ACT16245WD	ACTIVE	CFP (WD) 48	-55 TO 125	5962-9202301MXA	View Contents	1KU 22.39	1

TI INVENTORY STATUS

As Of 09:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY DATE	LEAD TIME
0*	> 10k 20 May	6 WKS
941*	> 10k 20 May	6 WKS

REPORTED DISTRIBUTOR INVENTORY

As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
None Reported View Distributors		
None Reported View Distributors		

Table Data Updated on: 4/17/2003