**TENTATIVE** TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

# 1,048,576-WORD × 16-BIT EDO (HYPER PAGE) DYNAMIC RAM

## DESCRIPTION

The TC51V18165CJ/CFT is an EDO (hyper page) dynamic RAM organized as 1,048,576 words by 16 bits. The TC51V18165CJ/CFT utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC51V18165CJ/CFT to be packaged in a 42-pin plastic SOJ or a 50-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. Other features include a single power supply of 3.3 V ± 0.3 V tolerance and direct interfacing with high performance logic families such as LVTTL.

## FEATURES

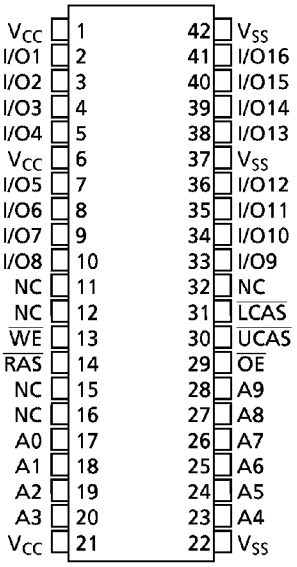
- 1,048,576 word by 16 bit organization
- Fast access time and cycle time

| | | TC51V18165CJ/CFT | |
|---|---|---|---|
| | | -50 | -60 |
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 50 ns | 60 ns |
| $t_{AA}$ | Column Address Access Time | 25 ns | 30 ns |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 14 ns | 17 ns |
| $t_{RC}$ | Cycle Time | 84 ns | 104 ns |
| $t_{HPC}$ | Hyper Page Mode Cycle Time | 20 ns | 25 ns |

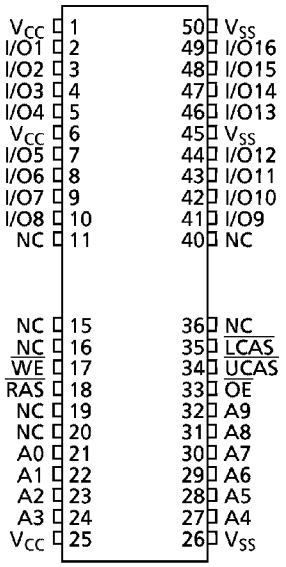
- Single power supply of 3.3 V ± 0.3 V with a built-in $V_{BB}$ generator
- Low-power dissipation (max)
  Operating: 810 mW (50 ns type)
  : 666 mW (60 ns type)
  Stand by : 1.8 mW (both devices)
- Unlatched outputs at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-Only refresh, Hidden refresh and EDO(Hyper Page mode) capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles per 16 ms
- Package
  CJ : SOJ42-P-400-1.27, 1.66 grams
  CFT: TSOP II 50/44-P-400-0.80, 0.53 grams

## PIN ASSIGNMENT (TOP VIEW)

Plastic SOJ




Plastic TSOP

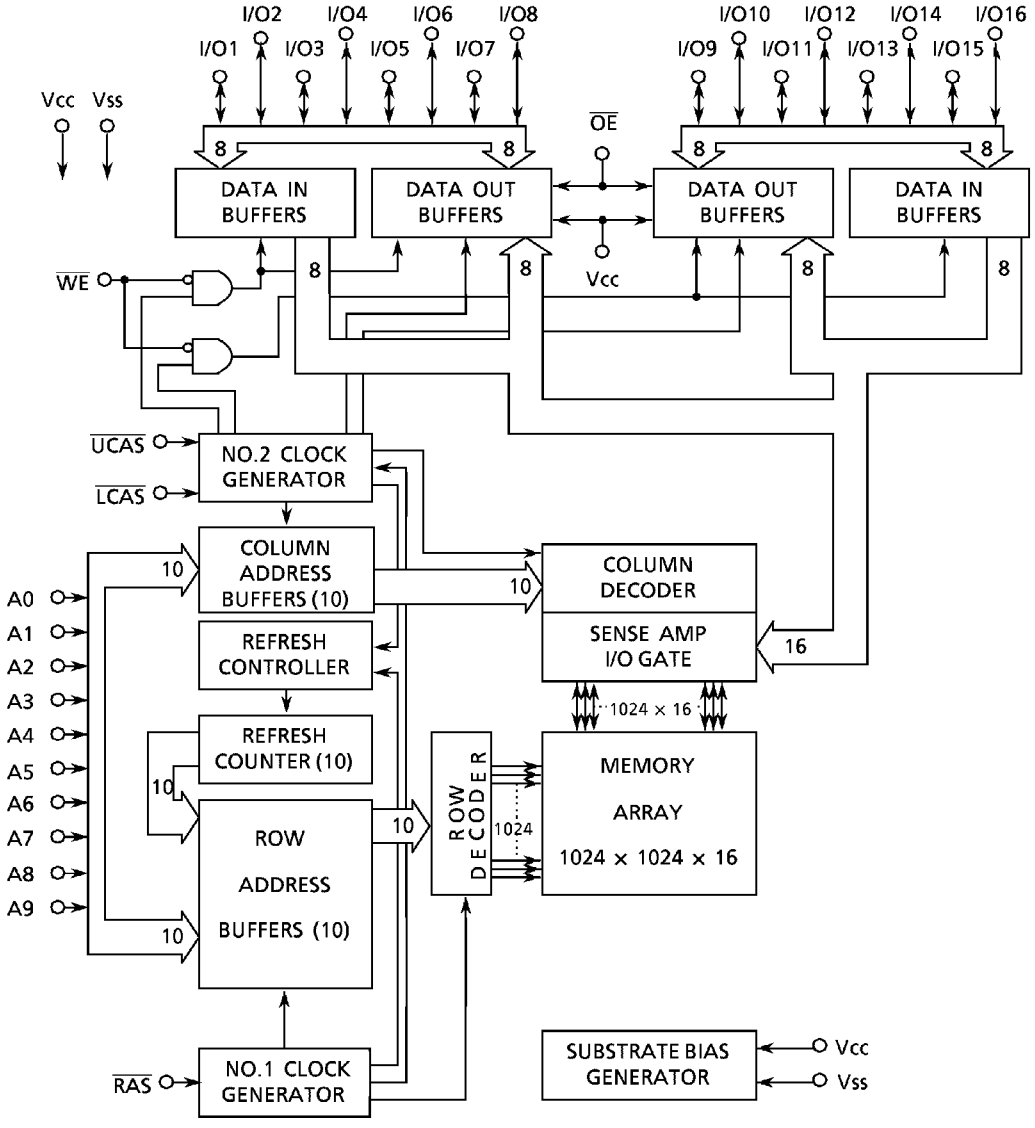



## PIN NAMES

| | |
|---|---|
| A0 to A9 | Address Inputs |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{UCAS}$ | Column Address Strobe /Upper Byte Control |
| $\overline{LCAS}$ | Column Address Strobe /Lower Byte Control |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| I/O1 to I/O16 | Data I/O |
| $V_{CC}$ | Power (+ 3.3 V) |
| $V_{SS}$ | Ground |
| N.C. | No Connection |

961001EBA2

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNIT | NOTES |
|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | − 0.3 to $V_{CC}$ + 0.3 | V | 1 |
| Output Voltage | $V_{OUT}$ | − 0.3 to $V_{CC}$ + 0.3 | V | 1 |
| Power Supply Voltage | $V_{CC}$ | − 0.3 to 4.6 | V | 1 |
| Operating Temperature | $T_{OPR}$ | 0 to 70 | °C | 1 |
| Storage Temperature | $T_{STG}$ | − 55 to 150 | °C | 1 |
| Soldering Temperature (10 s) | $T_{SOLDER}$ | 260 | °C | 1 |
| Power Dissipation | $P_D$ | 1.0 | W | 1 |
| Short Circuit Output Current | $I_{OUT}$ | 50 | mA | 1 |

## DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V | 2 |
| $V_{IH}$ | Input High Voltage | 2.2 | − | $V_{CC}$ + 0.3* | V | 2 |
| $V_{IL}$ | Input Low Voltage | − 0.3** | − | 0.8 | V | 2 |

* $V_{CC}$ + 1.2 V at pulse width ≦ 20 ns (pulse width is measured at $V_{CC}$)

** − 1.2 V at pulse width ≦ 20 ns (pulse width is measured at $V_{SS}$)

## DC CHARACTERISTICS ($V_{CC}$ = 3.3 V ± 0.3 V, Ta = 0° to 70°C)

| SYMBOL | PARAMETER | | MIN | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | OPERATING CURRENT<br>Average Power Supply Operating Current<br>($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: $t_{RC}$ = $t_{RC}$ min) | TC51V18165CJ/CFT-50 | – | 225 | mA | 3, 4, 5 |
| | | TC51V18165CJ/CFT-60 | – | 185 | | |
| $I_{CC2}$ | STANDBY CURRENT<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = $V_{IH}$) | | – | 1 | mA | |
| $I_{CC3}$ | $\overline{RAS}$-ONLY REFRESH CURRENT<br>Average Power Supply Current, $\overline{RAS}$-Only Mode<br>($\overline{RAS}$ Cycling, $\overline{UCAS}$ = $\overline{LCAS}$ = $V_{IH}$: $t_{RC}$ = $t_{RC}$ min) | TC51V18165CJ/CFT-50 | – | 225 | mA | 3, 5 |
| | | TC51V18165CJ/CFT-60 | – | 185 | | |
| $I_{CC4}$ | HYPER PAGE MODE CURRENT<br>Average Power Supply Current, Hyper Page Mode<br>($\overline{RAS}$ = $V_{IL}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: $t_{HPC}$ = $t_{HPC}$ min) | TC51V18165CJ/CFT-50 | – | 145 | mA | 3, 4, 5 |
| | | TC51V18165CJ/CFT-60 | – | 125 | | |
| $I_{CC5}$ | STANDBY CURRENT<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = $V_{CC}$ – 0.2 V) | | – | 500 | μA | |
| $I_{CC6}$ | $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT<br>Average Power Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Mode<br>($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Cycling: $t_{RC}$ = $t_{RC}$ min) | TC51V18165CJ/CFT-50 | – | 225 | mA | 3, 5 |
| | | TC51V18165CJ/CFT-60 | – | 185 | | |
| $I_{I\ (L)}$ | INPUT LEAKAGE CURRENT<br>Input Leakage Current, any input<br>(0 V ≦ $V_{IN}$ ≦ $V_{CC}$, All Other Pins Not under Test = 0 V) | | – 10 | 10 | μA | |
| $I_{O\ (L)}$ | OUTPUT LEAKAGE CURRENT<br>($D_{OUT}$ Is disabled, 0 V ≦ $V_{OUT}$ ≦ $V_{CC}$) | | – 10 | 10 | μA | |
| $V_{OH}$ | OUTPUT LEVEL<br>Output H Level Voltage ($I_{OUT}$ = – 2 mA) | | 2.4 | – | V | |
| $V_{OL}$ | OUTPUT LEVEL<br>Output L Level Voltage ($I_{OUT}$ = 2 mA) | | – | 0.4 | V | |

## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

($V_{CC}$ = 3.3 V ± 0.3 V, Ta = 0° to 70°C) (Notes 6, 7, 8)

| SYMBOL | PARAMETER | TC51V18165CJ/CFT | | | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| | | -50 | | -60 | | | |
| | | MIN | MAX | MIN | MAX | | |
| $t_{RC}$ | Random Read or Write Cycle Time | 84 | – | 104 | – | ns | |
| $t_{RMW}$ | Read-Modify-Write Cycle Time | 111 | – | 135 | – | ns | |
| $t_{RAC}$ | Access Time from $\overline{RAS}$ | – | 50 | – | 60 | ns | 9,14,15 |
| $t_{CAC}$ | Access Time from $\overline{CAS}$ | – | 14 | – | 17 | ns | 9,14 |
| $t_{AA}$ | Access Time from Column Address | – | 25 | – | 30 | ns | 9,15 |
| $t_{CPA}$ | Access Time from $\overline{CAS}$ Precharge | – | 28 | – | 35 | ns | 9 |
| $t_{CLZ}$ | $\overline{CAS}$ to output in Low-Z | 0 | – | 0 | – | ns | |
| $t_{OFF}$ | Output Buffer Turn-off Delay | 0 | 13 | 0 | 15 | ns | 10,16 |
| $t_T$ | Transition Time (Rise and Fall) | 1 | 50 | 1 | 50 | ns | 8 |
| $t_{RP}$ | $\overline{RAS}$ Precharge Time | 30 | – | 40 | – | ns | |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 50 | 10,000 | 60 | 10,000 | ns | |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Hyper Page Mode) | 50 | 100,000 | 60 | 100,000 | ns | |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time | 8 | – | 10 | – | ns | |
| $t_{RHCP}$ | $\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Hyper Page Mode) | 28 | – | 35 | – | ns | |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time | 35 | | 40 | | ns | |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 8 | 10,000 | 10 | 10,000 | ns | |
| $t_{RCD}$ | $\overline{RAS}$-to-$\overline{CAS}$ Delay Time | 12 | 36 | 14 | 43 | ns | 14 |
| $t_{RAD}$ | $\overline{RAS}$-to-Column-Address Delay Time | 10 | 25 | 12 | 30 | ns | 15 |
| $t_{CRP}$ | $\overline{CAS}$-to-$\overline{RAS}$ Precharge Time | 5 | – | 5 | – | ns | |
| $t_{CP}$ | $\overline{CAS}$ Precharge Time | 8 | – | 10 | – | ns | |
| $t_{ASR}$ | Row Address Set up Time | 0 | – | 0 | – | ns | |
| $t_{RAH}$ | Row Address Hold Time | 8 | – | 10 | – | ns | |
| $t_{ASC}$ | Column Address Set up Time | 0 | – | 0 | – | ns | |
| $t_{CAH}$ | Column Address Hold Time | 8 | – | 10 | – | ns | |
| $t_{RAL}$ | Column-Address-to-$\overline{RAS}$ Lead Time | 25 | – | 30 | – | ns | |
| $t_{RCS}$ | Read Command Set up Time Referenced to $\overline{RAS}$ | 0 | – | 0 | – | ns | |
| $t_{RCH}$ | Read Command Hold Time | 0 | – | 0 | – | ns | 11 |
| $t_{RRH}$ | Read Command Hold Time Referenced to $\overline{RAS}$ | 0 | – | 0 | – | ns | 11 |
| $t_{WCH}$ | Write Command Hold Time | 8 | – | 10 | – | ns | |

## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

| SYMBOL | PARAMETER | TC51V18165CJ/CFT | | | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| | | -50 | | -60 | | | |
| | | MIN | MAX | MIN | MAX | | |
| $t_{WP}$ | Write Command Pulse Width | 8 | – | 10 | – | ns | |
| $t_{RWL}$ | Write-Command-to-$\overline{RAS}$ Lead Time | 8 | – | 10 | – | ns | |
| $t_{CWL}$ | Write-Command-to-$\overline{CAS}$ Lead Time | 8 | – | 10 | – | ns | |
| $t_{DS}$ | Data Set up Time | 0 | – | 0 | – | ns | 12 |
| $t_{DH}$ | Data Hold Time | 8 | – | 10 | – | ns | 12 |
| $t_{REF}$ | Refresh Period | – | 16 | – | 16 | ms | |
| $t_{WCS}$ | Write Command Set up Time | 0 | – | 0 | – | ns | 13 |
| $t_{CWD}$ | $\overline{CAS}$-to-$\overline{WE}$ Delay Time | 31 | – | 36 | – | ns | 13 |
| $t_{RWD}$ | $\overline{RAS}$-to-$\overline{WE}$ Delay Time | 67 | – | 79 | – | ns | 13 |
| $t_{AWD}$ | Column-Address-to-$\overline{WE}$ Delay Time | 42 | – | 49 | – | ns | 13 |
| $t_{CPWD}$ | $\overline{CAS}$-Precharge-to-$\overline{WE}$ Delay Time | 45 | – | 54 | – | ns | 13 |
| $t_{CSR}$ | $\overline{CAS}$ Set up Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle) | 5 | – | 5 | – | ns | |
| $t_{CHR}$ | $\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle) | 8 | – | 10 | – | ns | |
| $t_{RPC}$ | $\overline{RAS}$-to-$\overline{CAS}$ Precharge Time | 5 | – | 5 | – | ns | |
| $t_{CPT}$ | $\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle) | 20 | – | 20 | – | ns | |
| $t_{ROH}$ | $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | 8 | – | 10 | – | ns | |
| $t_{OEA}$ | $\overline{OE}$ Access Time | – | 13 | – | 15 | ns | 9 |
| $t_{OED}$ | $\overline{OE}$-to-Data Delay | 13 | – | 15 | – | ns | |
| $t_{OLZ}$ | $\overline{OE}$ to Output in Low-Z | 0 | – | 0 | – | ns | |
| $t_{OEZ}$ | Output Buffer Turn-off Delay Time from $\overline{OE}$ | 0 | 13 | 0 | 15 | ns | 10 |
| $t_{OEH}$ | $\overline{OE}$ Command Hold Time | 8 | – | 10 | – | ns | |
| $t_{ODS}$ | Output Disable Set up Time | 0 | – | 0 | – | ns | |

## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

| SYMBOL | PARAMETER | TC51V18165CJ/CFT | | | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| | | -50 | | -60 | | | |
| | | MIN | MAX | MIN | MAX | | |
| $t_{RNCD}$ | $\overline{RAS}$ to next $\overline{CAS}$ Delay Time (Hyper Page Mode) | 50 | – | 60 | – | ns | |
| $t_{HPC}$ | Hyper Page Mode Cycle Time | 20 | – | 25 | – | ns | |
| $t_{HPRWC}$ | Hyper Page Mode Read-Modify-Write Cycle Time | 57 | – | 68 | – | ns | |
| $t_{COH}$ | Output Data Hold time | 5 | – | 5 | – | ns | |
| $t_{REZ}$ | Output Buffer Turn-off Delay from $\overline{RAS}$ | 0 | 13 | 0 | 15 | ns | 10,16 |
| $t_{WEZ}$ | Output Buffer Turn-off Delay from $\overline{WE}$ | 0 | 13 | 0 | 15 | ns | 10 |
| $t_{WED}$ | $\overline{WE}$-to-Data Delay | 13 | – | 15 | – | ns | |
| $t_{OE}$ | $\overline{OE}$ Pulse Width | 13 | – | 15 | – | ns | |
| $t_{OEP}$ | $\overline{OE}$ Precharge Time | 8 | – | 10 | – | ns | |
| $t_{CPO}$ | $\overline{CAS}$ to $\overline{OE}$ Precharge Time | 5 | – | 5 | – | ns | |
| $t_{OCH}$ | $\overline{CAS}$ Hold Time Referenced to $\overline{OE}$ | 8 | – | 10 | – | ns | |

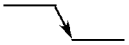
## CAPACITANCE ($V_{CC}$ = 3.3 V ± 0.3 V, f = 1 MHz, Ta = 0° to 70°C)

| SYMBOL | CHARACTERISTIC | MIN | MAX | UNIT |
|---|---|---|---|---|
| $C_{I1}$ | Input Capacitance (A0 to A9) | – | 5 | pF |
| $C_{I2}$ | Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$) | – | 7 | pF |
| $C_O$ | I/O Capacitance (I/O1 to I/O16) | – | 7 | pF |

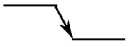
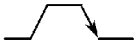
NOTES:

1. Conditions outside the limits listed under "Absolute Maximum Rating" may cause permanent damage to the device.
2. All voltages are referenced to $V_{SS}$.
3. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, $I_{CC6}$ depend on cycle rate.
4. $I_{CC1}$, $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once at most while $\overline{RAS}$ = $V_{IL}$. In case of $I_{CC4}$, it can be changed once at most during a Hyper Page mode cycle ($t_{HPC}$).
6. An initial pause of 200 $\mu$s is required after power-up followed by 8 $\overline{RAS}$-Only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$-Only refresh cycles are required.
7. AC measurements assume $t_T$ = 2 ns.
8. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
9. This is measured with a load equivalent to 1 TTL load and 100 pF at $V_{OH}$ = 2.0 V ($I_{OUT}$ = −2 mA), $V_{OL}$ = 0.8 V ($I_{OUT}$ = 2 mA).
10. $t_{OFF}$ (max), $t_{OEZ}$ (max), $t_{REZ}$ (max) and $t_{WEZ}$ (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a Read cycle.
12. These parameters are referenced to $\overline{UCAS}$, $\overline{LCAS}$ leading edge of $\overline{CAS}$ in Early Write cycles and to leading edge of $\overline{WE}$ in Read-Modify-Write cycles.
13. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an Early Write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met.
    $t_{RCD}$ (max) is specified as a reference point only: If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is determined by $t_{CAC}$.
15. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met.
    $t_{RAD}$ (max) is specified as a reference point only: If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is determined by $t_{AA}$.
16. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going ($t_{OFF}$). If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achived by $\overline{RAS}$ high going ($t_{REZ}$).

DATA-OUT LO-Z CONTROL LOGIC

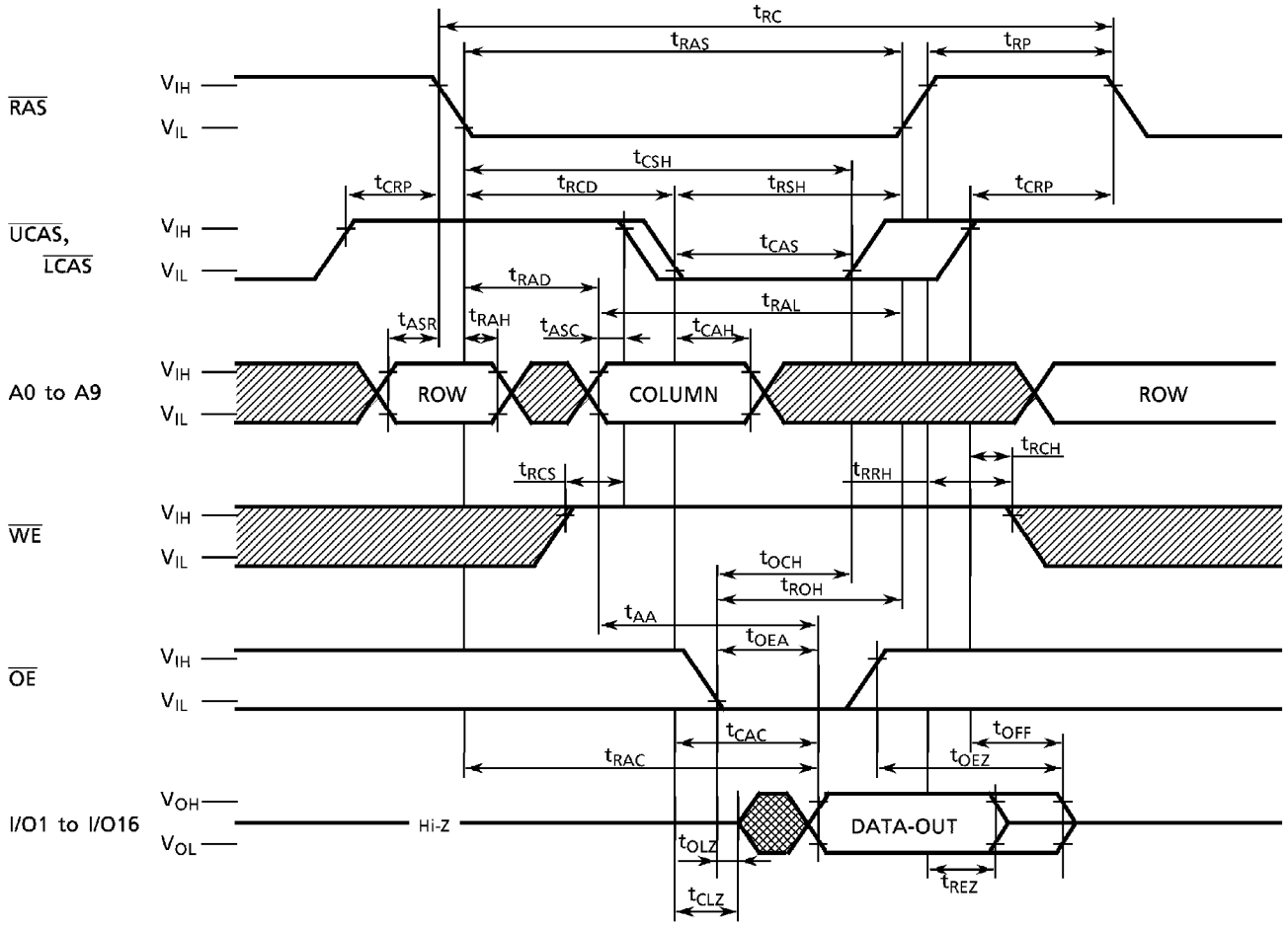
| $\overline{RAS}$ | $\overline{CAS}$ | $\overline{OE}$ | $\overline{WE}$ | Timing Specification |
|---|---|---|---|---|
| H |  | L | H | $t_{OFF}$ |
|  | H | L | H | $t_{REZ}$ |
| L | L |  | H | $t_{OEZ}$ |
| L | H | L |  | $t_{WEZ}$ |

DATA-OUT LO-Z CONTROL LOGIC

| $\overline{RAS}$ | $\overline{CAS}$ | $\overline{OE}$ | $\overline{WE}$ | Timing Specification |
|---|---|---|---|---|
| L |  | L | H | $t_{CLZ}$ |
| L | L |  | H | $t_{OLZ}$ |
| L | L |  | H | $t_{OLZ}$ |

## TIMING DIAGRAMS

### READ CYCLE

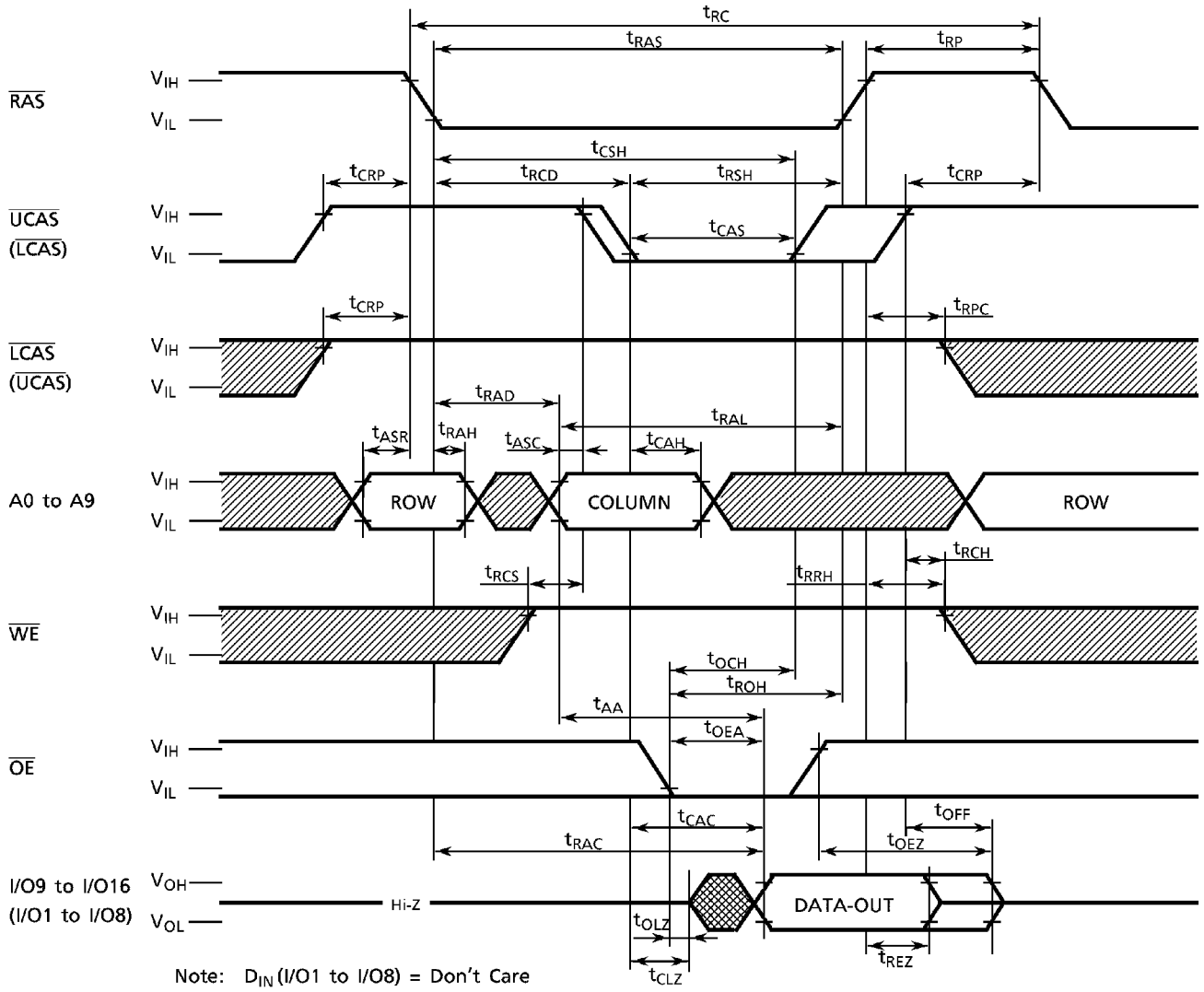



Note: $D_{IN}$ = Hi-Z

: H or L

: Invalid Data

## BYTE READ CYCLE

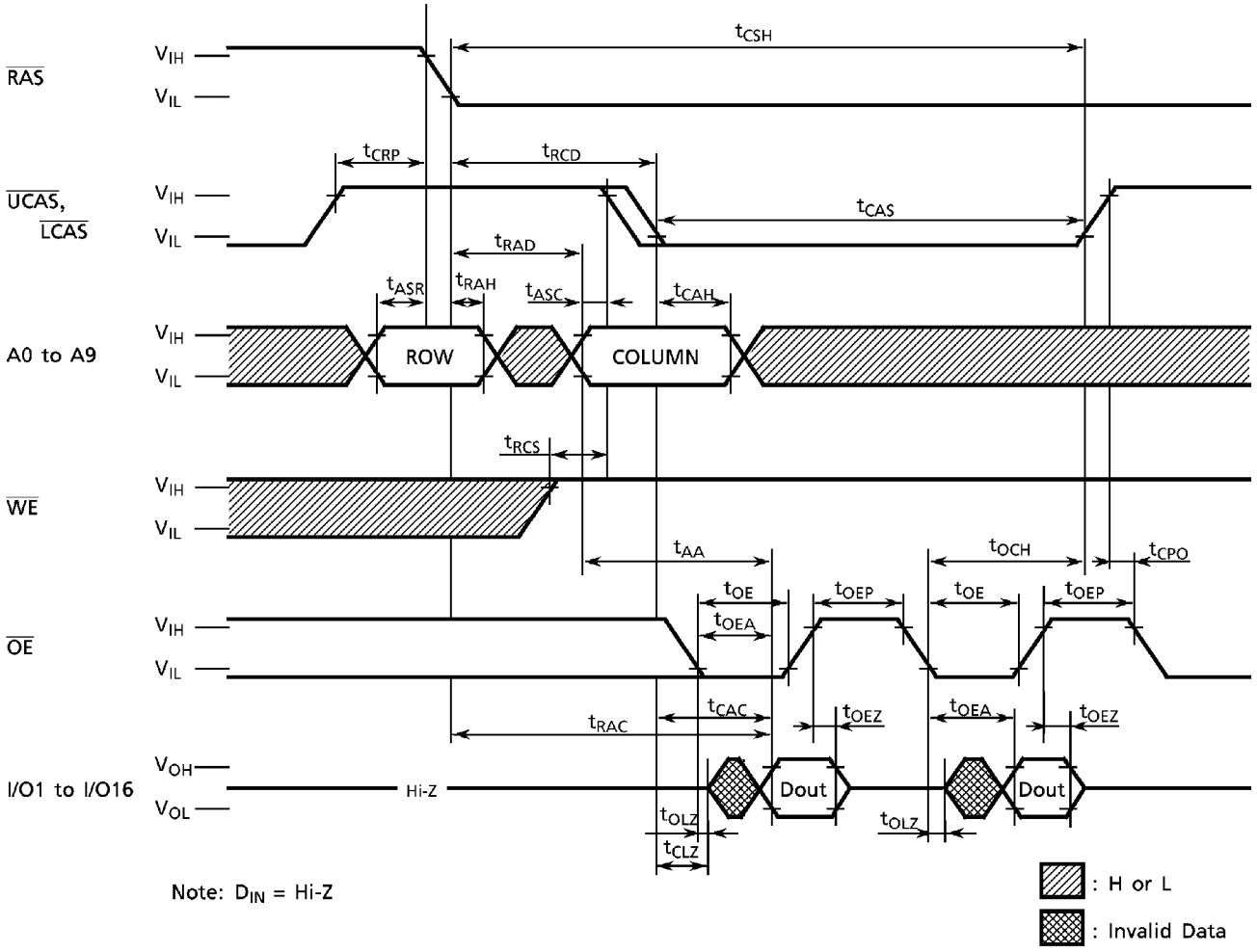



Note: $D_{IN}$ (I/O1 to I/O8) = Don't Care
$D_{IN}$ (I/O9 to I/O16) = Hi-Z
$D_{OUT}$ (I/O1 to I/O8) = Hi-Z
($D_{IN}$ (I/O9 to I/O16) = Don't Care
$D_{IN}$ (I/O1 to I/O8) = Hi-Z
$D_{OUT}$ (I/O9 to I/O16) = Hi-Z)

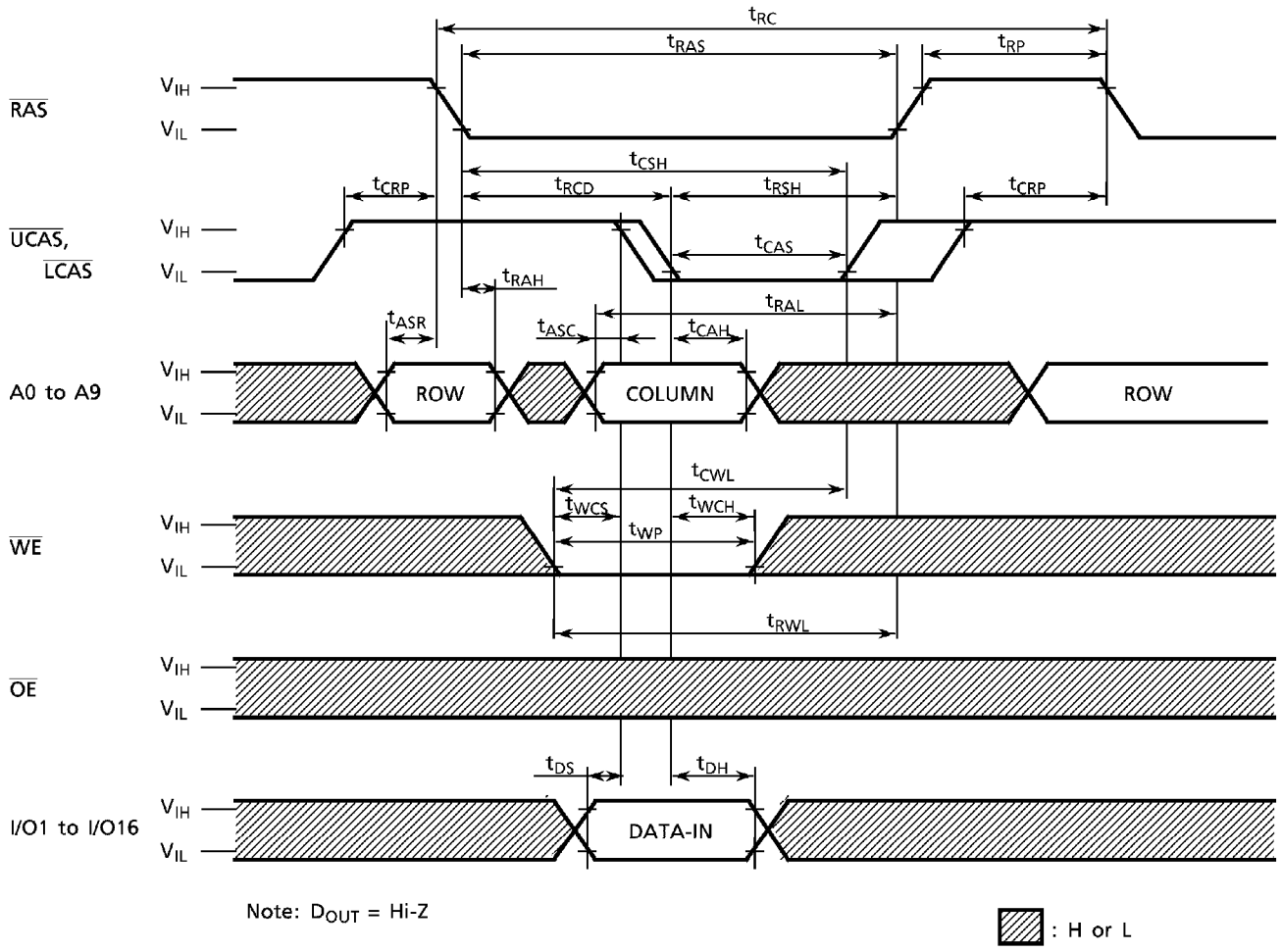
: H or L

: Invalid Data

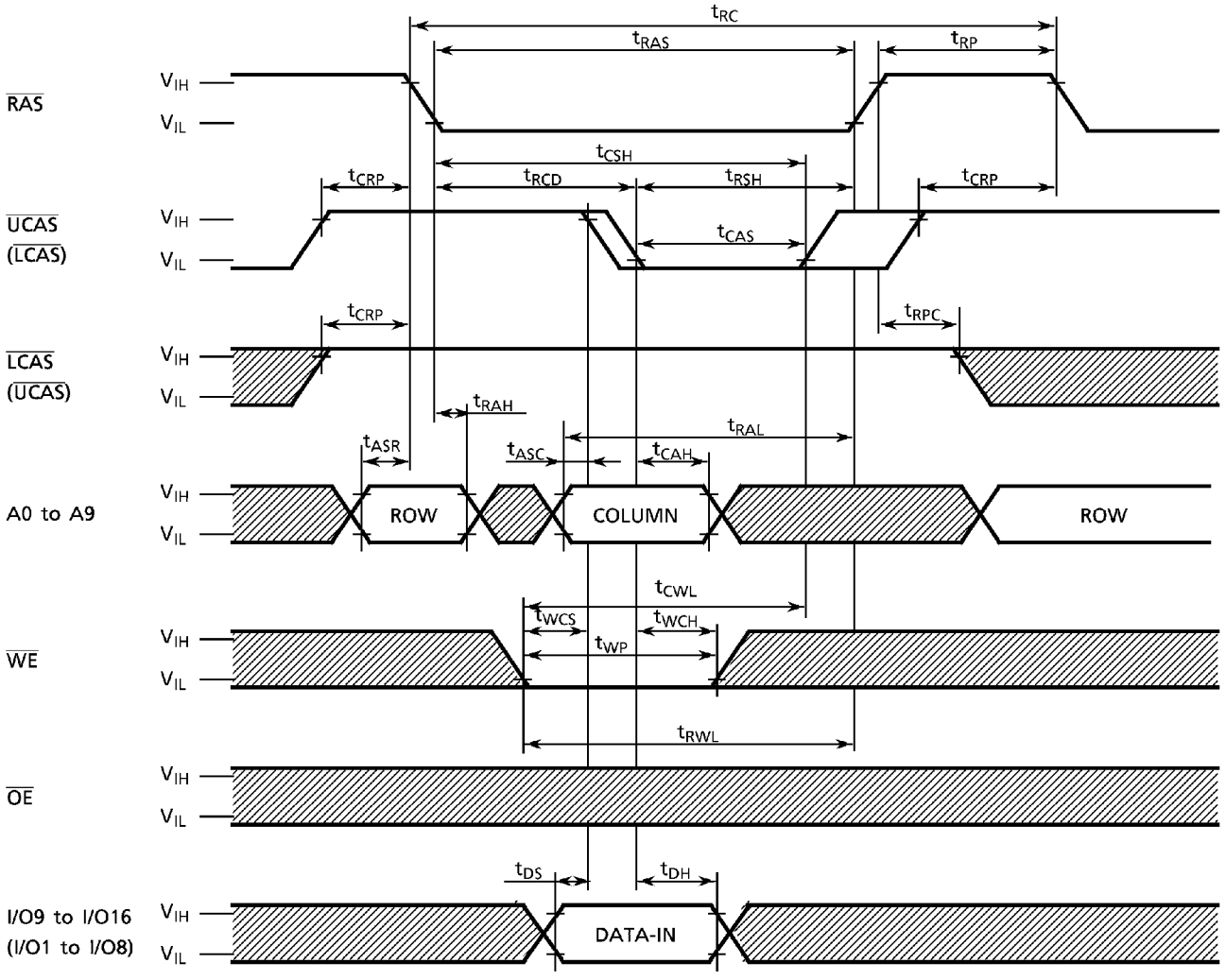
## $\overline{OE}$-CONTROLLED READ CYCLE



WRITE CYCLE (EARLY WRITE)



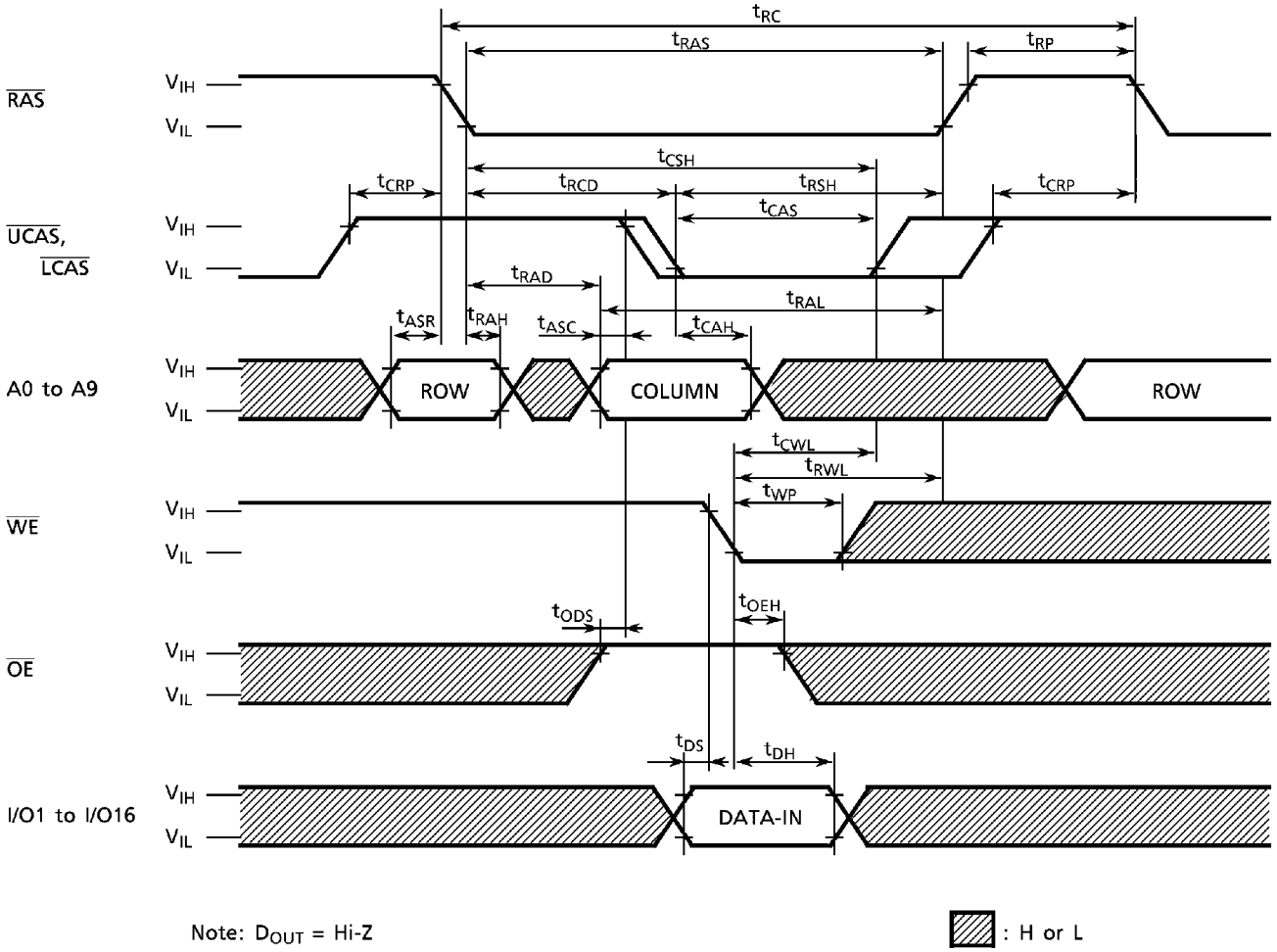
## BYTE WRITE CYCLE (EARLY WRITE)




Note: $D_{IN}$ (I/O1 to I/O8) = Don't Care
($D_{IN}$ (I/O9 to I/O16) = Don't Care)
$D_{OUT}$ = Hi-Z

▨ : H or L

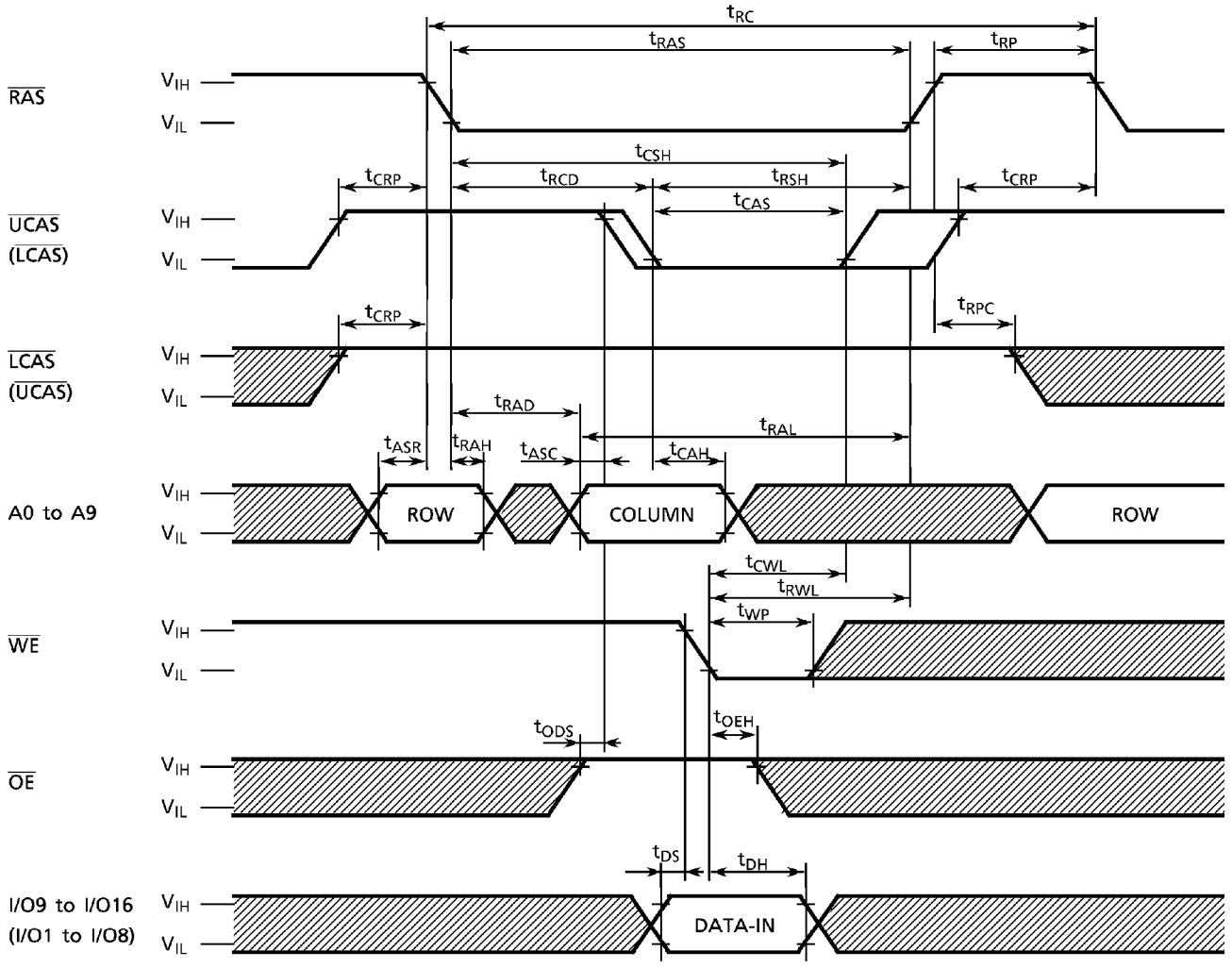
## $\overline{OE}$-CONTROLLED WRITE CYCLE




Note: $D_{OUT}$ = Hi-Z

▨ : H or L

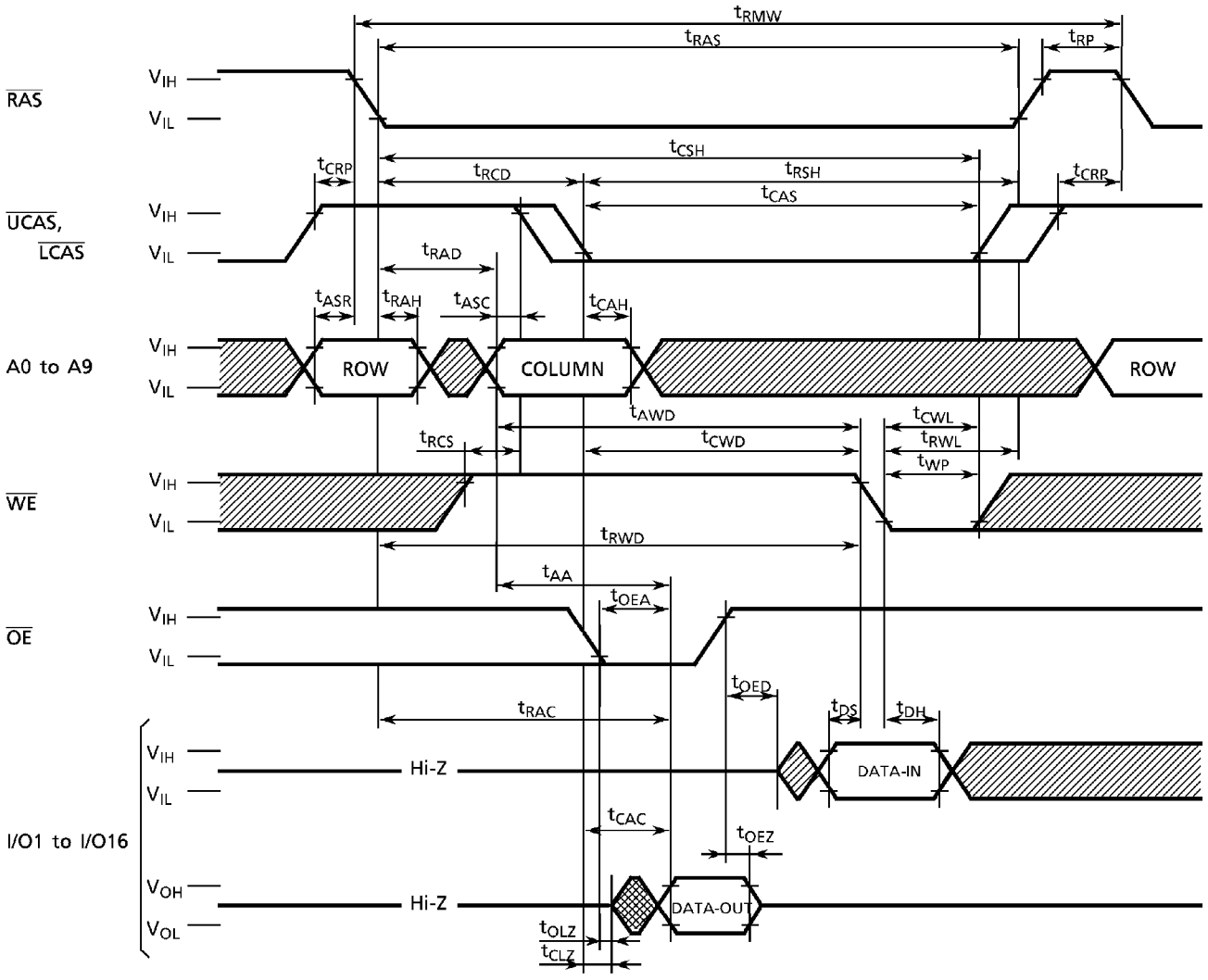
## $\overline{OE}$-CONTROLLED BYTE WRITE CYCLE



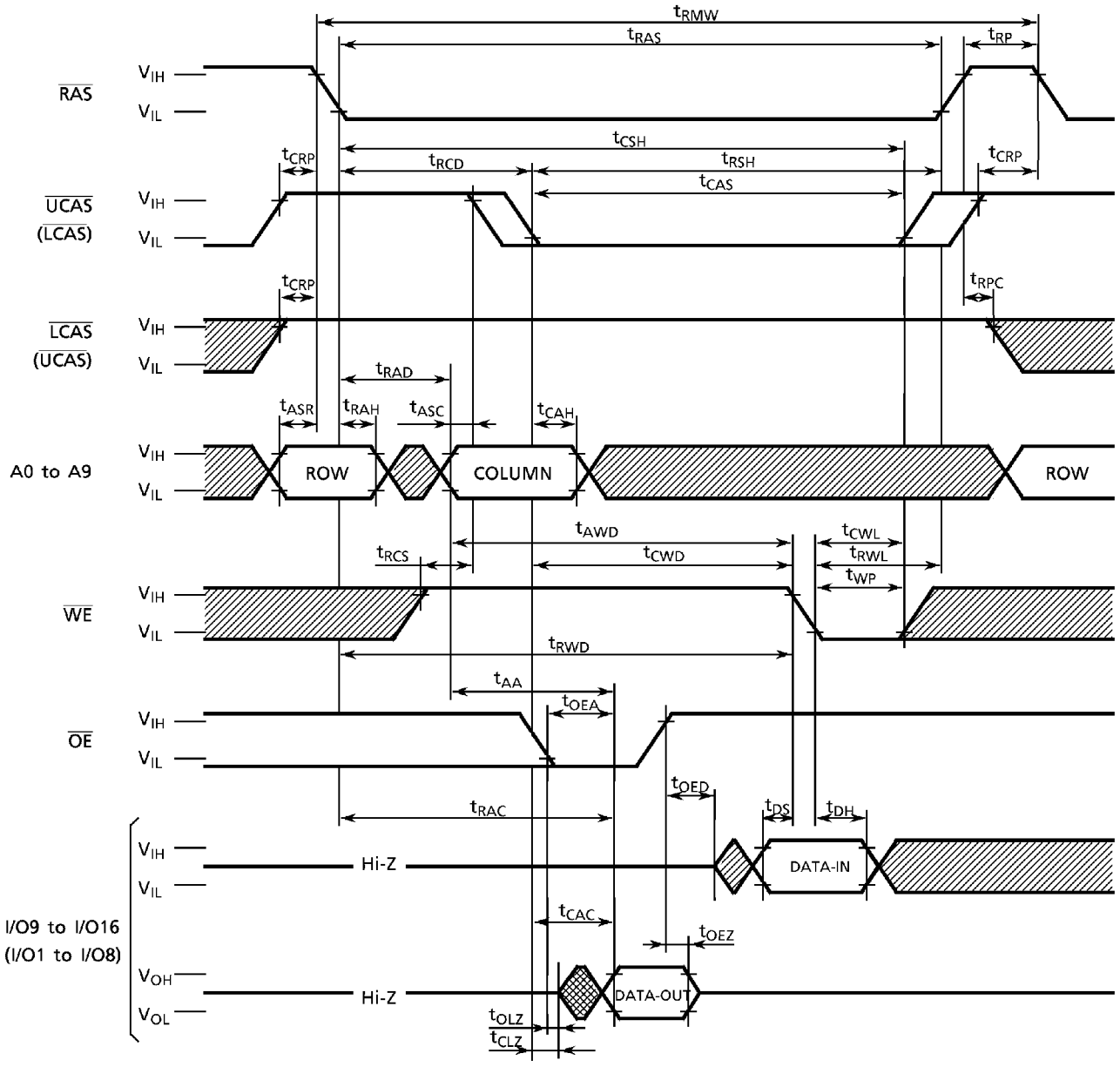

Note: $D_{IN}$ (I/O1 to I/O8) = Don't Care
($D_{IN}$ (I/O9 to I/O16) = Don't Care)
$D_{OUT}$ = Hi-Z

: H or L

READ-MODIFY-WRITE CYCLE



BYTE READ-MODIFY-WRITE CYCLE

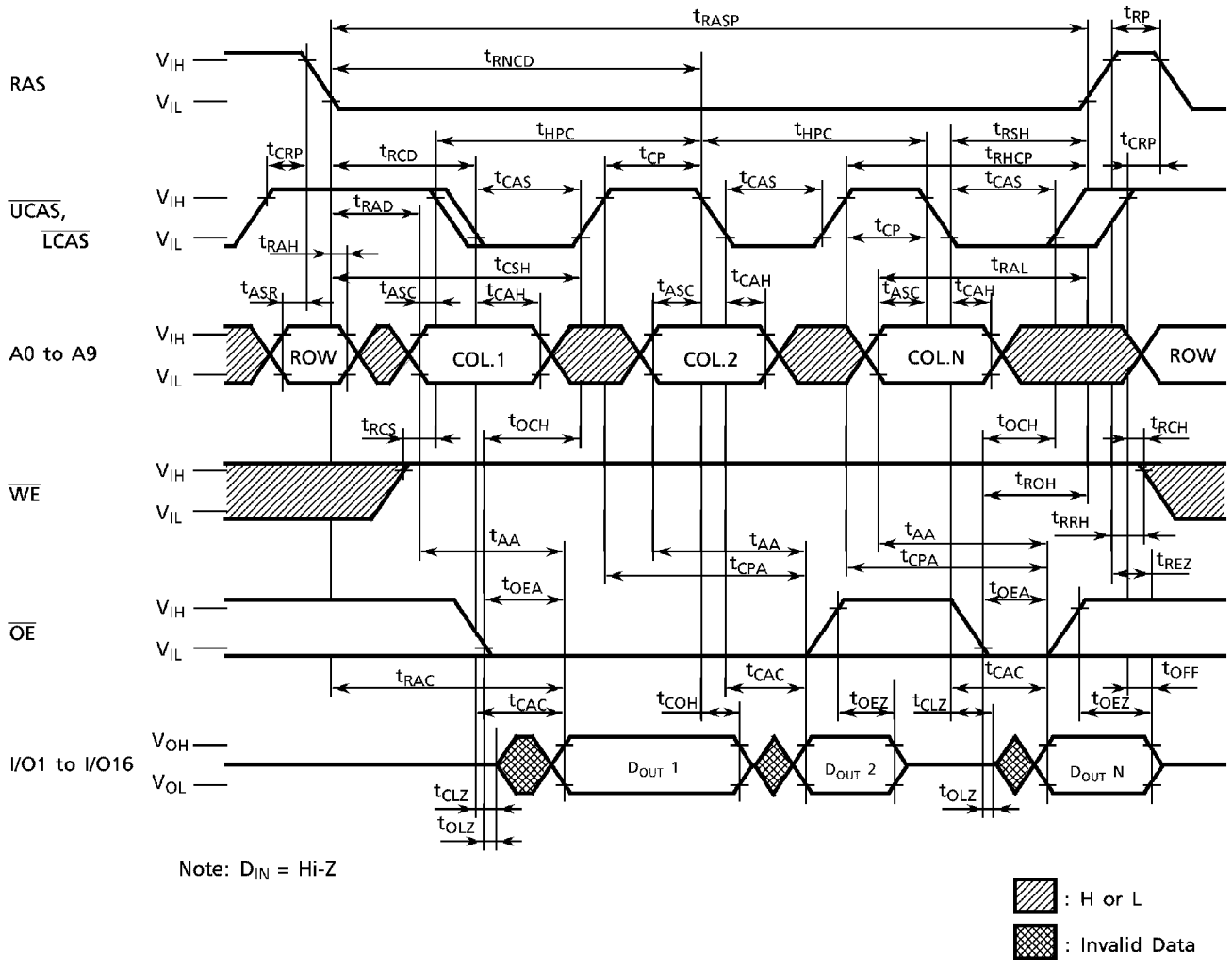



Note: $D_{IN}$ (I/O1 to I/O8) = Don't Care
$D_{OUT}$ (I/O1 to I/O8) = Hi-Z
( $D_{IN}$ (I/O9 to I/O16) = Don't Care
$D_{OUT}$ (I/O9 to I/O16) = Hi-Z )

: H or L

: Invalid Data

## HYPER PAGE MODE READ CYCLE

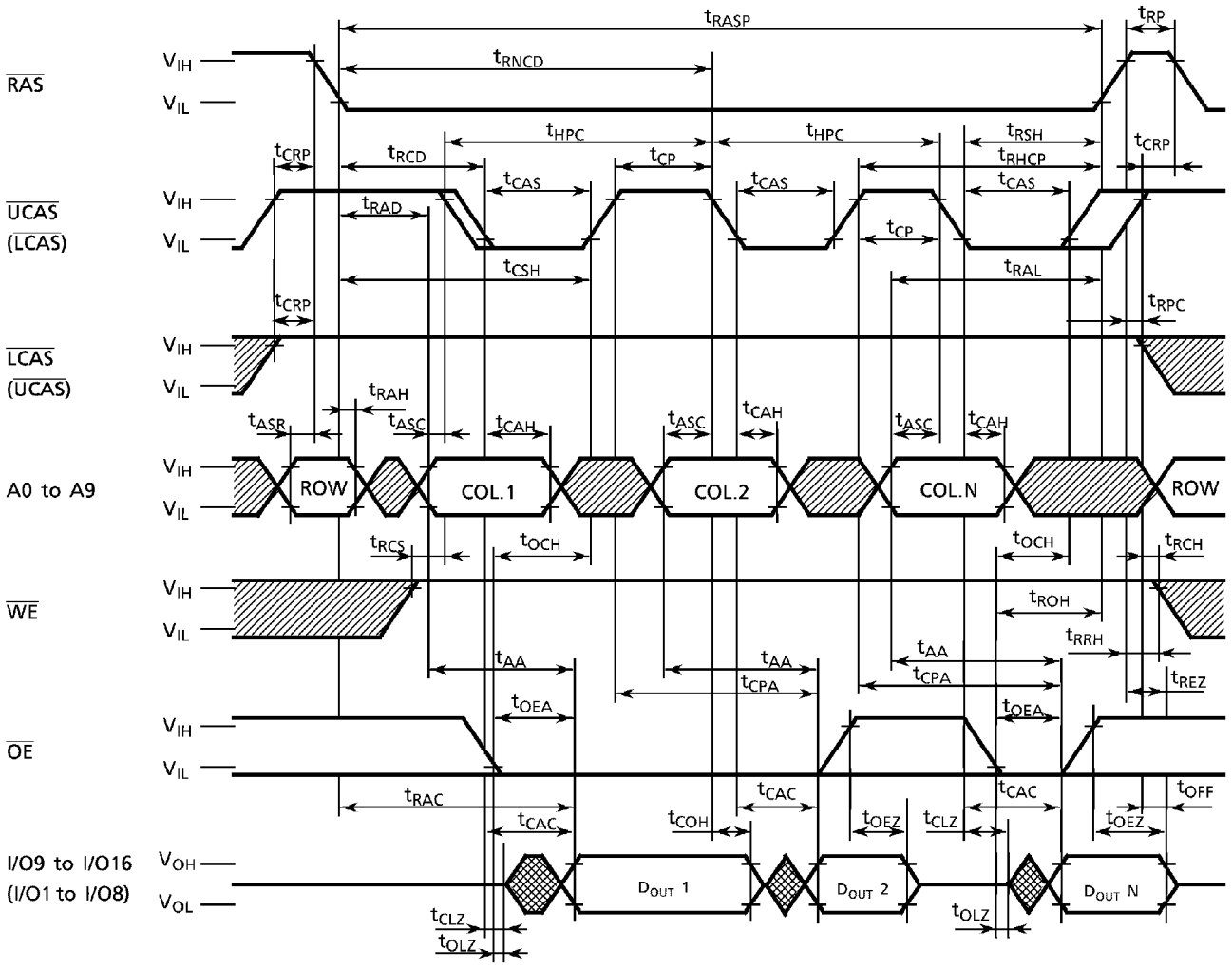



Note: $D_{IN}$ = Hi-Z

: H or L

: Invalid Data

## HYPER PAGE MODE BYTE READ CYCLE

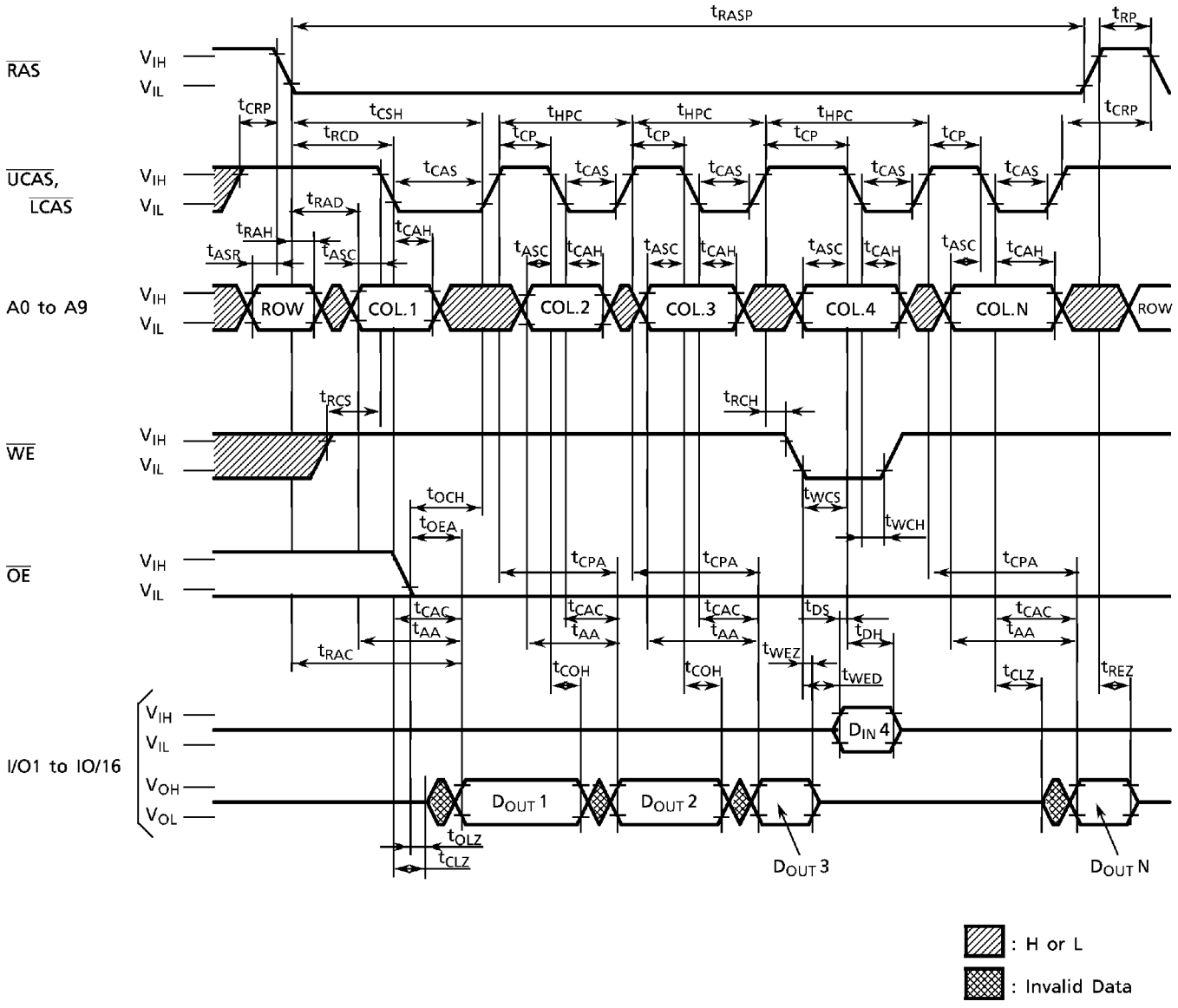



Note : $D_{IN}$ (I/O1 to I/O8) = Don't Care
$D_{OUT}$ (I/O1 to I/O8) = Hi-Z
($D_{IN}$ (I/O9 to I/O16) = Don't Care
$D_{OUT}$ (I/O9 to I/O16) = Hi-Z)

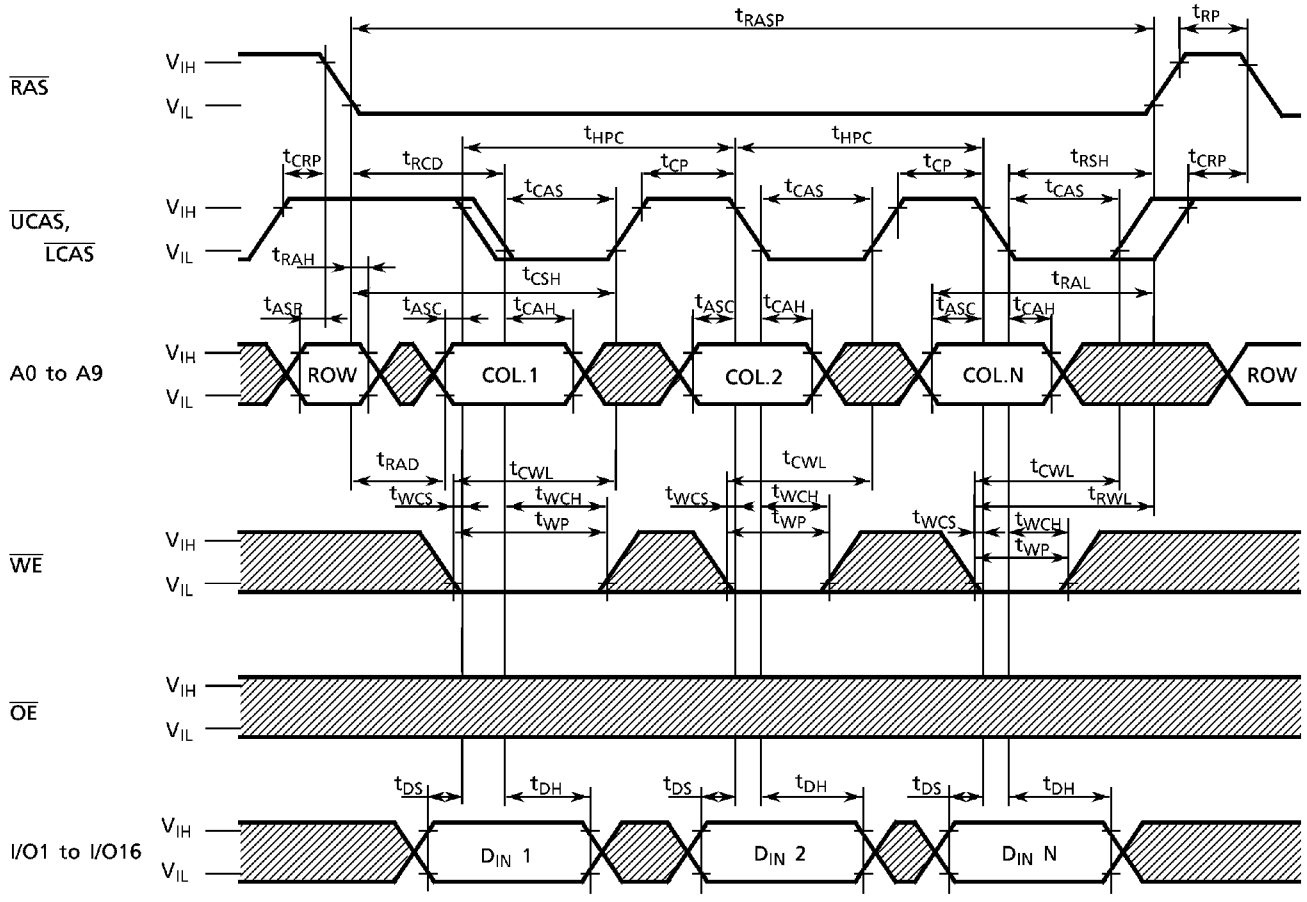
: H or L

: Invalid Data

## HYPER PAGE MODE READ-WRITE MIXED CYCLE



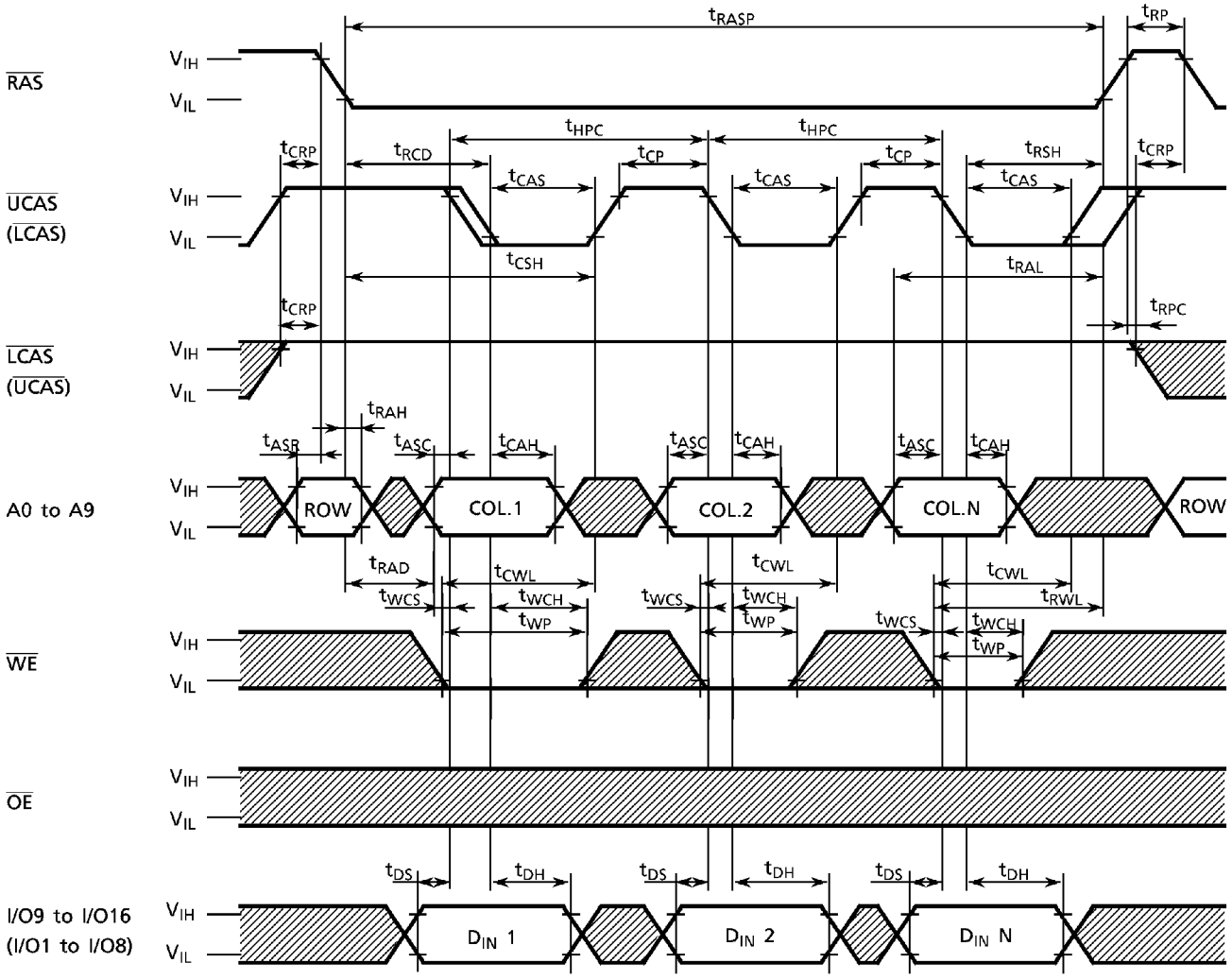
## HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)




Note: $D_{OUT}$ = Hi-Z

▨ : H or L

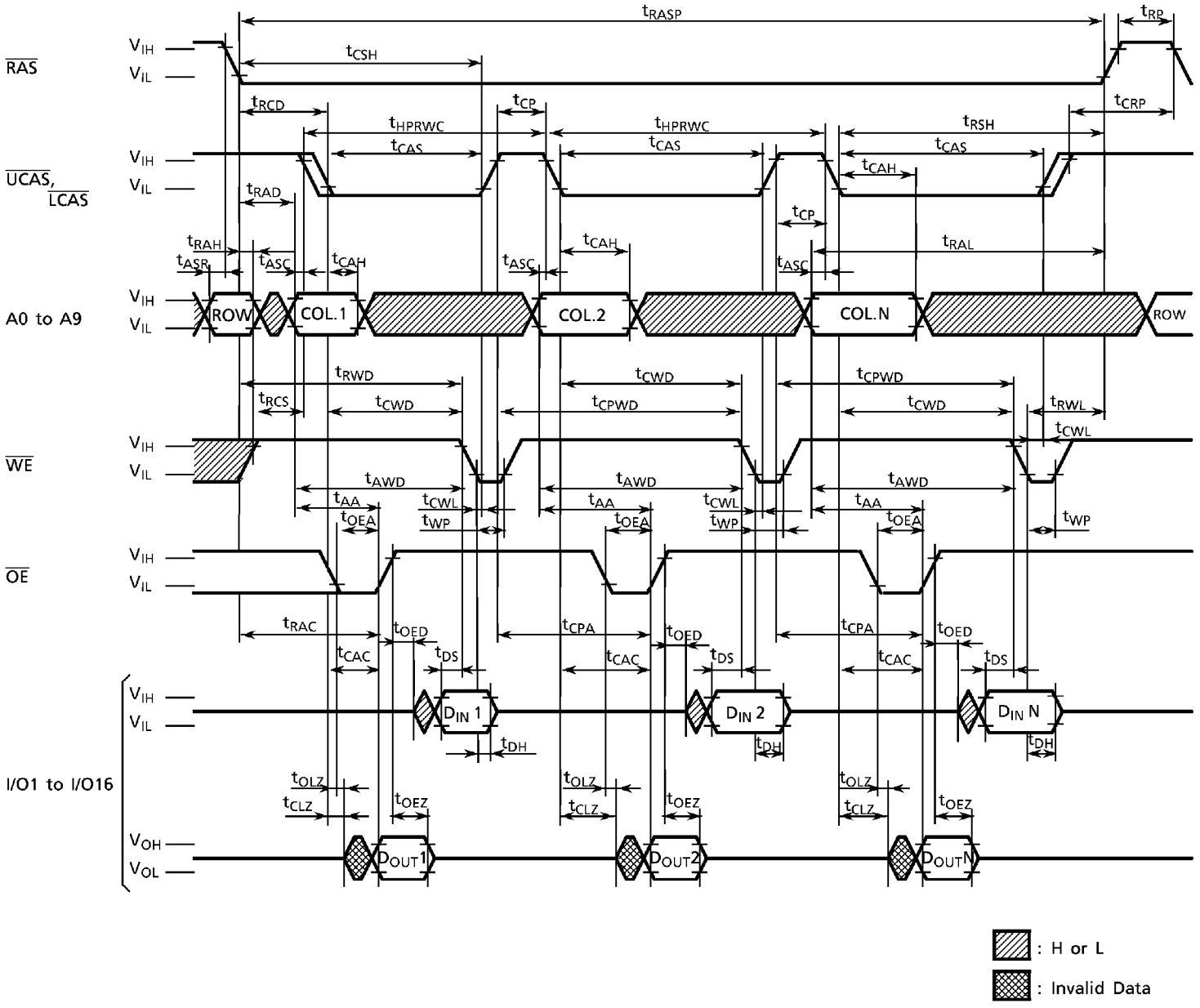
## HYPER PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



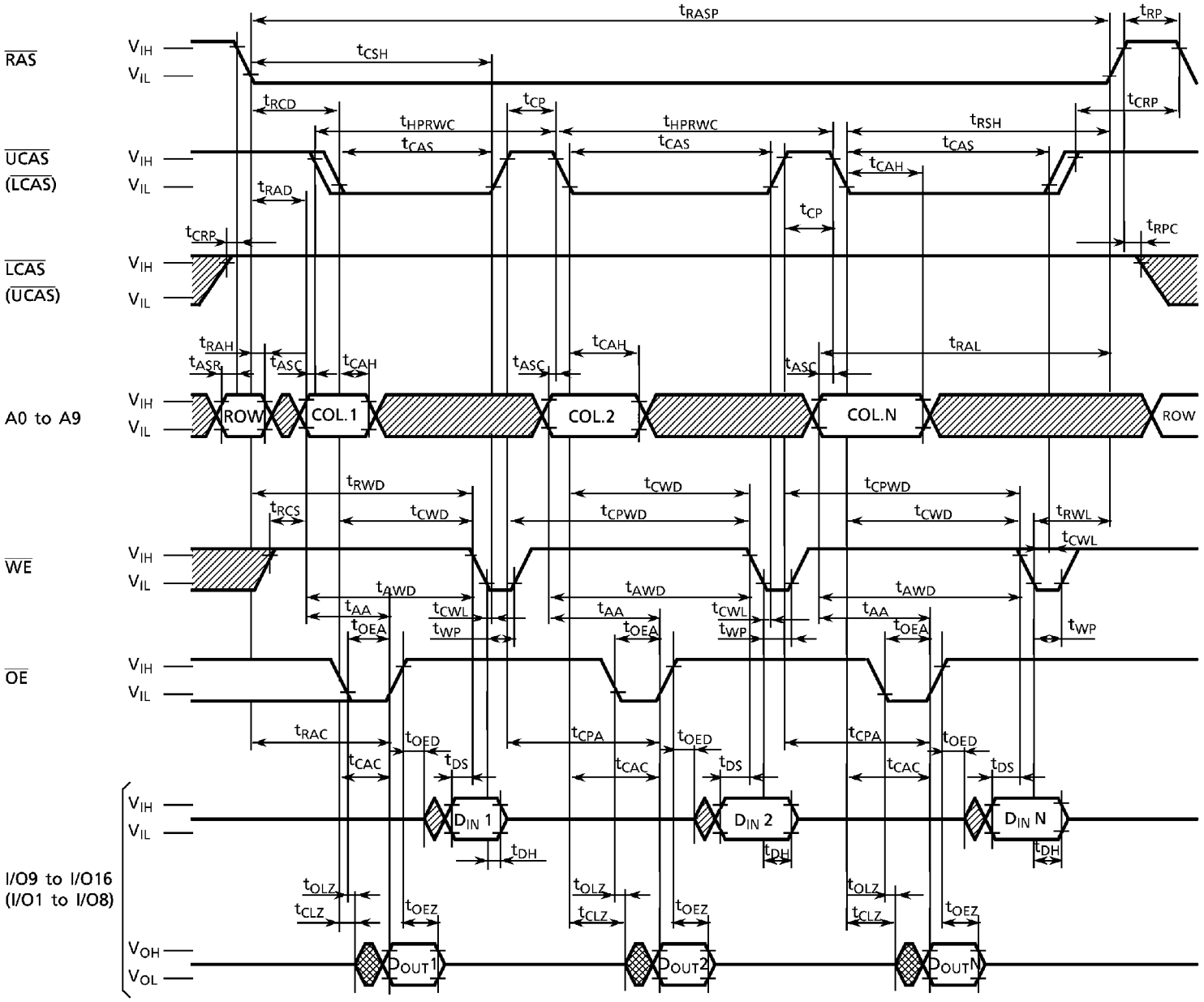

Note : $D_{IN}$ (I/O1 to I/O8) = Don't Care
($D_{IN}$ (I/O9 to I/O16) = Don't Care)
$D_{OUT}$ = Hi-Z

▨ : H or L

## HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



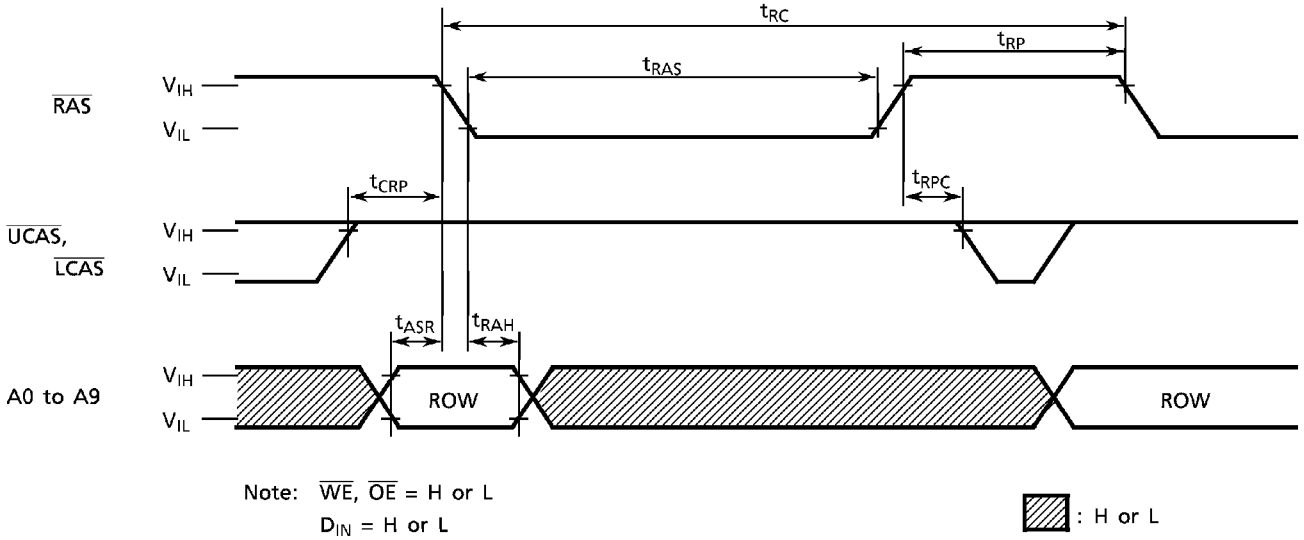
## HYPER PAGE MODE BYTE READ-MODIFY-WRITE CYCLE




Note : $D_{IN}$ (I/O1 to I/O8) = Don't Care
$D_{OUT}$ (I/O1 to I/O8) = Hi-Z
($D_{IN}$ (I/O9 to I/O16) = Don't Care
$D_{OUT}$ (I/O9 to I/O16) = Hi-Z)

: H or L
: Invalid Data

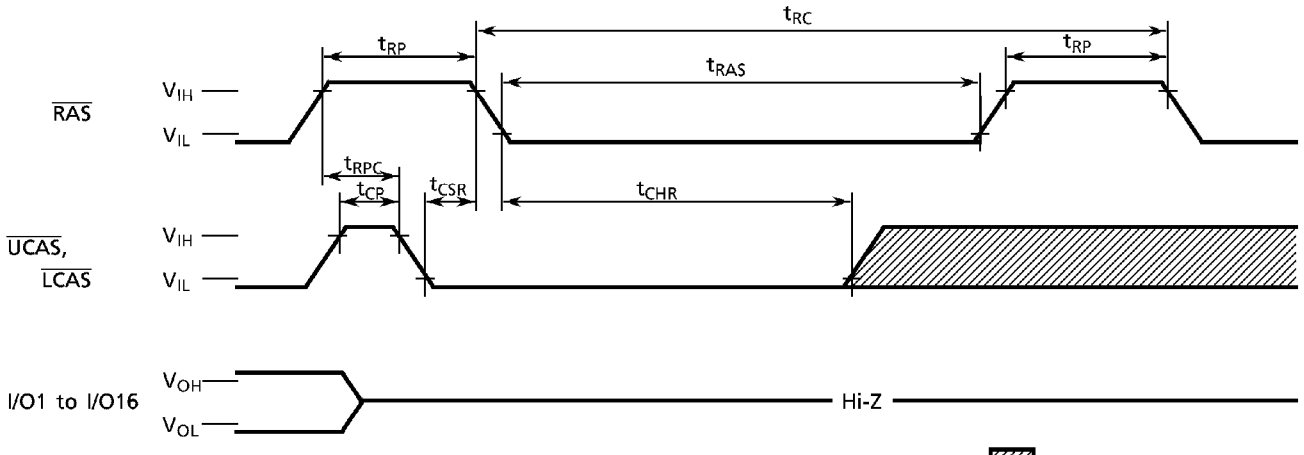
## $\overline{RAS}$-ONLY REFRESH CYCLE




Note: $\overline{WE}$, $\overline{OE}$ = H or L
$D_{IN}$ = H or L

▨ : H or L

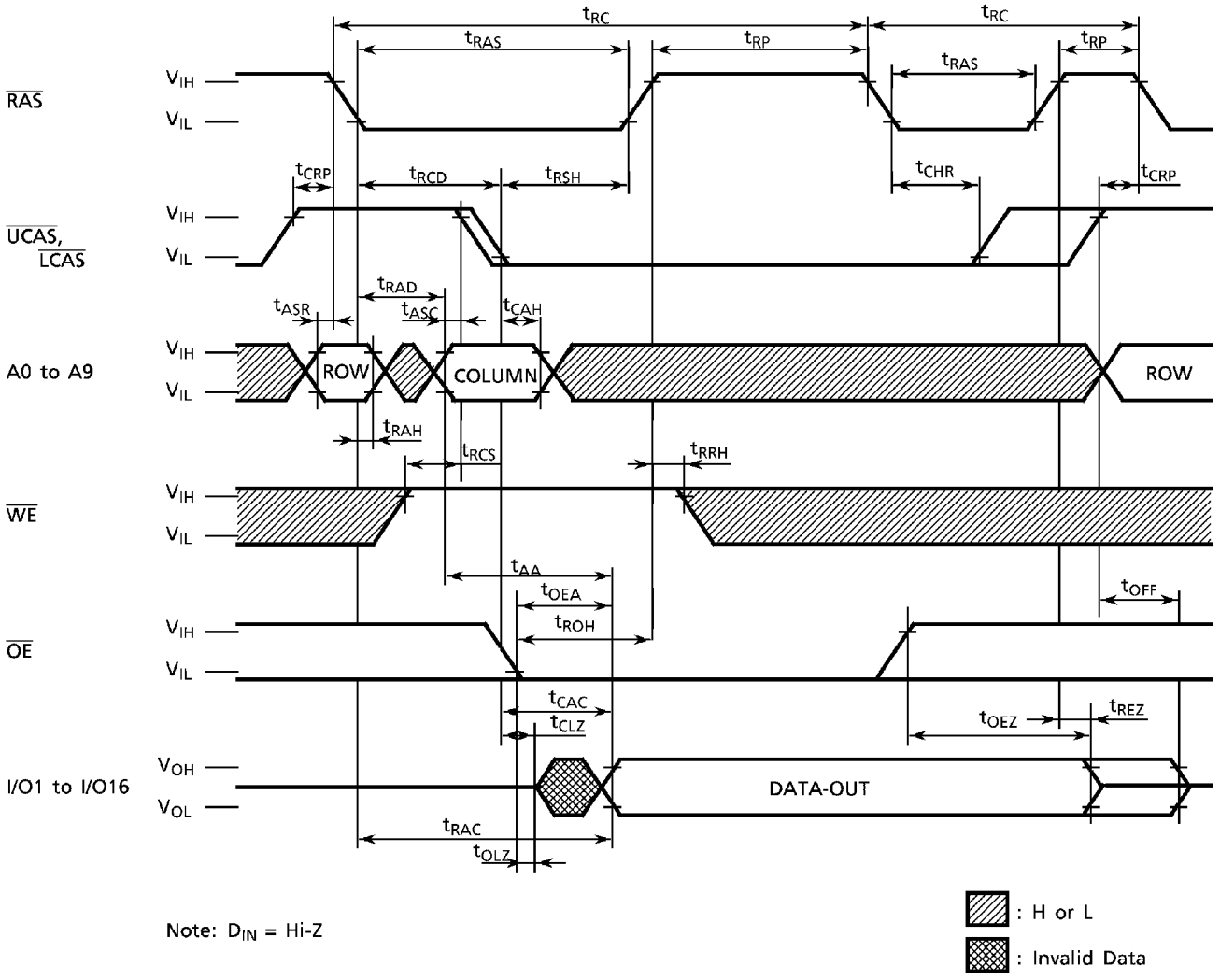
## $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE




▨ : H or L

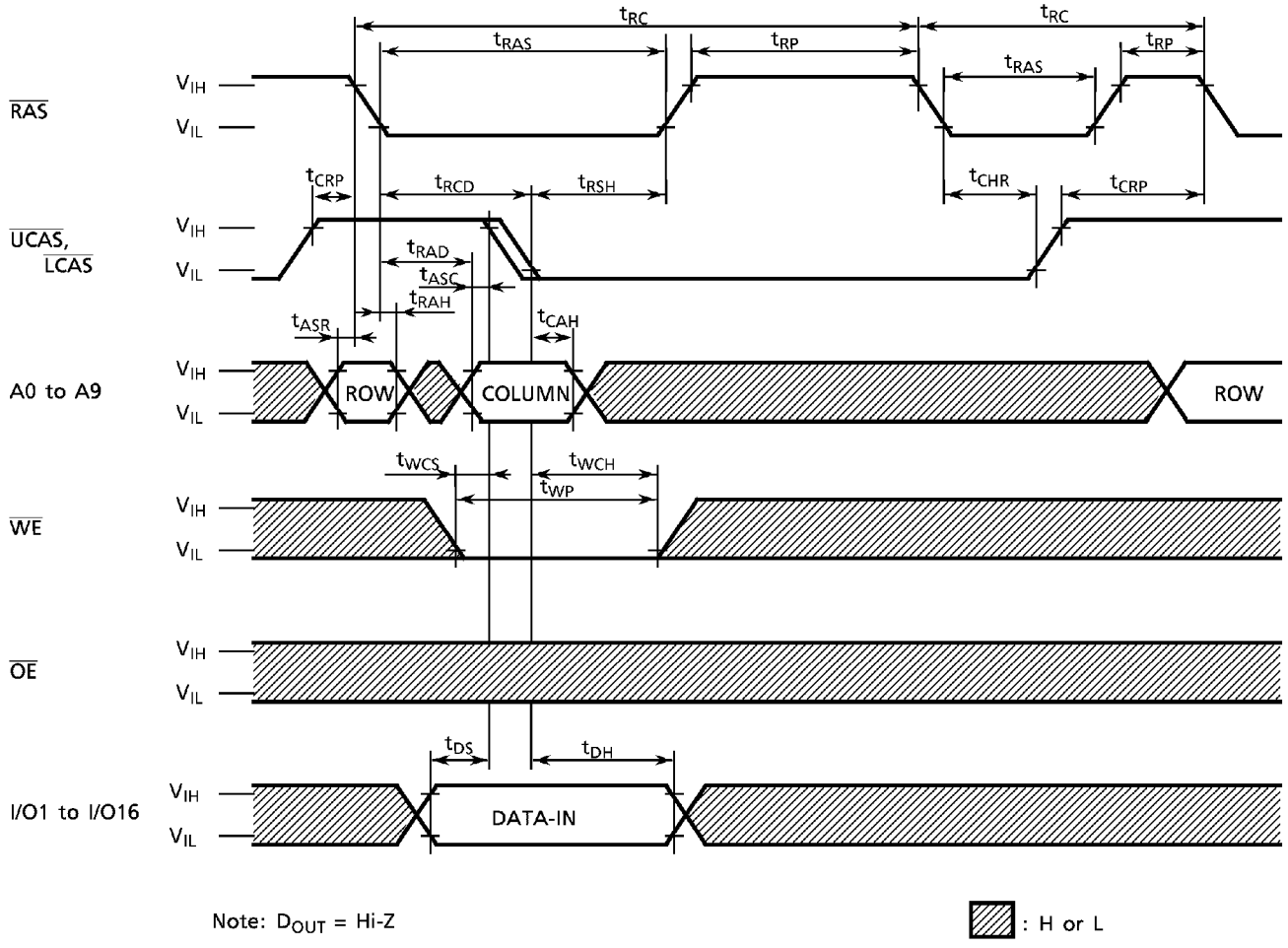
Note: $\overline{WE}$, $\overline{OE}$, A0 to A9 = H or L
$D_{IN}$ = H or L

## HIDDEN REFRESH CYCLE (READ)




Note: $D_{IN}$ = Hi-Z

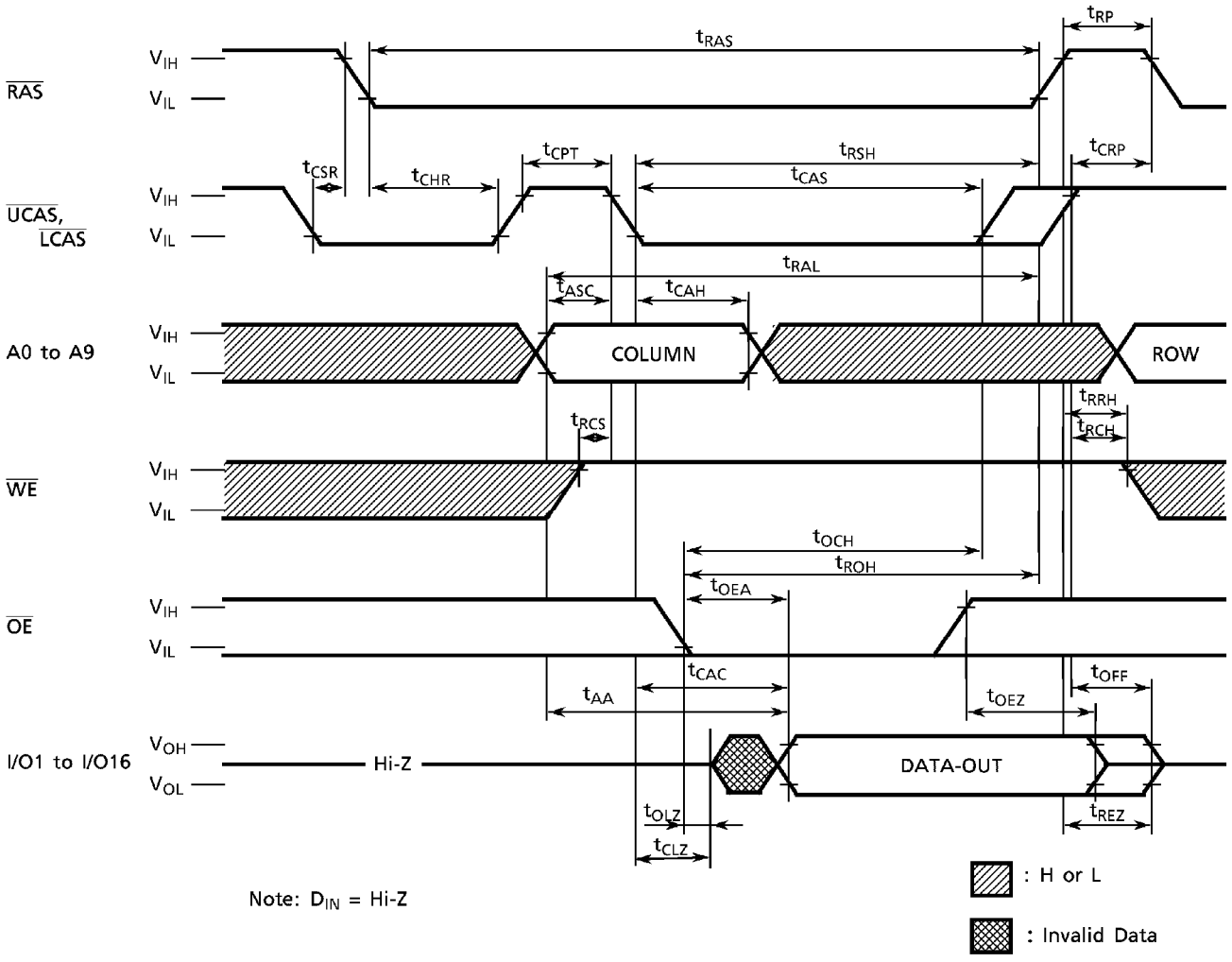
HIDDEN REEFRESH CYCLE (WRITE)




Note: $D_{OUT}$ = Hi-Z

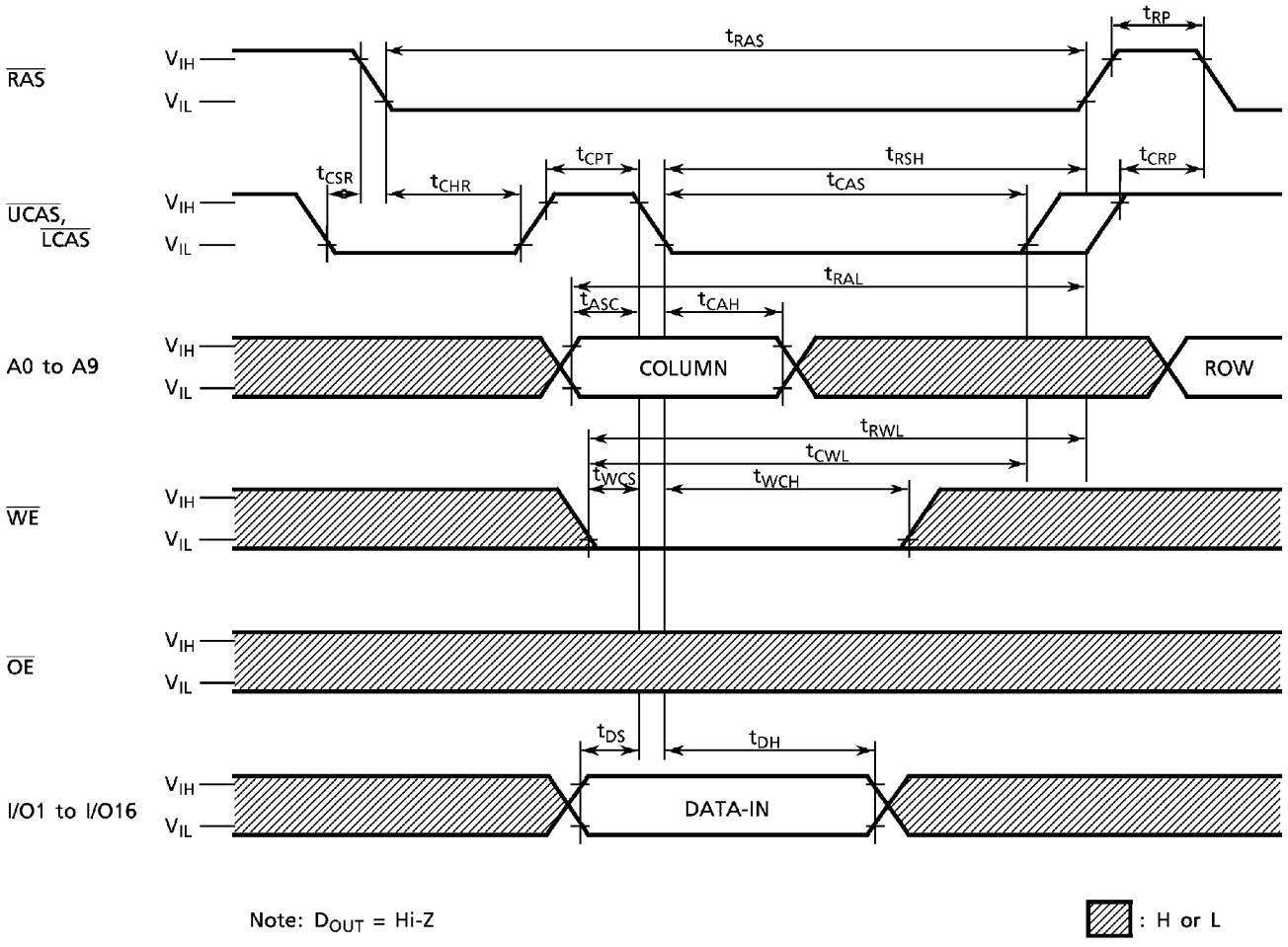
▨ : H or L

## $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH-COUNTER TEST READ CYCLE




Note: $D_{IN}$ = Hi-Z

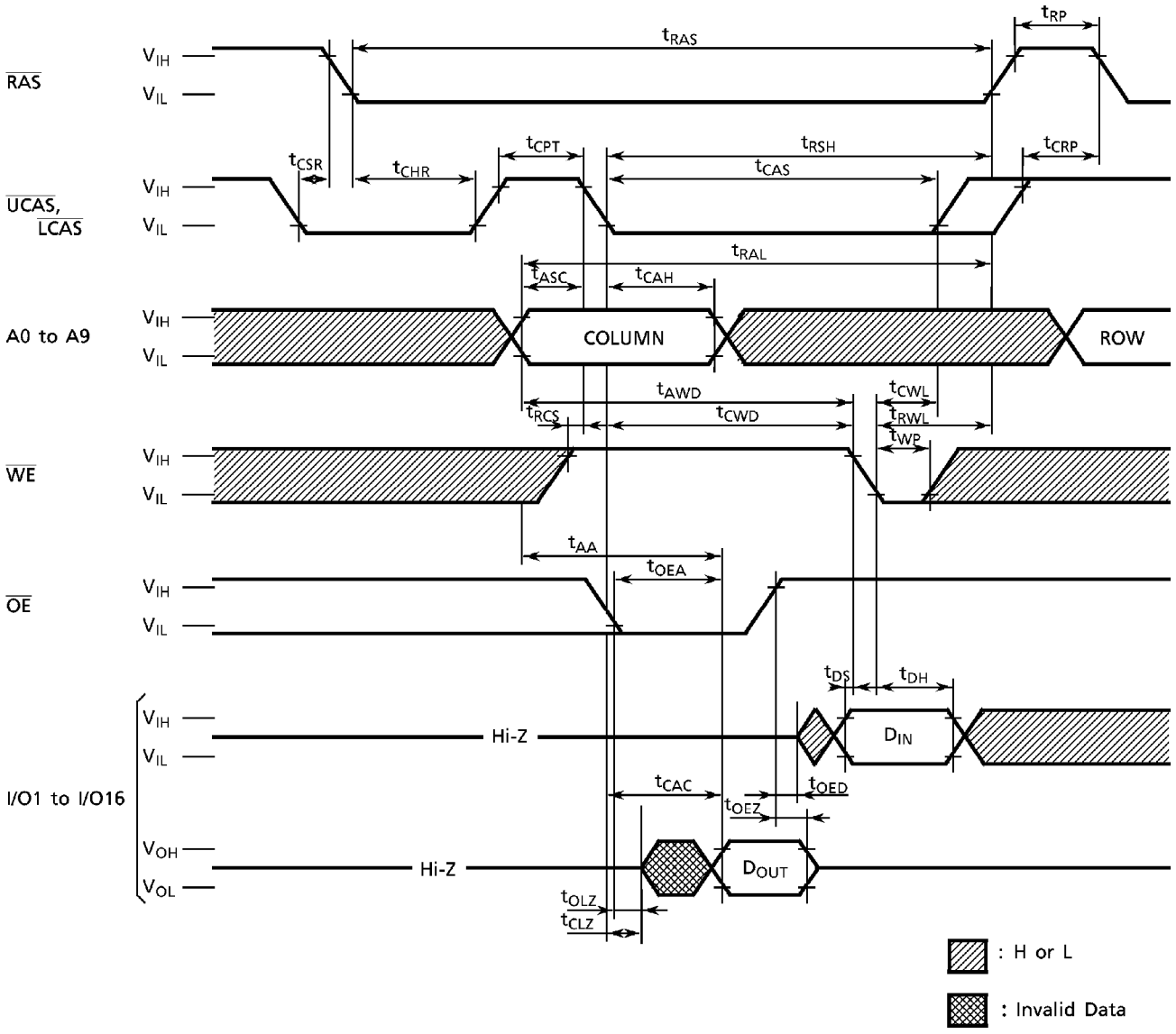
## $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH-COUNTER TEST WRITE CYCLE




Note: $D_{OUT}$ = Hi-Z

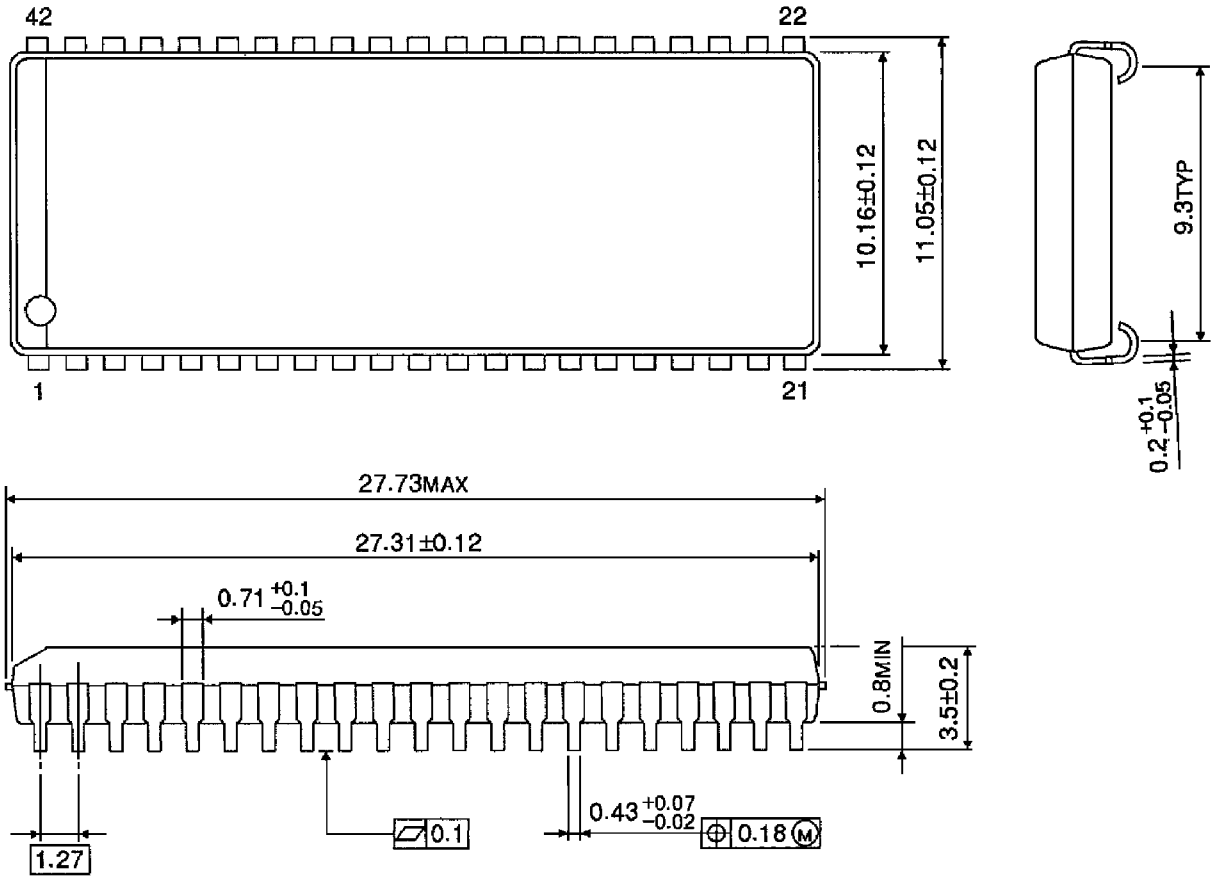
▨ : H or L

## CAS-BEFORE-RAS REFRESH-COUNTER TEST READ-MODIFY-WRITE CYCLE



OUTLINE DRAWING (SOJ42-P-400-1.27)

Unit: mm



OUTLINE DRAWING (TSOPII 50/44-P-400-0.80)

Unit: mm