ECL 10KH High-Speed Emitter-Coupled Logic Family
MC10H016
4-Bit Binary Counter

Features/Benefits

- Counting frequency, 200 MHz min.
- Power dissipation 570 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

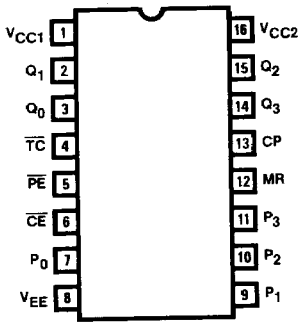
The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit Binary Counter. This device is a member of Monolithic Memories' new ECL 10KH family. It is useful for a large number of conversion, counting, and digital integration applications.

Ordering Information

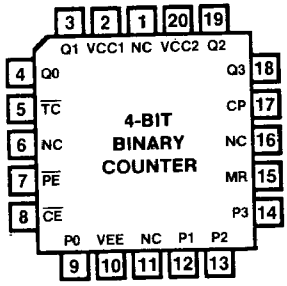
PART NUMBER	PACKAGE	TEMPERATURE
MC10H016	J, N, NL	Com

Pin Configuration

MC10H016
4-bit Binary Counter



MC10H016



Function Select Table

$\overline{CE}$	$\overline{PE}$	MR	CP	FUNCTION
L	L	L	Z	Load parallel (P_n to Q_n)
H	L	L	Z	Load parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters respond; slaves hold
X	X	H	X	Reset (Q_n = LOW, T_C = HIGH)

Z = Clock Pulse (Low to High)

ZZ = Clock Pulse (High to Low).

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

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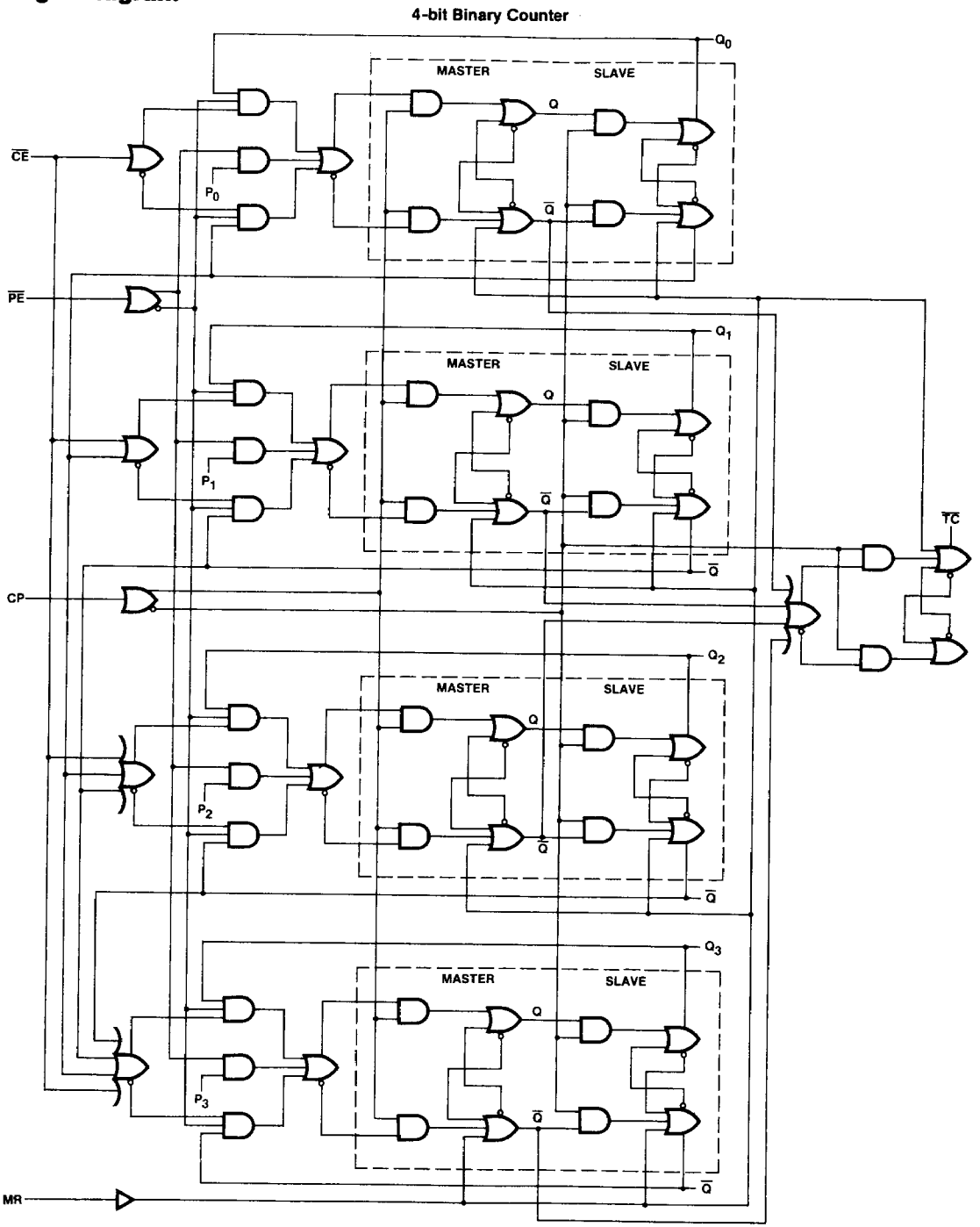
Monolithic Memories MMI

Logic Diagram



Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

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Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to 0 Vdc
Input voltage V_I (V_{CC} = 0) ..... 0 Vdc to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{STG}	Storage Temperature Range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	126	—	115	—	126	mA
I_{inH}	Input current HIGH	All except MR	—	450	—	265	—	265	µA
		Pin 12 MR	—	1190	—	700	—	700	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	Low input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = 5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Clock to Q	1.0	2.4	1.0	2.5	1.0	2.7	ns
		Clock to TC	0.7	2.4	0.7	2.5	0.7	2.6	
		MR to Q	0.7	2.4	0.7	2.5	0.7	2.6	
t_{set}	Setup time	Pn to Clock	2.0	—	2.0	—	2.0	—	ns
		CE or PE to Clock	2.5	—	2.5	—	2.5	—	
t_{hold}	Hold time	Clock to Pn	1.0	—	1.0	—	1.0	—	ns
		Clock to CE or PE	0.5	—	0.5	—	0.5	—	
f_{count}	Counting frequency		200	—	200	—	200	—	MHz
t_r,t+	Rise time		0.5	2.0	0.5	2.1	0.5	2.2	ns
t_f,t-	Fall time		0.5	2.0	0.5	2.1	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.