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# HM51W16160A Series

# HM51W18160A Series

1048576-word × 16-bit Dynamic Random Access Memory

# HITACHI

ADE-203-217B (Z)

Rev. 2.0

Jul. 2, 1996

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## Description

The Hitachi HM51W16160A Series, HM51W18160A Series are CMOS dynamic RAMs organized as 1,048,576-word × 16-bit. They employ the most advanced CMOS technology for high performance and low power. The HM51W16160A Series, HM51W18160A Series offer Fast Page Mode as a high speed access mode. They have package variations of 42-pin plastic SOJ and 50-pin plastic TSOP II.

## Features

- Single 3.3 V ( $\pm 0.3$  V)
- High speed
  - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode : 360 mW/324 mW/288 mW (max) (HM51W16160A Series)  
: 612 mW/540 mW/468 mW (max) (HM51W18160A Series)
  - Standby mode : 7.2 mW (max)  
: 0.54 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
  - 4096 refresh cycles : 64 ms (HM51W16160A Series)  
: 128 ms (L-version)
  - 1024 refresh cycles : 16 ms (HM51W18160A Series)  
: 128 ms (L-version)

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

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## HM51W16160A Series, HM51W18160A Series

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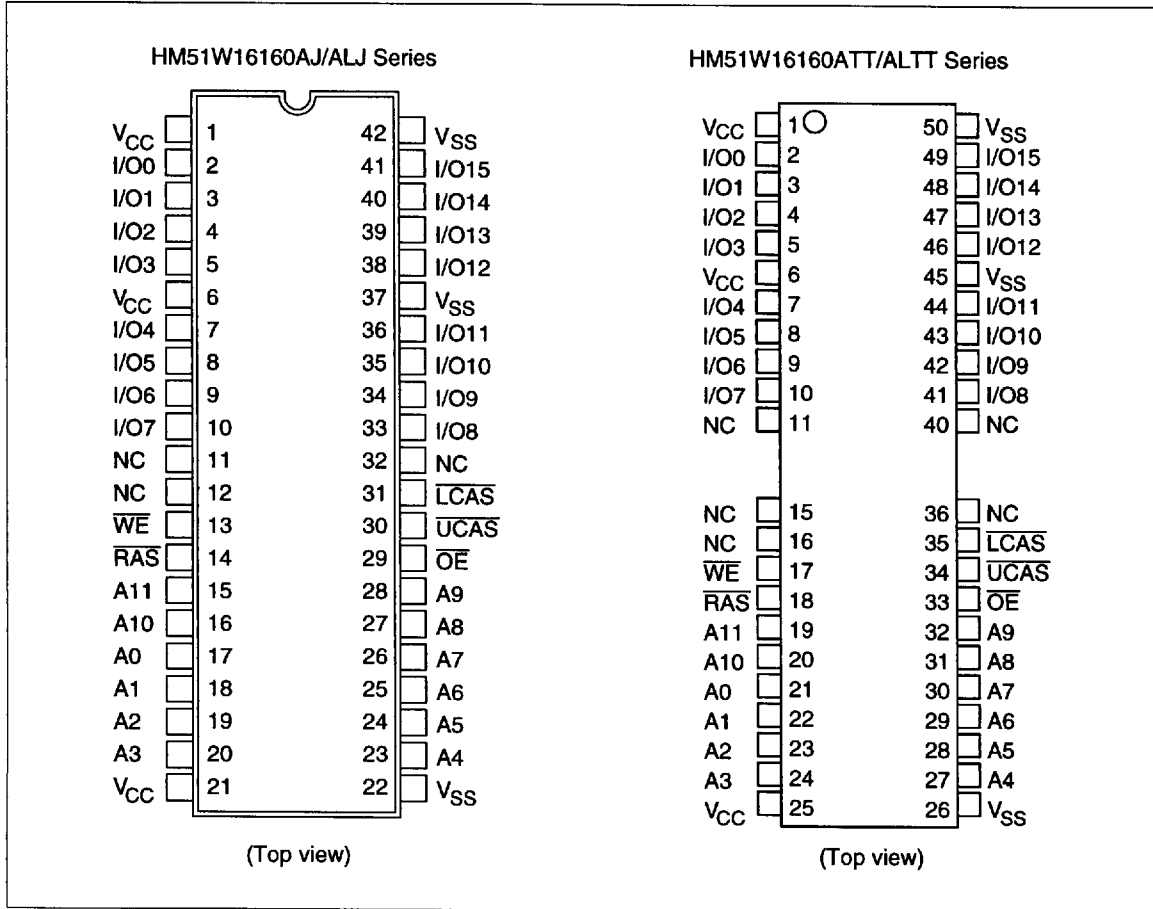
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)
- $\overline{2\text{CAS}}$ -byte control
- Battery backup operation (L-version)

### Ordering Information

| Type No.         | Access time | Package                                      |
|------------------|-------------|--|
| HM51W16160AJ-6   | 60 ns       | 400-mil 42-pin plastic SOJ (CP-42D)          |
| HM51W16160AJ-7   | 70 ns       |  |
| HM51W16160AJ-8   | 80 ns       |  |
| HM51W16160ALJ-6  | 60 ns       |  |
| HM51W16160ALJ-7  | 70 ns       |  |
| HM51W16160ALJ-8  | 80 ns       |  |
| HM51W18160AJ-6   | 60 ns       |  |
| HM51W18160AJ-7   | 70 ns       |  |
| HM51W18160AJ-8   | 80 ns       |  |
| HM51W18160ALJ-6  | 60 ns       |  |
| HM51W18160ALJ-7  | 70 ns       |  |
| HM51W18160ALJ-8  | 80 ns       |  |
| HM51W16160ATT-6  | 60 ns       | 400-mil 50-pin plastic TSOP II (TTP-50/44DC) |
| HM51W16160ATT-7  | 70 ns       |  |
| HM51W16160ATT-8  | 80 ns       |  |
| HM51W16160ALTT-6 | 60 ns       |  |
| HM51W16160ALTT-7 | 70 ns       |  |
| HM51W16160ALTT-8 | 80 ns       |  |
| HM51W18160ATT-6  | 60 ns       |  |
| HM51W18160ATT-7  | 70 ns       |  |
| HM51W18160ATT-8  | 80 ns       |  |
| HM51W18160ALTT-6 | 60 ns       |  |
| HM51W18160ALTT-7 | 70 ns       |  |
| HM51W18160ALTT-8 | 80 ns       |  |

# HM51W16160A Series, HM51W18160A Series

## Pin Arrangement

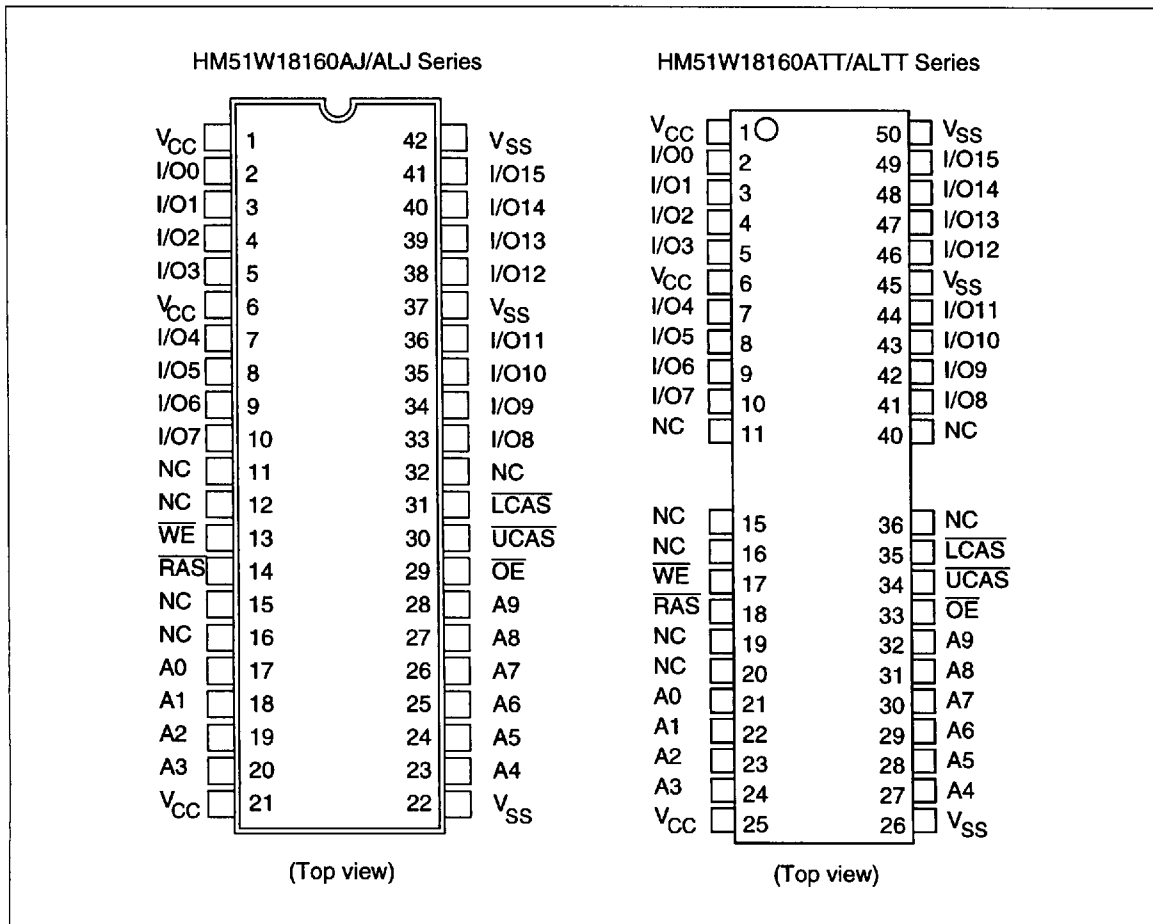


## Pin Description

| Pin name        | Function  |
|-----------------|---|
| A0 to A11       | Address input<br>— Row/Refresh address    A0 to A11<br>— Column address            A0 to A7 |
| I/O0 to I/O15   | Data input/Data output  |
| RAS             | Row address strobe  |
| UCAS, LCAS      | Column address strobe   |
| WE              | Read/Write enable   |
| OE              | Output enable   |
| V <sub>CC</sub> | Power supply  |
| V <sub>SS</sub> | Ground  |
| NC              | No connection   |

# HM51W16160A Series, HM51W18160A Series

## Pin Arrangement

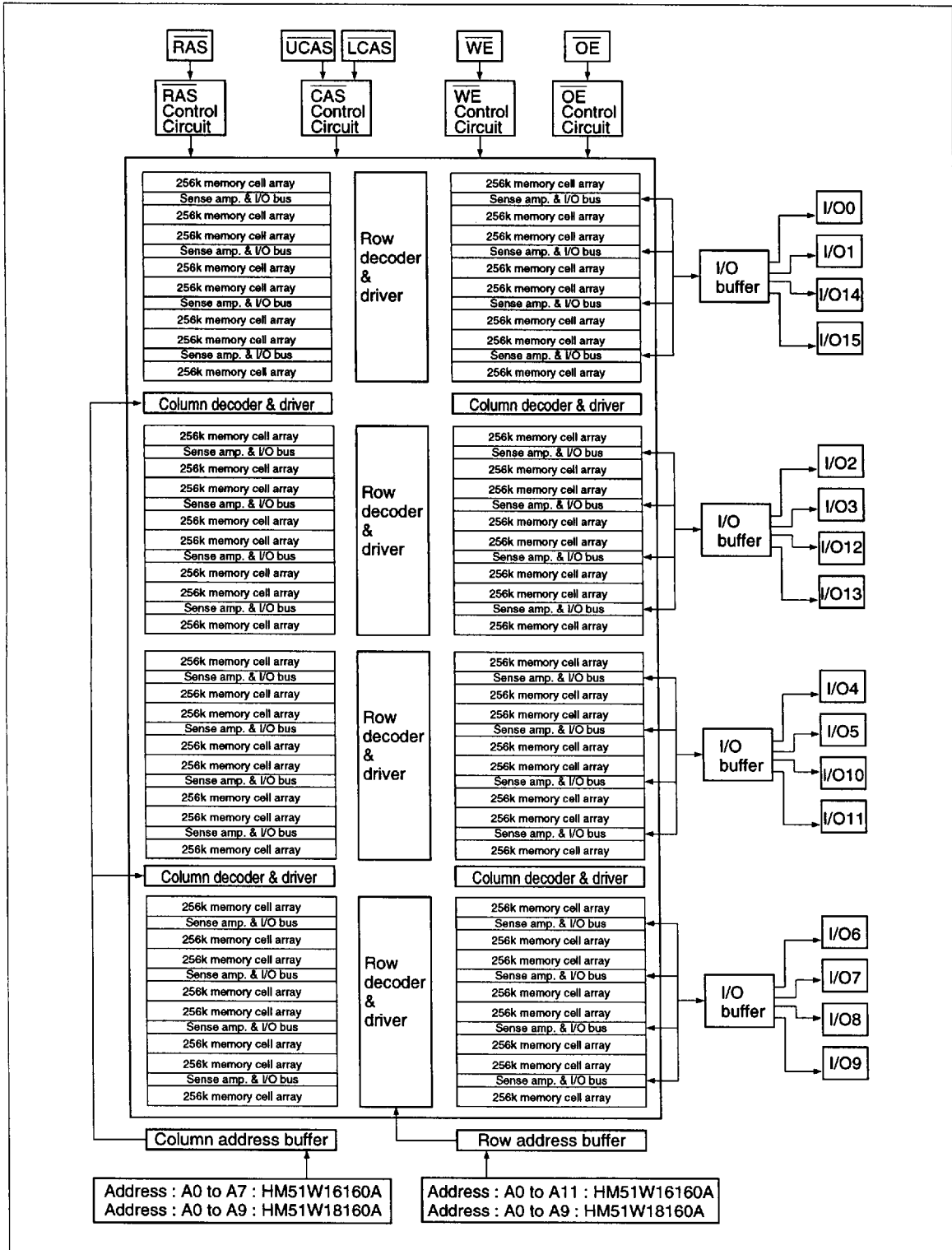


## Pin Description

| Pin name        | Function   |
|-----------------|--|
| A0 to A9        | Address input<br>— Row/Refresh address A0 to A9<br>— Column address A0 to A9 |
| I/O0 to I/O15   | Data input/Data output   |
| RAS             | Row address strobe   |
| UCAS, LCAS      | Column address strobe  |
| WE              | Read/Write enable  |
| OE              | Output enable  |
| V <sub>cc</sub> | Power supply   |
| V <sub>ss</sub> | Ground   |
| NC              | No connection  |

# HM51W16160A Series, HM51W18160A Series

## Block Diagram



## HM51W16160A Series, HM51W18160A Series

### Truth Table

| $\overline{\text{RAS}}$ | $\overline{\text{LCAS}}$ | $\overline{\text{UCAS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Output    | Operation  |
|-------------------------|--------------------------|--------------------------|------------------------|------------------------|-----------|--|
| H                       | D                        | D                        | D                      | D                      | Open      | Standby  |
| L                       | L                        | H                        | H                      | L                      | Valid     | Lower byte Read cycle  |
| L                       | H                        | L                        | H                      | L                      | Valid     | Upper byte   |
| L                       | L                        | L                        | H                      | L                      | Valid     | Word   |
| L                       | L                        | H                        | L* <sup>2</sup>        | D                      | Open      | Lower byte Early write cycle   |
| L                       | H                        | L                        | L* <sup>2</sup>        | D                      | Open      | Upper byte   |
| L                       | L                        | L                        | L* <sup>2</sup>        | D                      | Open      | Word   |
| L                       | L                        | H                        | L* <sup>2</sup>        | H                      | Undefined | Lower byte Delayed write cycle   |
| L                       | H                        | L                        | L* <sup>2</sup>        | H                      | Undefined | Upper byte   |
| L                       | L                        | L                        | L* <sup>2</sup>        | H                      | Undefined | Word   |
| L                       | L                        | H                        | H to L                 | L to H                 | Valid     | Lower byte Read-modify-write cycle   |
| L                       | H                        | L                        | H to L                 | L to H                 | Valid     | Upper byte   |
| L                       | L                        | L                        | H to L                 | L to H                 | Valid     | Word   |
| L                       | H                        | H                        | D                      | D                      | Open      | Word $\overline{\text{RAS}}$ -only refresh cycle                               |
| H to L                  | H                        | L                        | D                      | D                      | Open      | Word $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or |
| H to L                  | L                        | H                        | D                      | D                      | Open      | Word Self refresh cycle (L-version)  |
| H to L                  | L                        | L                        | D                      | D                      | Open      | Word   |
| L                       | L                        | L                        | H                      | H                      | Open      | Read cycle (Output disabled)   |

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2.  $t_{\text{wcs}} \geq 0$  ns Early write cycle

$t_{\text{wcs}} < 0$  ns Delayed write cycle

3. Mode is determined by the OR function of the  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ . (Mode is set by the earliest of  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  active edge and reset by the latest of  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  inactive edge.) However write OPERATION and output HIZ control are done independently by each  $\overline{\text{UCAS}}$ ,  $\overline{\text{LCAS}}$ .

ex. if  $\overline{\text{RAS}} = \text{H to L}$ ,  $\overline{\text{UCAS}} = \text{H}$ ,  $\overline{\text{LCAS}} = \text{L}$ , then  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle is selected.

## HM51W16160A Series, HM51W18160A Series

### Absolute Maximum Ratings

| Parameter                               | Symbol    | Value  | Unit |
|---|-----------|--|------|
| Voltage on any pin relative to $V_{SS}$ | $V_T$     | -0.5 to $V_{CC} + 0.5$ ( $\leq 4.6$ V (max)) | V    |
| Supply voltage relative to $V_{SS}$     | $V_{CC}$  | -0.5 to 4.6                                  | V    |
| Short circuit output current            | $I_{out}$ | 50   | mA   |
| Power dissipation                       | $P_T$     | 1.0  | W    |
| Operating temperature                   | $T_{opr}$ | 0 to +70                                     | °C   |
| Storage temperature                     | $T_{stg}$ | -55 to +125                                  | °C   |

### Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

| Parameter          | Symbol   | Min  | Typ | Max            | Unit | Notes |
|--------------------|----------|------|-----|----------------|------|-------|
| Supply voltage     | $V_{CC}$ | 3.0  | 3.3 | 3.6            | V    | 1, 2  |
| Input high voltage | $V_{IH}$ | 2.0  | —   | $V_{CC} + 0.3$ | V    | 1     |
| Input low voltage  | $V_{IL}$ | -0.3 | —   | 0.8            | V    | 1     |

Notes: 1. All voltage referred to  $V_{SS}$

2. The supply voltage with all  $V_{CC}$  pins must be on the same level. The supply voltage with all  $V_{SS}$  pins must be on the same level.

## HM51W16160A Series, HM51W18160A Series

### DC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ) (HM51W16160A Series)

| Parameter   | Symbol     | HM51W16160A |          |     |          |     |          | Unit          | Test conditions   |
|---|------------|-------------|----------|-----|----------|-----|----------|---------------|---|
|   |            | -6          |          | -7  |          | -8  |          |               |   |
|   |            | Min         | Max      | Min | Max      | Min | Max      |               |   |
| Operating current* <sup>1, *2</sup>   | $I_{CC1}$  | —           | 100      | —   | 90       | —   | 80       | mA            | $t_{RC} = \text{min}$   |
| Standby current   | $I_{CC2}$  | —           | 2        | —   | 2        | —   | 2        | mA            | TTL interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} = V_{IH}$<br>Dout = High-Z                          |
|   |            | —           | 1        | —   | 1        | —   | 1        | mA            | CMOS interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}},$<br>$\overline{\text{LCAS}} \geq V_{CC} - 0.2 \text{ V}$<br>Dout = High-Z |
| Standby current (L-version)   | $I_{CC2}$  | —           | 150      | —   | 150      | —   | 150      | $\mu\text{A}$ | CMOS interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}},$<br>$\overline{\text{LCAS}} \geq V_{CC} - 0.2 \text{ V}$<br>Dout = High-Z |
| RAS-only refresh current* <sup>2</sup>  | $I_{CC3}$  | —           | 100      | —   | 90       | —   | 80       | mA            | $t_{RC} = \text{min}$   |
| Standby current* <sup>1</sup>   | $I_{CC5}$  | —           | 5        | —   | 5        | —   | 5        | mA            | $\overline{\text{RAS}} = V_{IH}$<br>$\overline{\text{UCAS}}, \overline{\text{LCAS}} = V_{IL}$<br>Dout = enable                              |
| $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current          | $I_{CC6}$  | —           | 100      | —   | 90       | —   | 80       | mA            | $t_{RC} = \text{min}$   |
| Fast page mode current* <sup>1, *3</sup>  | $I_{CC7}$  | —           | 100      | —   | 90       | —   | 80       | mA            | $t_{PC} = \text{min}$   |
| Battery backup current* <sup>4</sup><br>(Standby with CBR refresh)<br>(L-version) | $I_{CC10}$ | —           | 400      | —   | 400      | —   | 400      | $\mu\text{A}$ | CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC} = 31.3 \mu\text{s}$<br>$t_{RAS} \leq 0.3 \mu\text{s}$                               |
| Self refresh mode current<br>(L-version)  | $I_{CC11}$ | —           | 250      | —   | 250      | —   | 250      | $\mu\text{A}$ | CMOS interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} \leq 0.2 \text{ V}$<br>Dout = High-Z               |
| Input leakage current   | $I_{LI}$   | -10         | 10       | -10 | 10       | -10 | 10       | $\mu\text{A}$ | $0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$  |
| Output leakage current  | $I_{LO}$   | -10         | 10       | -10 | 10       | -10 | 10       | $\mu\text{A}$ | $0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$<br>Dout = disable   |
| Output high voltage   | $V_{OH}$   | 2.4         | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V             | High Iout = -2 mA   |
| Output low voltage  | $V_{OL}$   | 0           | 0.4      | 0   | 0.4      | 0   | 0.4      | V             | Low Iout = 2 mA   |

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}} = V_{IH}$ .

4.  $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ ,  $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ .



## HM51W16160A Series, HM51W18160A Series

### DC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ) (HM51W18160A Series)

| Parameter   | Symbol     | HM51W18160A |          |     |          |     |          | Unit          | Test conditions   |
|---|------------|-------------|----------|-----|----------|-----|----------|---------------|---|
|   |            | -6          |          | -7  |          | -8  |          |               |   |
|   |            | Min         | Max      | Min | Max      | Min | Max      |               |   |
| Operating current* <sup>1, *2</sup>   | $I_{CC1}$  | —           | 170      | —   | 150      | —   | 130      | mA            | $t_{RC} = \text{min}$   |
| Standby current   | $I_{CC2}$  | —           | 2        | —   | 2        | —   | 2        | mA            | TTL interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} = V_{IH}$<br>Dout = High-Z                          |
|   |            | —           | 1        | —   | 1        | —   | 1        | mA            | CMOS interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}},$<br>$\overline{\text{LCAS}} \geq V_{CC} - 0.2 \text{ V}$<br>Dout = High-Z |
| Standby current<br>(L-version)  | $I_{CC2}$  | —           | 150      | —   | 150      | —   | 150      | $\mu\text{A}$ | CMOS interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}},$<br>$\overline{\text{LCAS}} \geq V_{CC} - 0.2 \text{ V}$<br>Dout = High-Z |
| $\overline{\text{RAS}}$ -only refresh current* <sup>2</sup>                       | $I_{CC3}$  | —           | 170      | —   | 150      | —   | 130      | mA            | $t_{RC} = \text{min}$   |
| Standby current* <sup>1</sup>   | $I_{CC5}$  | —           | 5        | —   | 5        | —   | 5        | mA            | $\overline{\text{RAS}} = V_{IH}$<br>$\overline{\text{UCAS}}, \overline{\text{LCAS}} = V_{IL}$<br>Dout = enable                              |
| $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh<br>current       | $I_{CC6}$  | —           | 170      | —   | 150      | —   | 130      | mA            | $t_{RC} = \text{min}$   |
| Fast page mode current* <sup>1, *3</sup>  | $I_{CC7}$  | —           | 170      | —   | 150      | —   | 130      | mA            | $t_{PC} = \text{min}$   |
| Battery backup current* <sup>4</sup><br>(Standby with CBR refresh)<br>(L-version) | $I_{CC10}$ | —           | 400      | —   | 400      | —   | 400      | $\mu\text{A}$ | CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC} = 125 \mu\text{s}$<br>$t_{RAS} \leq 0.3 \mu\text{s}$                                |
| Self refresh mode current<br>(L-version)  | $I_{CC11}$ | —           | 250      | —   | 250      | —   | 250      | $\mu\text{A}$ | CMOS interface<br>$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} \leq 0.2 \text{ V}$<br>Dout = High-Z               |
| Input leakage current   | $I_{LI}$   | -10         | 10       | -10 | 10       | -10 | 10       | $\mu\text{A}$ | $0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$  |
| Output leakage current  | $I_{LO}$   | -10         | 10       | -10 | 10       | -10 | 10       | $\mu\text{A}$ | $0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$<br>Dout = disable   |
| Output high voltage   | $V_{OH}$   | 2.4         | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V             | High Iout = -2 mA   |
| Output low voltage  | $V_{OL}$   | 0           | 0.4      | 0   | 0.4      | 0   | 0.4      | V             | Low Iout = 2 mA   |

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}} = V_{IH}$ .

4.  $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ ,  $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ .

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**HM51W16160A Series, HM51W18160A Series**

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**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )

| Parameter                              | Symbol   | Typ | Max | Unit | Notes |
|--|----------|-----|-----|------|-------|
| Input capacitance (Address)            | $C_{I1}$ | —   | 5   | pF   | 1     |
| Input capacitance (Clocks)             | $C_{I2}$ | —   | 7   | pF   | 1     |
| Output capacitance (Data-in, Data-out) | $C_{VO}$ | —   | 7   | pF   | 1, 2  |

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{UCAS}$  and  $\overline{LCAS} = V_{IH}$  to disable Dout.

## HM51W16160A Series, HM51W18160A Series

### AC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ) \*1, \*2, \*18, \*19, \*20

#### Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

#### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

|   |           | HM51W16160A/HM51W18160A |       |     |       |     |       |      |       |
|---|-----------|-------------------------|-------|-----|-------|-----|-------|------|-------|
|   |           | -6                      |       | -7  |       | -8  |       |      |       |
| Parameter   | Symbol    | Min                     | Max   | Min | Max   | Min | Max   | Unit | Notes |
| Random read or write cycle time                                   | $t_{RC}$  | 110                     | —     | 130 | —     | 150 | —     | ns   |       |
| $\overline{\text{RAS}}$ precharge time                            | $t_{RP}$  | 40                      | —     | 50  | —     | 60  | —     | ns   |       |
| $\overline{\text{CAS}}$ precharge time                            | $t_{CP}$  | 10                      | —     | 10  | —     | 10  | —     | ns   |       |
| $\overline{\text{RAS}}$ pulse width                               | $t_{RAS}$ | 60                      | 10000 | 70  | 10000 | 80  | 10000 | ns   |       |
| $\overline{\text{CAS}}$ pulse width                               | $t_{CAS}$ | 15                      | 10000 | 18  | 10000 | 20  | 10000 | ns   |       |
| Row address setup time  | $t_{ASR}$ | 0                       | —     | 0   | —     | 0   | —     | ns   |       |
| Row address hold time   | $t_{RAH}$ | 10                      | —     | 10  | —     | 10  | —     | ns   |       |
| Column address setup time   | $t_{ASC}$ | 0                       | —     | 0   | —     | 0   | —     | ns   | 21    |
| Column address hold time  | $t_{CAH}$ | 10                      | —     | 15  | —     | 15  | —     | ns   | 21    |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time     | $t_{RCD}$ | 20                      | 45    | 20  | 52    | 20  | 60    | ns   | 3     |
| $\overline{\text{RAS}}$ to column address delay time              | $t_{RAD}$ | 15                      | 30    | 15  | 35    | 15  | 40    | ns   | 4     |
| $\overline{\text{RAS}}$ hold time                                 | $t_{RSH}$ | 15                      | —     | 18  | —     | 20  | —     | ns   |       |
| $\overline{\text{CAS}}$ hold time                                 | $t_{CSH}$ | 60                      | —     | 70  | —     | 80  | —     | ns   | 23    |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | $t_{CRP}$ | 5                       | —     | 5   | —     | 5   | —     | ns   | 22    |
| $\overline{\text{OE}}$ to Din delay time                          | $t_{OED}$ | 15                      | —     | 18  | —     | 20  | —     | ns   | 5     |
| $\overline{\text{OE}}$ delay time from Din                        | $t_{DZO}$ | 0                       | —     | 0   | —     | 0   | —     | ns   | 6     |
| $\overline{\text{CAS}}$ delay time from Din                       | $t_{DZC}$ | 0                       | —     | 0   | —     | 0   | —     | ns   | 6     |
| Transition time (rise and fall)                                   | $t_f$     | 3                       | 50    | 3   | 50    | 3   | 50    | ns   | 7     |

## HM51W16160A Series, HM51W18160A Series

### Read Cycle

| Parameter   | Symbol           | HM51W16160A/HM51W18160A |     |     |     |     |     | Unit | Notes     |
|---|------------------|-------------------------|-----|-----|-----|-----|-----|------|-----------|
|   |                  | -6                      |     | -7  |     | -8  |     |      |           |
|   |                  | Min                     | Max | Min | Max | Min | Max |      |           |
| Access time from $\overline{\text{RAS}}$            | $t_{\text{RAC}}$ | —                       | 60  | —   | 70  | —   | 80  | ns   | 8, 9      |
| Access time from $\overline{\text{CAS}}$            | $t_{\text{CAC}}$ | —                       | 15  | —   | 18  | —   | 20  | ns   | 9, 10, 17 |
| Access time from address                            | $t_{\text{AA}}$  | —                       | 30  | —   | 35  | —   | 40  | ns   | 9, 11, 17 |
| Access time from $\overline{\text{OE}}$             | $t_{\text{OEA}}$ | —                       | 15  | —   | 18  | —   | 20  | ns   | 9, 25     |
| Read command setup time                             | $t_{\text{RCS}}$ | 0                       | —   | 0   | —   | 0   | —   | ns   |           |
| Read command hold time to $\overline{\text{CAS}}$   | $t_{\text{RCH}}$ | 0                       | —   | 0   | —   | 0   | —   | ns   | 12, 22    |
| Read command hold time to $\overline{\text{RAS}}$   | $t_{\text{RRH}}$ | 5                       | —   | 5   | —   | 5   | —   | ns   | 12        |
| Column address to $\overline{\text{RAS}}$ lead time | $t_{\text{RAL}}$ | 30                      | —   | 35  | —   | 40  | —   | ns   |           |
| Column address to $\overline{\text{CAS}}$ lead time | $t_{\text{CAL}}$ | 30                      | —   | 35  | —   | 40  | —   | ns   |           |
| $\overline{\text{CAS}}$ to output in low-Z          | $t_{\text{CLZ}}$ | 0                       | —   | 0   | —   | 0   | —   | ns   |           |
| Output data hold time                               | $t_{\text{OH}}$  | 3                       | —   | 3   | —   | 3   | —   | ns   |           |
| Output data hold time from $\overline{\text{OE}}$   | $t_{\text{OHO}}$ | 3                       | —   | 3   | —   | 3   | —   | ns   |           |
| Output buffer turn-off time                         | $t_{\text{OFF}}$ | —                       | 15  | —   | 15  | —   | 15  | ns   | 13        |
| Output buffer turn-off to $\overline{\text{OE}}$    | $t_{\text{OEZ}}$ | —                       | 15  | —   | 15  | —   | 15  | ns   | 13        |
| $\overline{\text{CAS}}$ to Din delay time           | $t_{\text{ODD}}$ | 15                      | —   | 18  | —   | 20  | —   | ns   | 5         |

### Write Cycle

| Parameter  | Symbol           | HM51W16160A/HM51W18160A |     |     |     |     |     | Unit | Notes  |
|--|------------------|-------------------------|-----|-----|-----|-----|-----|------|--------|
|  |                  | -6                      |     | -7  |     | -8  |     |      |        |
|  |                  | Min                     | Max | Min | Max | Min | Max |      |        |
| Write command setup time                           | $t_{\text{WCS}}$ | 0                       | —   | 0   | —   | 0   | —   | ns   | 14, 21 |
| Write command hold time                            | $t_{\text{WCH}}$ | 10                      | —   | 15  | —   | 15  | —   | ns   | 21     |
| Write command pulse width                          | $t_{\text{WP}}$  | 10                      | —   | 10  | —   | 10  | —   | ns   |        |
| Write command to $\overline{\text{RAS}}$ lead time | $t_{\text{RWL}}$ | 15                      | —   | 18  | —   | 20  | —   | ns   |        |
| Write command to $\overline{\text{CAS}}$ lead time | $t_{\text{CWL}}$ | 15                      | —   | 18  | —   | 20  | —   | ns   | 23     |
| Data-in setup time                                 | $t_{\text{DS}}$  | 0                       | —   | 0   | —   | 0   | —   | ns   | 15, 23 |
| Data-in hold time                                  | $t_{\text{DH}}$  | 10                      | —   | 15  | —   | 15  | —   | ns   | 15, 23 |

## HM51W16160A Series, HM51W18160A Series

### Read-Modify-Write Cycle

| Parameter                                      | Symbol    | HM51W16160A/HM51W18160A |     |     |     |     |     | Unit | Notes |
|--|-----------|-------------------------|-----|-----|-----|-----|-----|------|-------|
|  |           | -6                      |     | -7  |     | -8  |     |      |       |
|  |           | Min                     | Max | Min | Max | Min | Max |      |       |
| Read-modify-write cycle time                   | $t_{RWC}$ | 155                     | —   | 181 | —   | 205 | —   | ns   |       |
| RAS to $\overline{WE}$ delay time              | $t_{RWD}$ | 85                      | —   | 98  | —   | 110 | —   | ns   | 14    |
| CAS to $\overline{WE}$ delay time              | $t_{CWD}$ | 40                      | —   | 46  | —   | 50  | —   | ns   | 14    |
| Column address to $\overline{WE}$ delay time   | $t_{AWD}$ | 55                      | —   | 63  | —   | 70  | —   | ns   | 14    |
| $\overline{OE}$ hold time from $\overline{WE}$ | $t_{OEH}$ | 15                      | —   | 18  | —   | 20  | —   | ns   |       |

### Refresh Cycle

| Parameter                          | Symbol    | HM51W16160A/HM51W18160A |     |     |     |     |     | Unit | Notes |
|------------------------------------|-----------|-------------------------|-----|-----|-----|-----|-----|------|-------|
|                                    |           | -6                      |     | -7  |     | -8  |     |      |       |
|                                    |           | Min                     | Max | Min | Max | Min | Max |      |       |
| CAS setup time (CBR refresh cycle) | $t_{CSR}$ | 5                       | —   | 5   | —   | 5   | —   | ns   | 21    |
| CAS hold time (CBR refresh cycle)  | $t_{CHR}$ | 10                      | —   | 10  | —   | 10  | —   | ns   | 22    |
| RAS precharge to CAS hold time     | $t_{RPC}$ | 0                       | —   | 0   | —   | 0   | —   | ns   | 21    |

### Fast Page Mode Cycle

| Parameter  | Symbol     | HM51W16160A/HM51W18160A |        |     |        |     |        | Unit | Notes     |
|--|------------|-------------------------|--------|-----|--------|-----|--------|------|-----------|
|  |            | -6                      |        | -7  |        | -8  |        |      |           |
|  |            | Min                     | Max    | Min | Max    | Min | Max    |      |           |
| Fast page mode cycle time                                  | $t_{PC}$   | 40                      | —      | 45  | —      | 50  | —      | ns   |           |
| Fast page mode $\overline{RAS}$ pulse width                | $t_{RASP}$ | —                       | 100000 | —   | 100000 | —   | 100000 | ns   | 16        |
| Access time from $\overline{CAS}$ precharge                | $t_{CPA}$  | —                       | 35     | —   | 40     | —   | 45     | ns   | 9, 17, 22 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | 35                      | —      | 40  | —      | 45  | —      | ns   |           |

## HM51W16160A Series, HM51W18160A Series

### Fast Page Mode Read-Modify-Write Cycle

| Parameter  | Symbol     | HM51W16160A/HM51W18160A |     |     |     |     |     | Unit | Notes  |
|--|------------|-------------------------|-----|-----|-----|-----|-----|------|--------|
|  |            | -6                      |     | -7  |     | -8  |     |      |        |
|  |            | Min                     | Max | Min | Max | Min | Max |      |        |
| Fast page mode read-modify-write cycle time                | $t_{PRWC}$ | 85                      | —   | 96  | —   | 105 | —   | ns   |        |
| $\overline{WE}$ delay time from $\overline{CAS}$ precharge | $t_{CPW}$  | 60                      | —   | 68  | —   | 75  | —   | ns   | 14, 22 |

### Refresh (HM51W16160A Series)

| Parameter                  | Symbol    | Max | Unit | Note        |
|----------------------------|-----------|-----|------|-------------|
| Refresh period             | $t_{REF}$ | 64  | ms   | 4096 cycles |
| Refresh period (L-version) | $t_{REF}$ | 128 | ms   | 4096 cycles |

### Refresh (HM51W18160A Series)

| Parameter                  | Symbol    | Max | Unit | Note        |
|----------------------------|-----------|-----|------|-------------|
| Refresh period             | $t_{REF}$ | 16  | ms   | 1024 cycles |
| Refresh period (L-version) | $t_{REF}$ | 128 | ms   | 1024 cycles |

## HM51W16160A Series, HM51W18160A Series

### Self Refresh Mode (L-version)

| Parameter   | Symbol            | HM51W16160AL/HM51W18160AL |     |     |     |     |     | Unit          | Notes |
|---|-------------------|---------------------------|-----|-----|-----|-----|-----|---------------|-------|
|   |                   | -6                        |     | -7  |     | -8  |     |               |       |
|   |                   | Min                       | Max | Min | Max | Min | Max |               |       |
| $\overline{\text{RAS}}$ pulse width (Self refresh)    | $t_{\text{RASS}}$ | 100                       | —   | 100 | —   | 100 | —   | $\mu\text{s}$ | 26    |
| $\overline{\text{RAS}}$ precharge time (Self refresh) | $t_{\text{RPS}}$  | 110                       | —   | 130 | —   | 150 | —   | ns            |       |
| $\overline{\text{CAS}}$ hold time (Self refresh)      | $t_{\text{CHS}}$  | -50                       | —   | -50 | —   | -50 | —   | ns            |       |

- Notes:
- AC measurements assume  $t_f = 5$  ns.
  - An initial pause of 200  $\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles are required.
  - Operation with the  $t_{\text{RCD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RCD}}$  (max) is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}$  (max) limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
  - Operation with the  $t_{\text{RAD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RAD}}$  (max) is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}$  (max) limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
  - Either  $t_{\text{OED}}$  or  $t_{\text{ODD}}$  must be satisfied.
  - Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
  - $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max).
  - Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}$  (max) and  $t_{\text{RAD}} \leq t_{\text{RAD}}$  (max). If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
  - Measured with a load circuit equivalent to 1 TTL loads and 100 pF. ( $V_{\text{OH}} = 2.0$  V,  $V_{\text{OL}} = 0.8$  V)
  - Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}$  (max) and  $t_{\text{RCD}} + t_{\text{CAC}}$  (max)  $\geq t_{\text{RAD}} + t_{\text{AA}}$  (max).
  - Assumes that  $t_{\text{RAD}} \geq t_{\text{RAD}}$  (max) and  $t_{\text{RCD}} + t_{\text{CAC}}$  (max)  $\leq t_{\text{RAD}} + t_{\text{AA}}$  (max).
  - Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
  - $t_{\text{OFF}}$  (max) and  $t_{\text{OEZ}}$  (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  - $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}}$  (min),  $t_{\text{CWD}} \geq t_{\text{CWD}}$  (min), and  $t_{\text{AWD}} \geq t_{\text{AWD}}$  (min), or  $t_{\text{CWD}} \geq t_{\text{CWD}}$  (min),  $t_{\text{AWD}} \geq t_{\text{AWD}}$  (min) and  $t_{\text{CPW}} \geq t_{\text{CPW}}$  (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  - These parameters are referred to  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in delayed write or read-modify-write cycles.
  - $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in fast page mode cycles.
  - Access time is determined by the longest among  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{CPA}}$ .
  - In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device. After  $\overline{\text{RAS}}$  is reset, if  $t_{\text{OEH}} \geq t_{\text{CWL}}$ , the I/O pin will remain open circuit (high impedance); if  $t_{\text{OEH}} < t_{\text{CWL}}$ , invalid data will be out at each I/O.
  - When both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  go low at the same time, all 16-bit data are written into the device.  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  cannot be staggered within the same write/read cycles.
  - All the  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins shall be supplied with the same voltages.
  - $t_{\text{ASC}}$ ,  $t_{\text{CAH}}$ ,  $t_{\text{RCS}}$ ,  $t_{\text{WCS}}$ ,  $t_{\text{WCH}}$ ,  $t_{\text{CSR}}$  and  $t_{\text{RPC}}$  are determined by the earlier falling edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  - $t_{\text{CRP}}$ ,  $t_{\text{CHR}}$ ,  $t_{\text{RCH}}$ ,  $t_{\text{CPA}}$  and  $t_{\text{CPW}}$  are determined by the later rising edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  - $t_{\text{CWL}}$ ,  $t_{\text{DH}}$  and  $t_{\text{DS}}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .

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## HM51W16160A Series, HM51W18160A Series

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24.  $t_{CP}$  is determined by the time that both  $\overline{UCAS}$  and  $\overline{LCAS}$  are high.
25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH\ min}/V_{IL\ max}$  level.
26. Please do not use  $t_{RASS}$  timing,  $10\ \mu s \leq t_{RASS} \leq 100\ \mu s$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} \geq 100\ \mu s$ , then  $\overline{RAS}$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .
27. If you use distributed CBR refresh mode with  $15.6\ \mu s$  interval in normal read/write cycle, CBR refresh should be executed within  $15.6\ \mu s$  immediately after exiting from and before entering into self refresh mode.
28. If you use  $\overline{RAS}$  only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 1024 cycles (4096 cycles: HM51W16160A Series, 1024 cycles: HM51W18160A Series) of distributed CBR refresh with  $15.6\ \mu s$  interval should be executed within 64 or 16 ms (64 ms: HM51W16160A, 16 ms: HM51W18160A) immediately after exiting from and before entering into the self refresh mode.
29. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
30. XXX: H or L (H:  $V_{IH\ (min)} \leq V_{IN} \leq V_{IH\ (max)}$ , L:  $V_{IL\ (min)} \leq V_{IN} \leq V_{IL\ (max)}$ )  
///: Invalid Dout

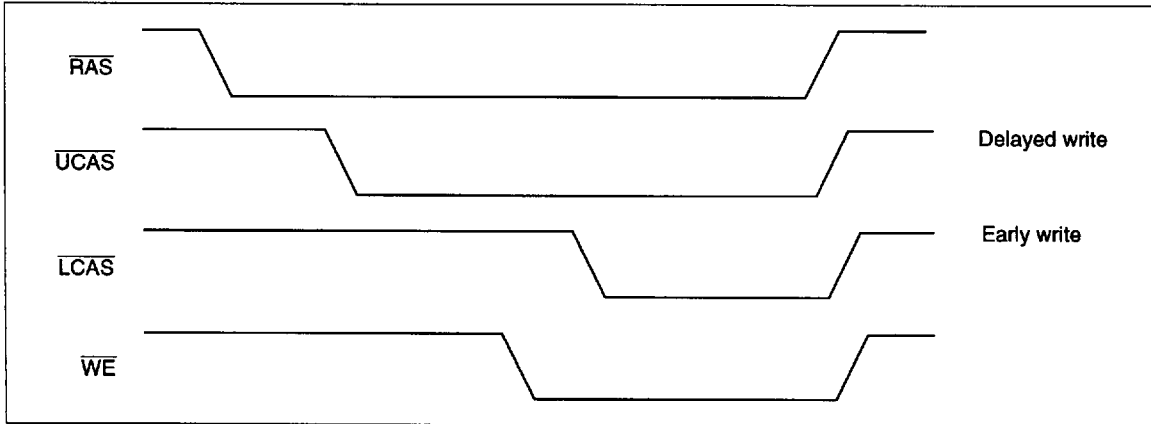


## HM51W16160A Series, HM51W18160A Series

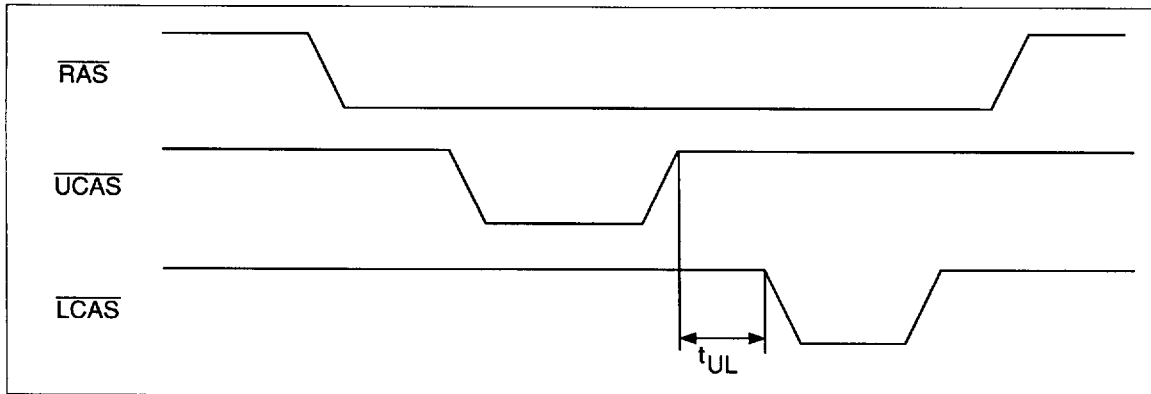
### Notes concerning $\overline{2CAS}$ control

Please do not separate the  $\overline{UCAS/LCAS}$  operation timing intentionally. However skew between  $\overline{UCAS/LCAS}$  are allowed under the following conditions.

1. Each of the  $\overline{UCAS/LCAS}$  should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



3. Closely separated upper/lower byte control is not allowed. However when the condition ( $t_{CP} \leq t_{UL}$ ) is satisfied, fast page mode can be performed.

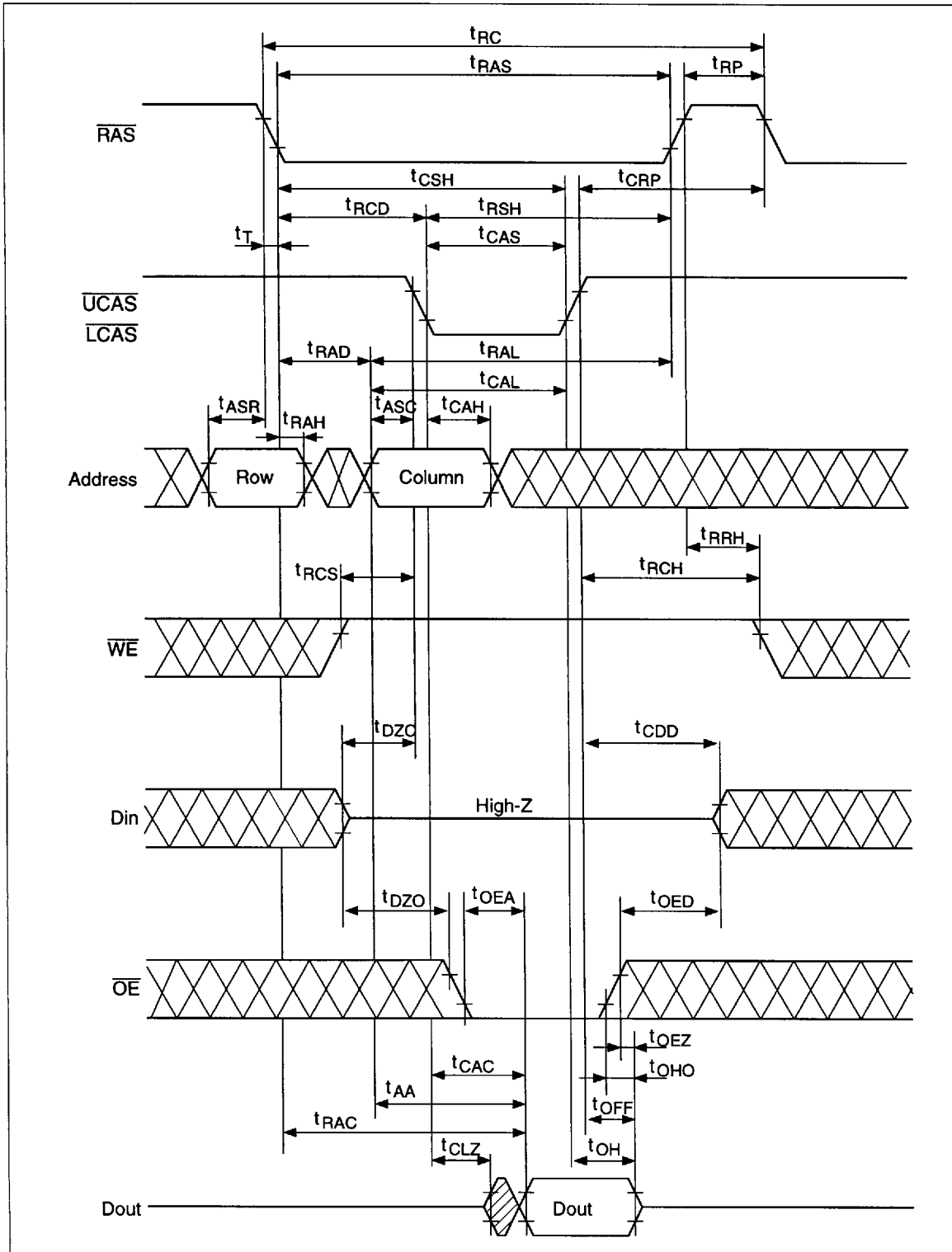


4. Byte control operation by remaining  $\overline{UCAS}$  or  $\overline{LCAS}$  high is guaranteed.

# HM51W16160A Series, HM51W18160A Series

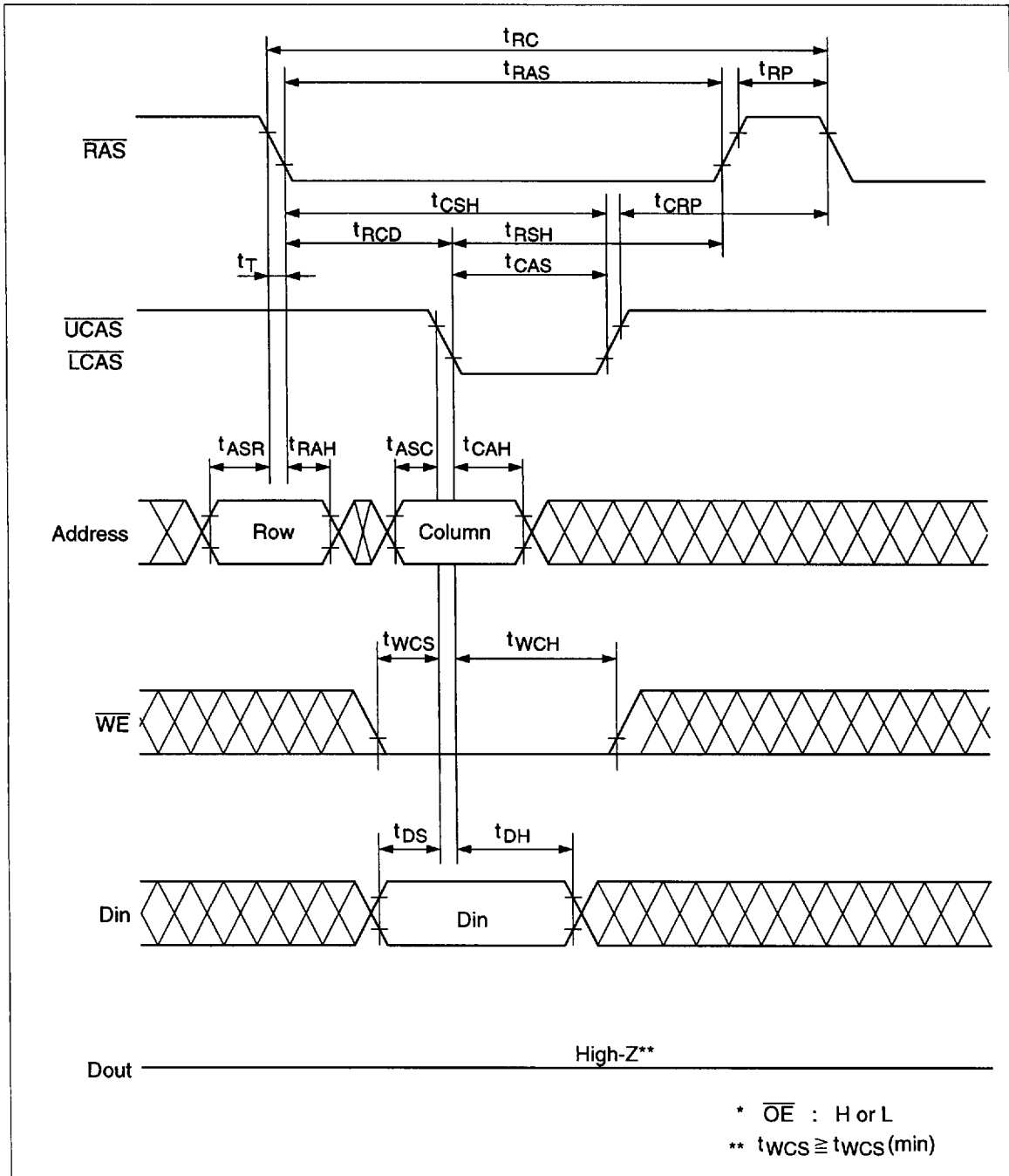
## Timing Waveforms\*30

### Read Cycle



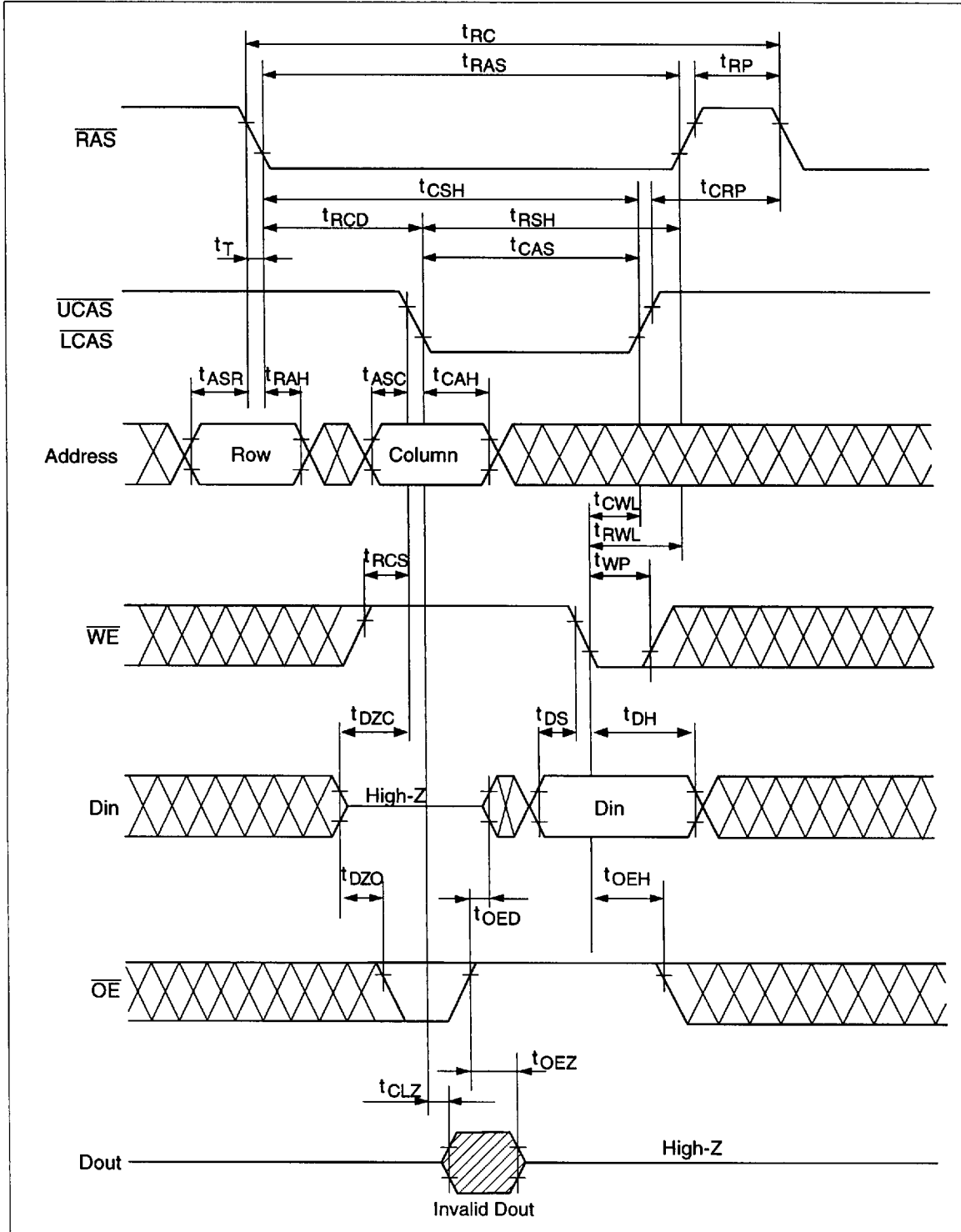
# HM51W16160A Series, HM51W18160A Series

## Early Write Cycle



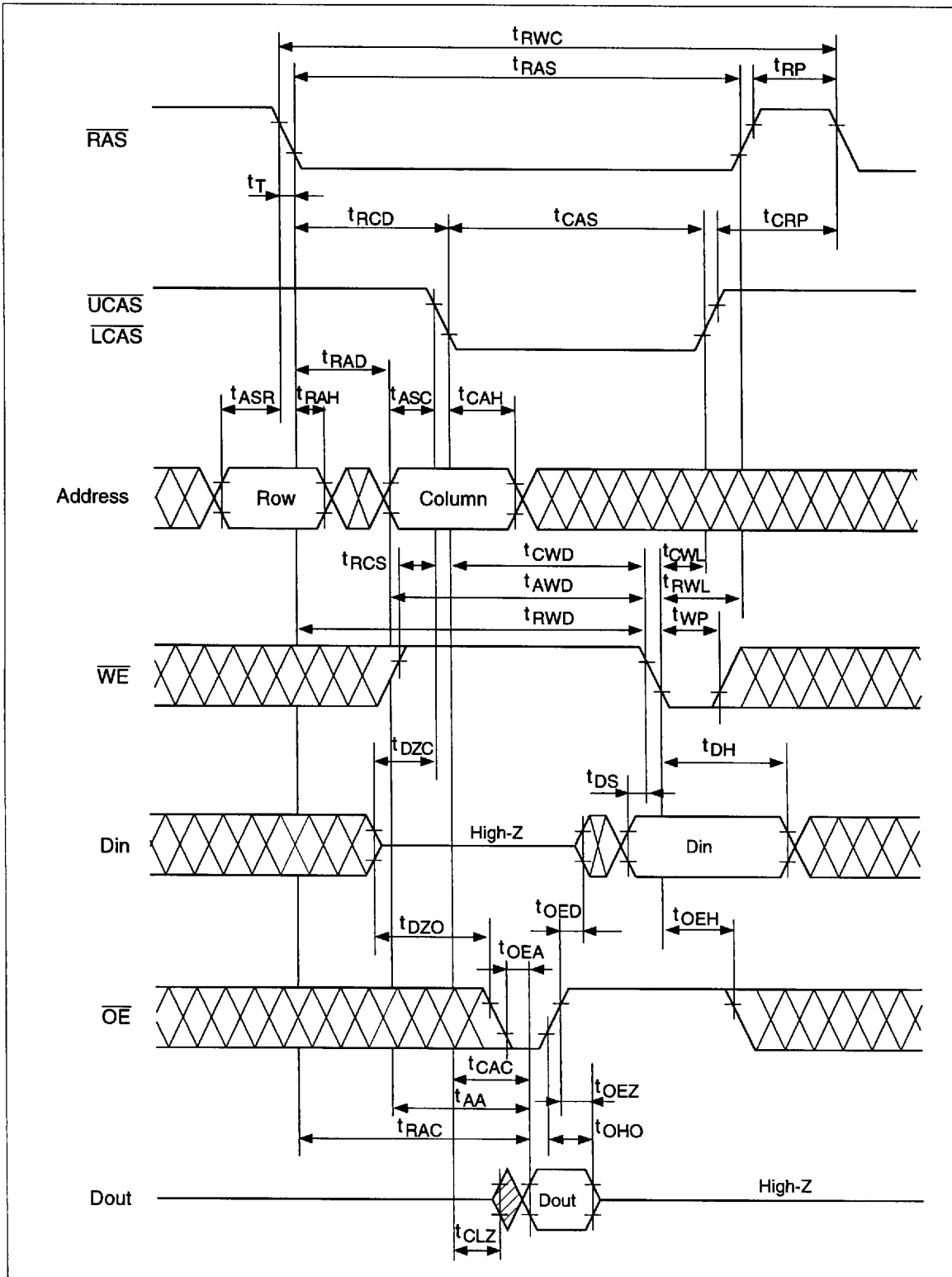
# HM51W16160A Series, HM51W18160A Series

## Delayed Write Cycle\*18



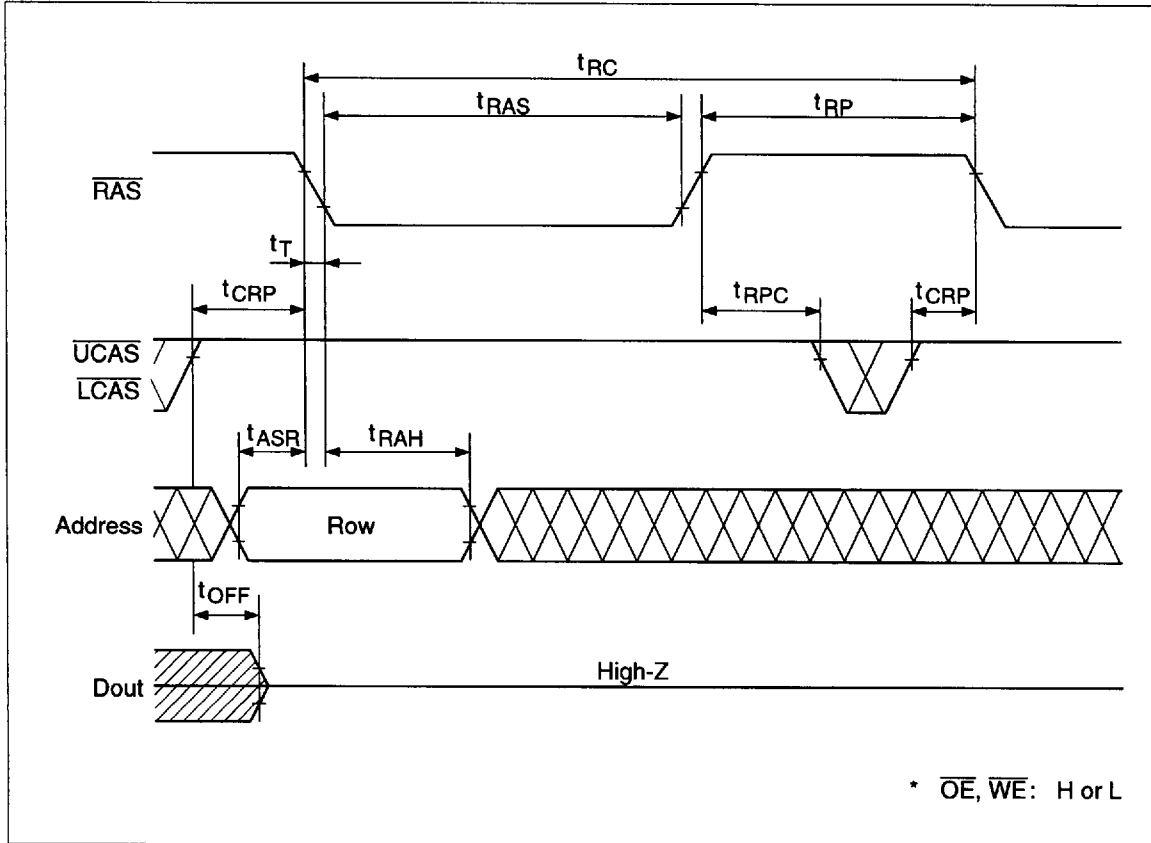
# HM51W16160A Series, HM51W18160A Series

## Read-Modify-Write Cycle\*18



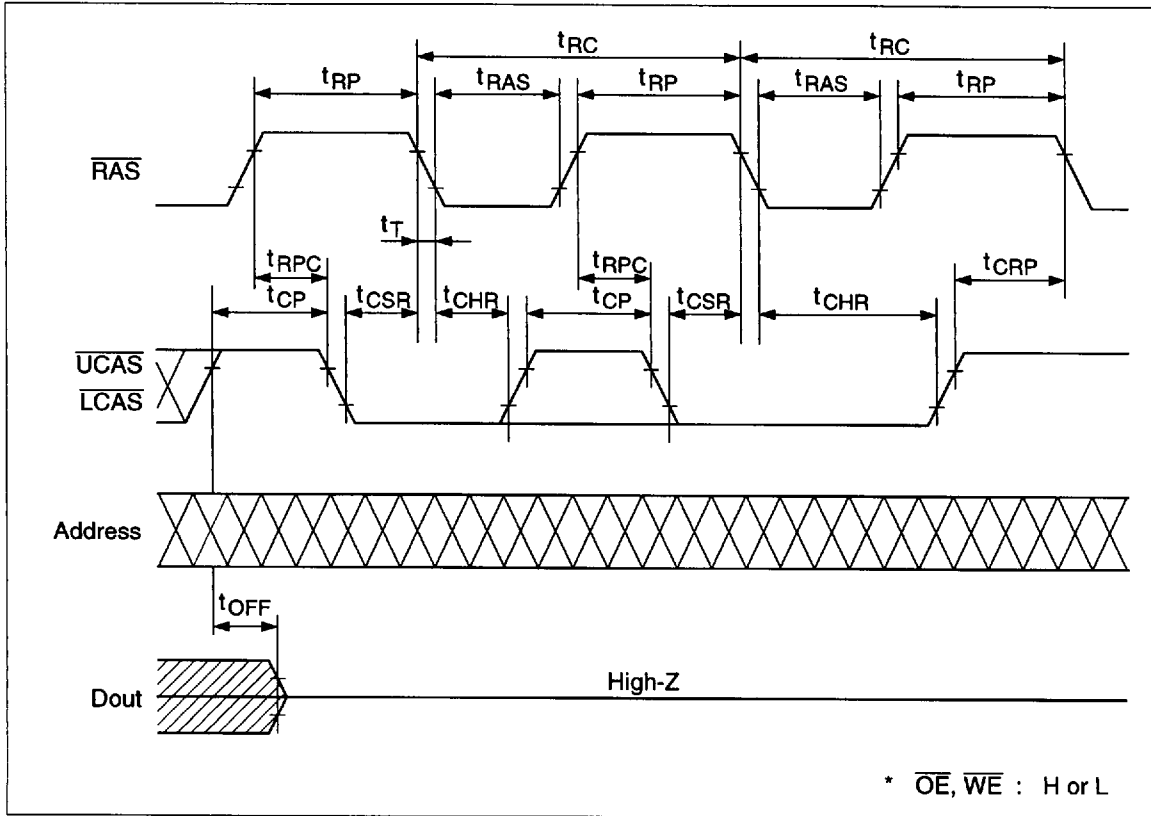
# HM51W16160A Series, HM51W18160A Series

## RAS-Only Refresh Cycle



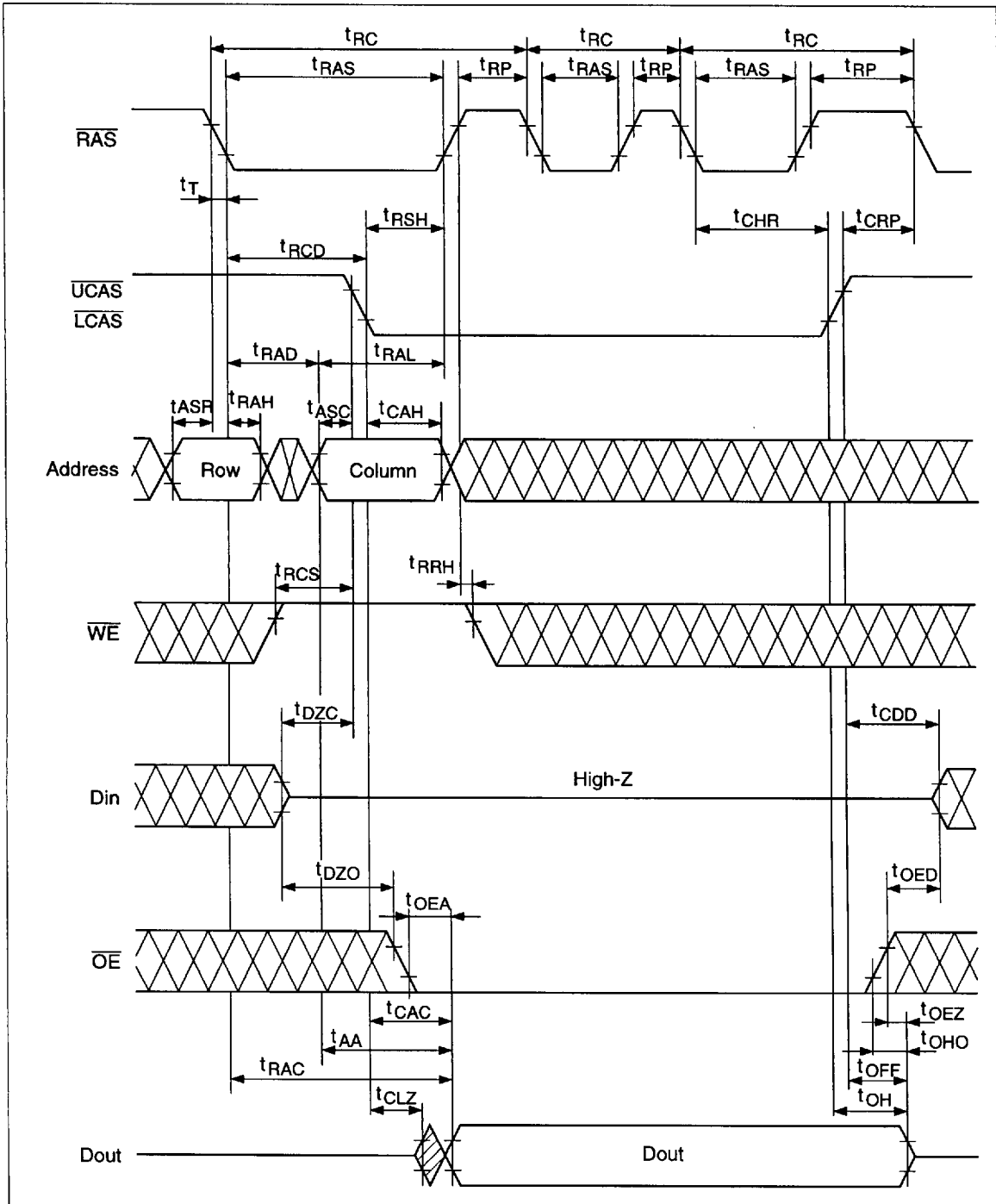
# HM51W16160A Series, HM51W18160A Series

## CAS-Before-RAS Refresh Cycle



# HM51W16160A Series, HM51W18160A Series

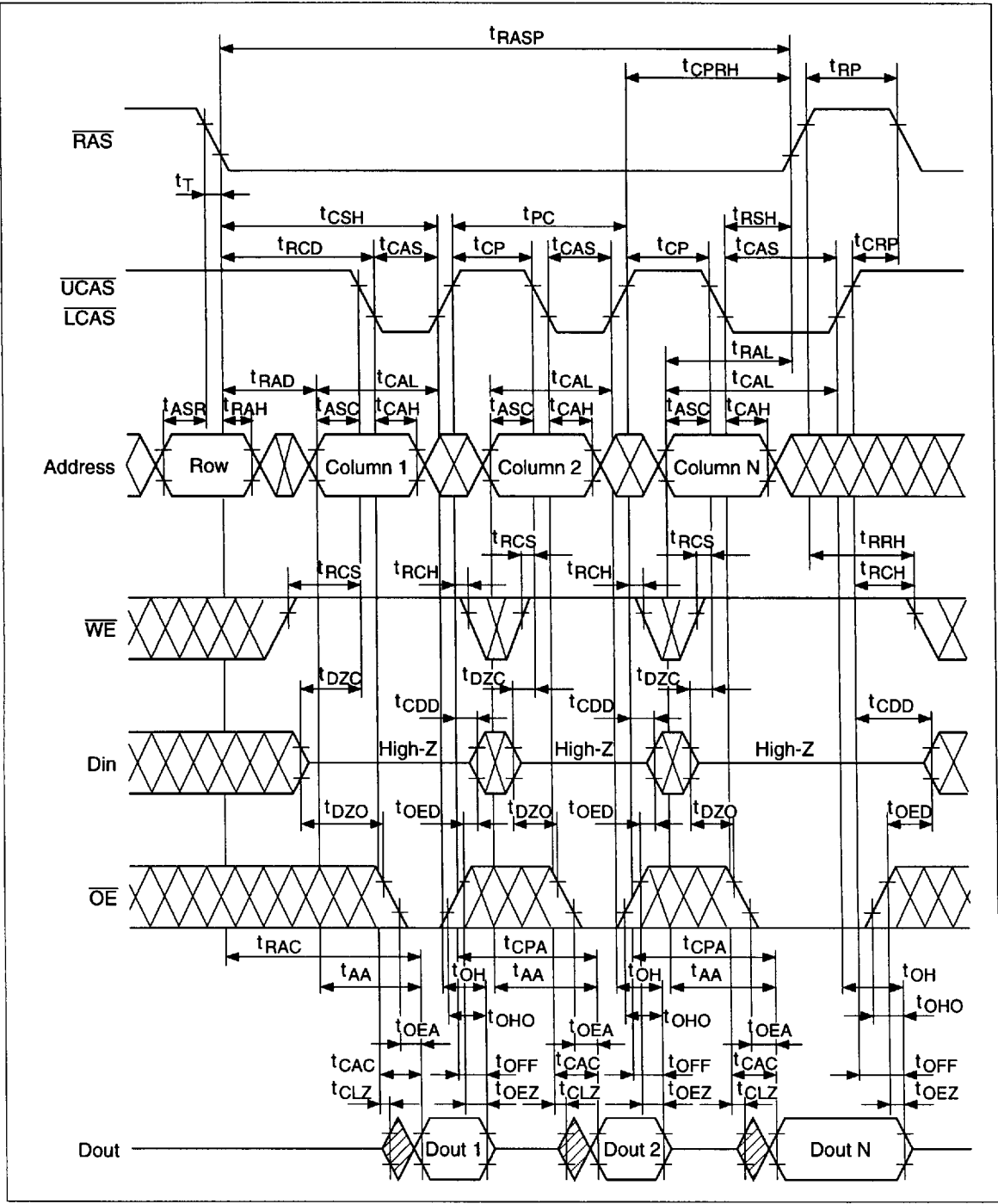
## Hidden Refresh Cycle





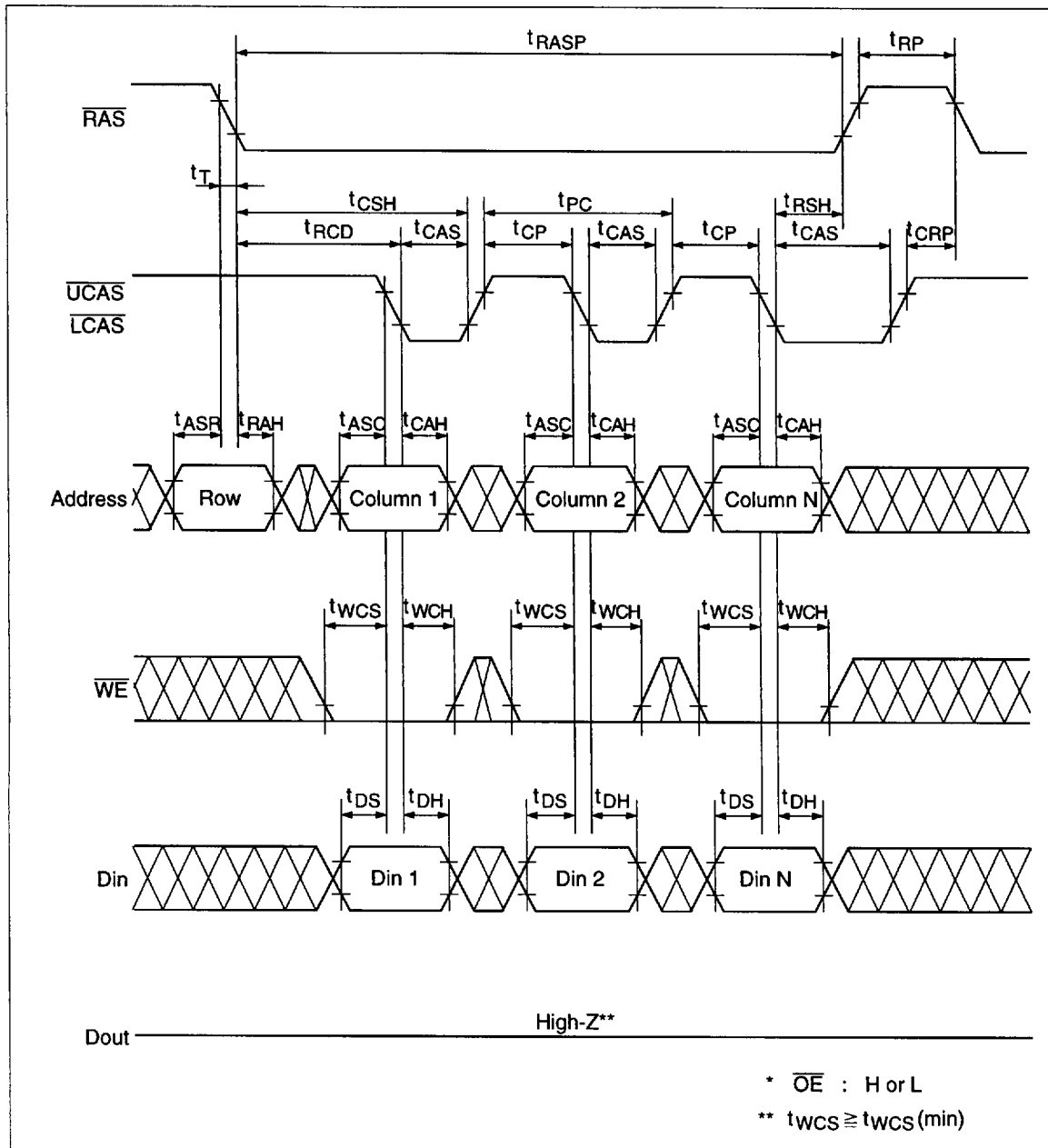
**HM51W16160A Series, HM51W18160A Series**

**Fast Page Read Cycle**



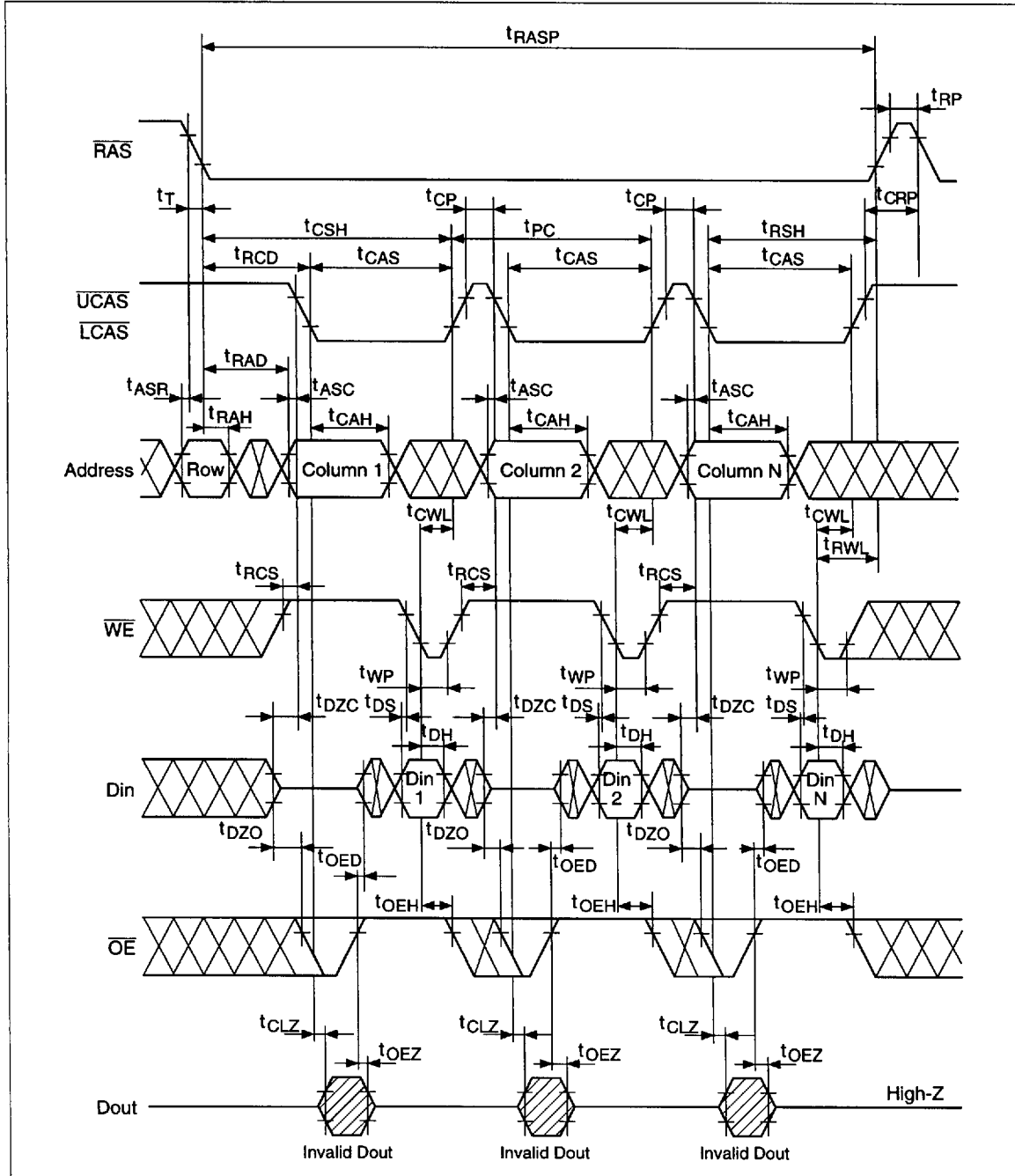
# HM51W16160A Series, HM51W18160A Series

## Fast Page Mode Early Write Cycle



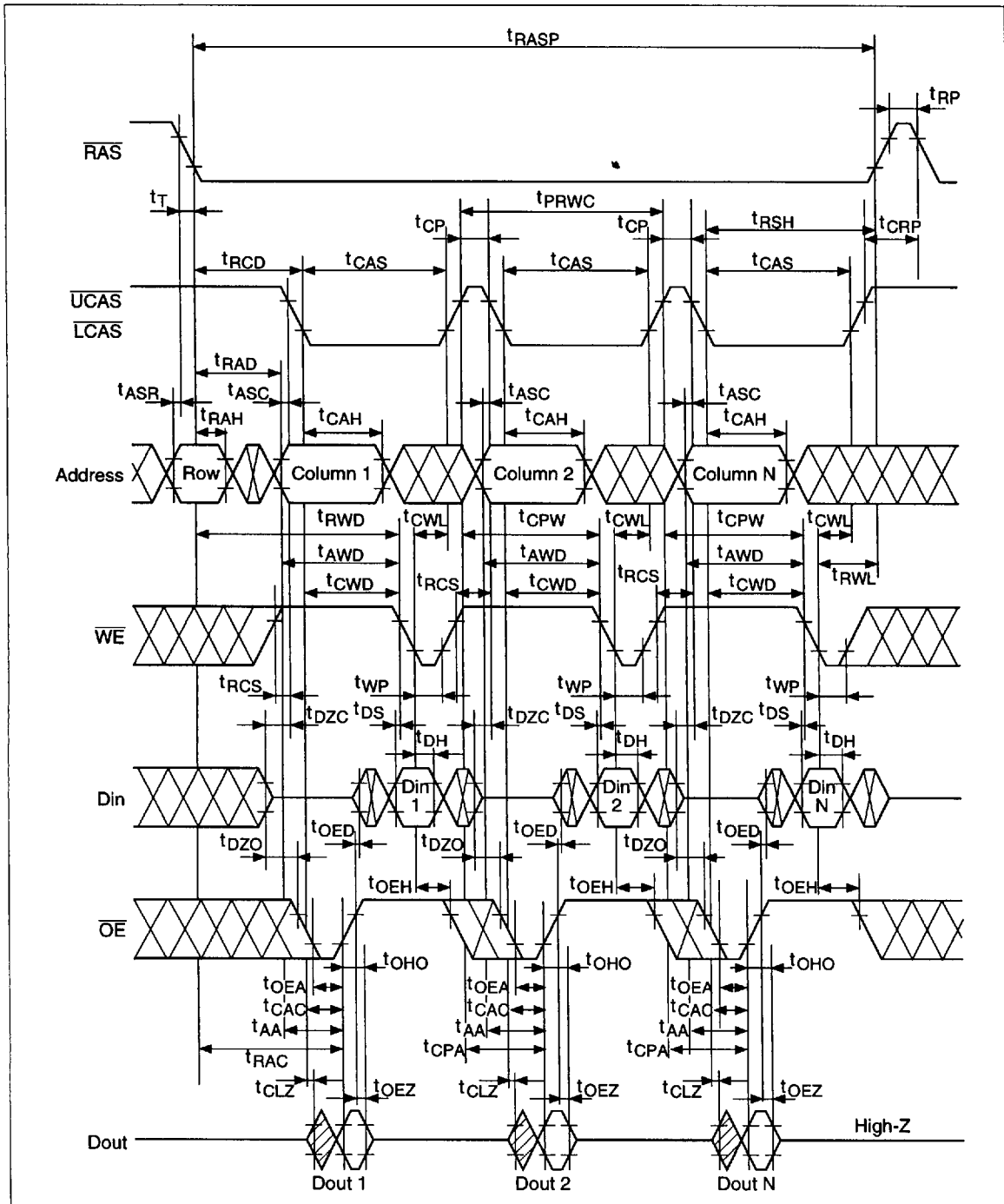
# HM51W16160A Series, HM51W18160A Series

## Fast Page Mode Delayed Write Cycle\*18



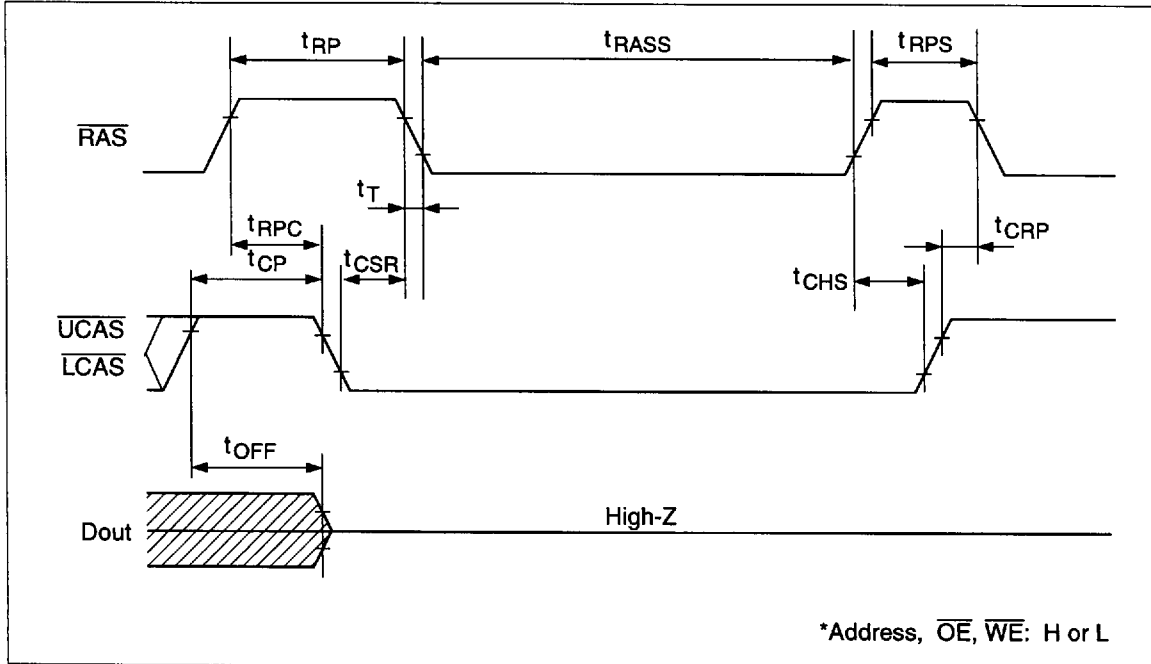
# HM51W16160A Series, HM51W18160A Series

## Fast Page Mode Read-Modify-Write Cycle\*18



# HM51W16160A Series, HM51W18160A Series

Self Refresh Cycle (L-version)\*26, 27, 28, 29



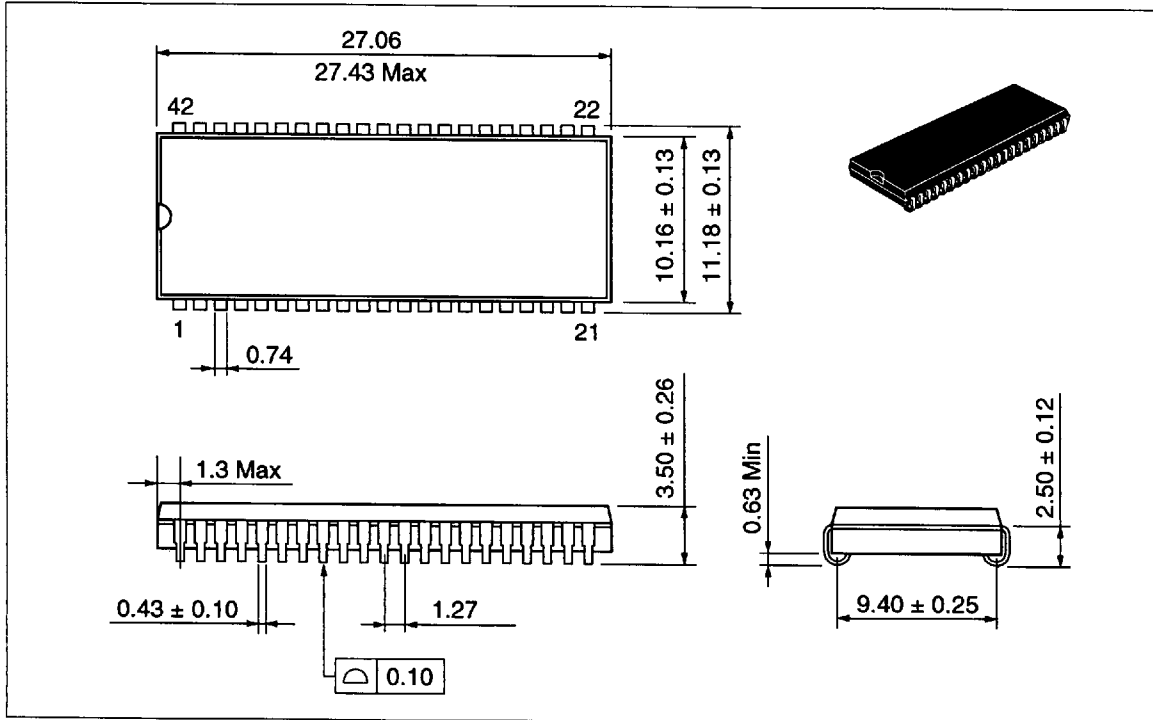
# HM51W16160A Series, HM51W18160A Series

## Package Dimensions

HM51W16160AJ/ALJ Series

HM51W18160AJ/ALJ Series (CP-42D)

Unit: mm



# HM51W16160A Series, HM51W18160A Series

HM51W16160ATT/ALTT Series

HM51W18160ATT/ALTT Series (TTP-50/44DC)

Unit: mm

