PCI EXPRESS/JITTER ATTENUATOR ICS874001I-02

General Description

The ICS874001I-02 is a high performance Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874001I-02 has 2 PLL bandwidth modes: 2.2MHz and 3MHz. The 2.2MHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 3MHz bandwidth provides the best track-ing skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. The 874001I-02 can be set for different modes using the F_SELx pins, as shown in Table 3C.

The ICS874001I-02 uses IDT's 3rd Generation FemtoClock™ PLL technology to achive the lowest possible phase noise. The device is packaged in a small 20-pin TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

Features

- One differential LVDS output pair
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 640MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 50ps (maximum) design target
- 3.3V or 2.5V operating supply
- Two bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

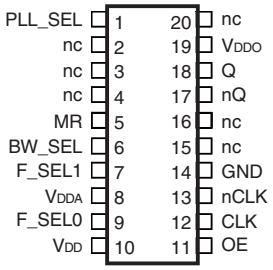
PLL Bandwidth Control Table

BW_SEL
0 = PLL Bandwidth: 2.2MHz (default)
1 = PLL Bandwidth: 3MHz

PLL _SEL Control Table

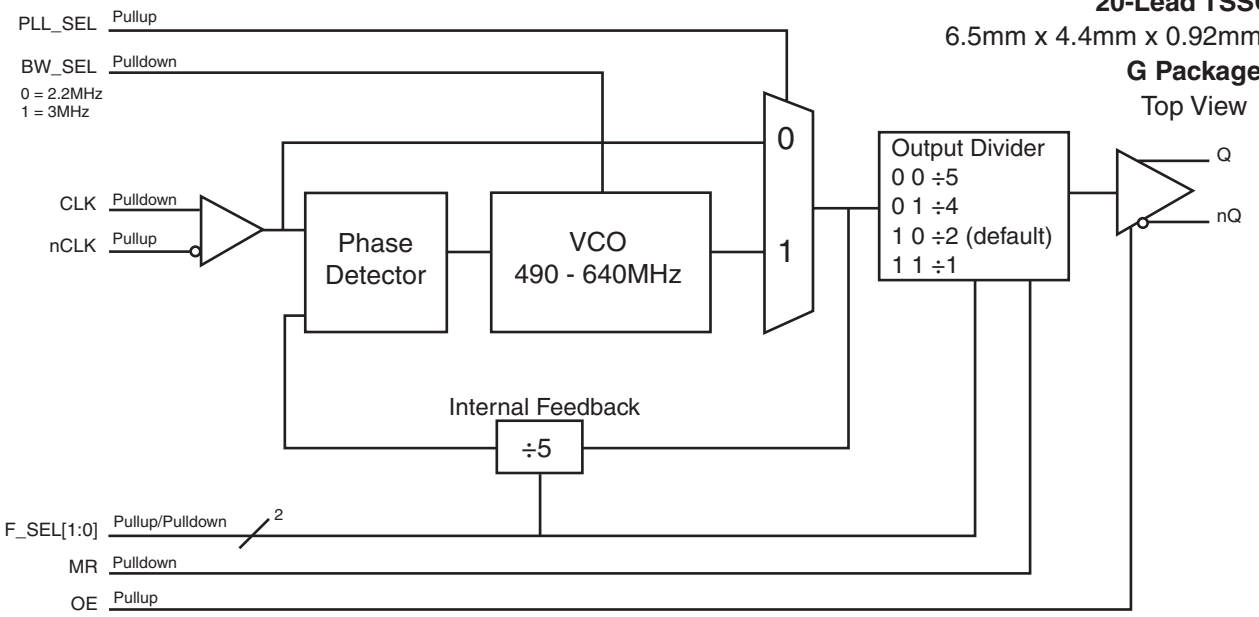
0 = Bypass
1 = VCO (default)

Pin Assignment



ICS874001I-02
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PLL_SEL	Input	Pullup	PLL select pin. When LOW, bypasses or selects VCO. When HIGH selects VCO. LVCMOS/LVTTL interface levels.
2, 3, 4, 15, 16, 20	nc	Unused		No connect.
5	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go LOW and the inverted output nQ to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	BW_SEL	Input	Pulldown	Selects PLL Bandwidth input. LVCMOS/LVTTL interface levels. See Table 3B.
7	F_SEL1	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels. See Table 3C.
8	V_{DDA}	Power		Analog supply pin.
9	F_SEL0	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels. See Table 3C.
10	V_{DD}	Power		Core supply pin.
11	OE	Input	Pullup	Output enable. When HIGH, outputs are enabled. When LOW, forces outputs to HiZ state. LVCMOS/LVTTL interface levels. See Table 3A.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
17, 18	nQ, Q	Output		Differential output pair. LVDS interface levels.
19	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Inputs	Outputs
OE	Q/nQ
0	HiZ
1	Enabled

TABLE 3B. PLL BANDWIDTH CONTROL TABLE

Input	
BW_SEL	PLL Bandwidth
0	2.2MHz (default)
1	3MHz

TABLE 3C. F_SELX FUNCTION TABLE

Input Frequency (MHz)	Inputs			Output Frequency (MHz)
	F_SEL1	F_SEL0	Divider	
100	0	0	5	100
100	0	1	4	125
100	1	0	2	250 (default)
100	1	1	1	500

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			60		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO}	Output Supply Current			20		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			60		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO}	Output Supply Current			20		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$ or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	F_SEL1, OE, PLL_SEL	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
		F_SEL0, MR, BW_SEL	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	F_SEL1, OE, PLL_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		F_SEL0, MR, BW_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

TABLE 4D. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V	5			µA
I_{IL}	Input Low Current	CLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 4E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			425		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.4		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 4F. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			390		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.2		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		640	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter, NOTE 1				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		350		ps
odc	Output Duty Cycle			50		%

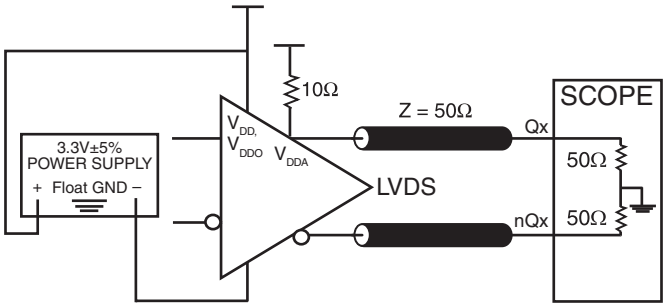
Minimum and maximum values are design target specs.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

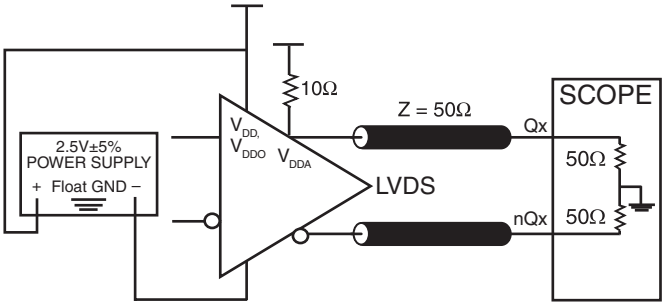
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		640	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter, NOTE 1				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		355		ps
odc	Output Duty Cycle			50		%

Minimum and maximum values are design target specs.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

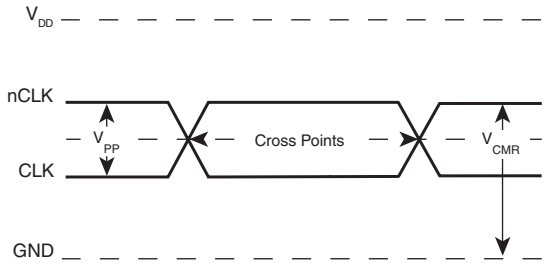
PARAMETER MEASUREMENT INFORMATION



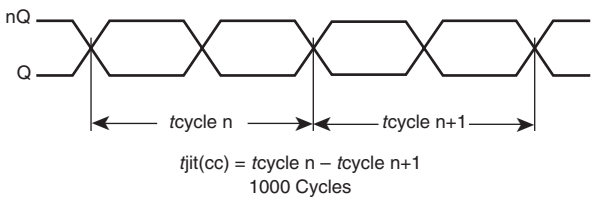
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



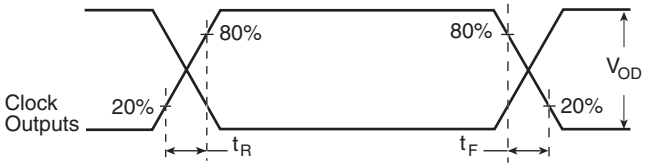
2.5V LVDS OUTPUT LOAD AC TEST CIRCUIT



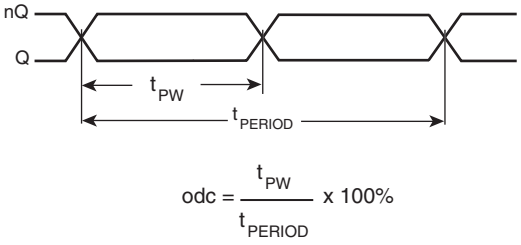
DIFFERENTIAL INPUT LEVEL



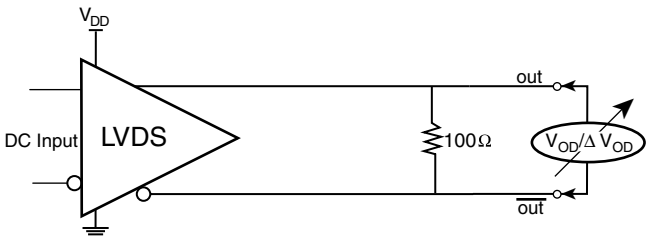
CYCLE-TO-CYCLE JITTER



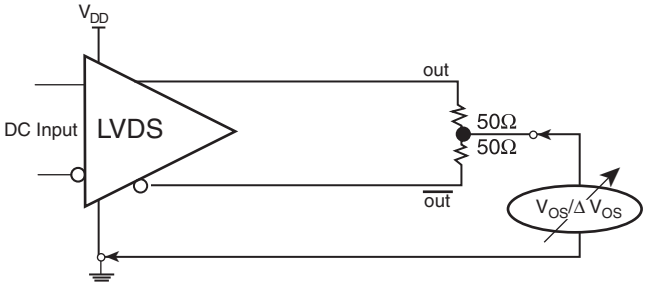
OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS874001I-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

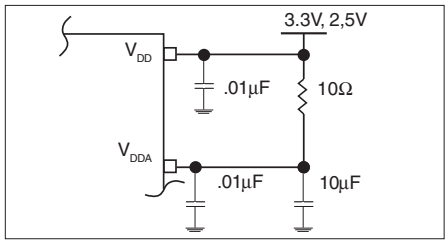


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

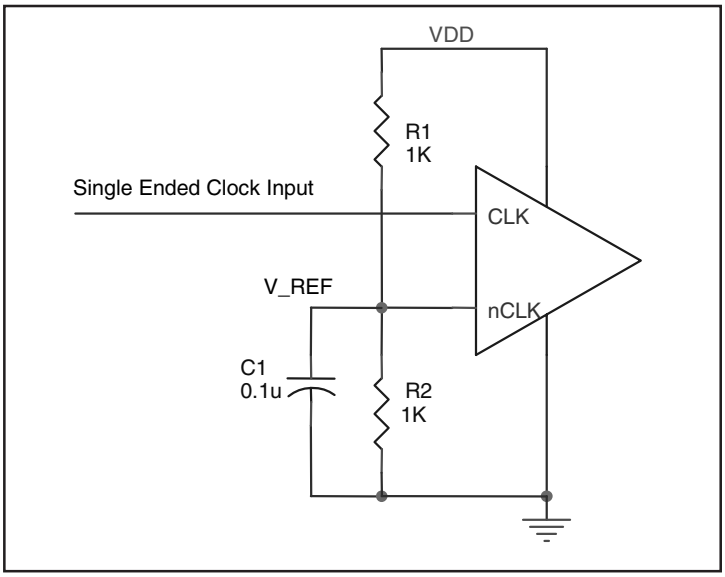


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

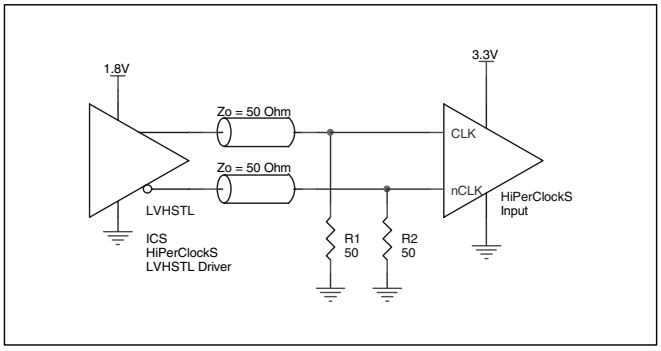


Figure 3A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

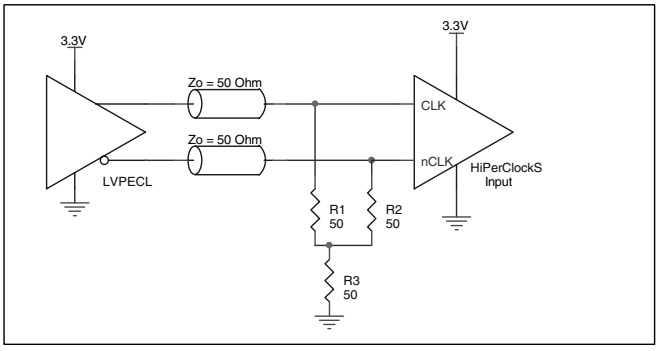


Figure 3B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

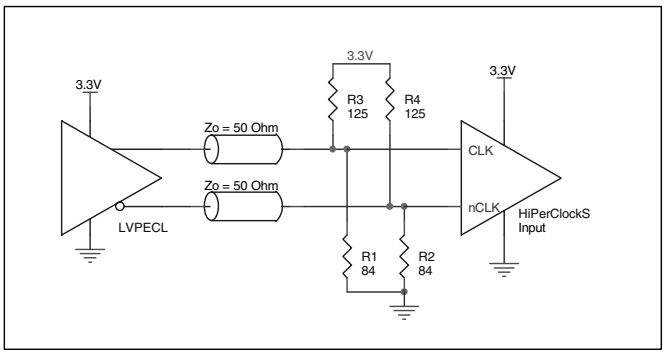


Figure 3C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

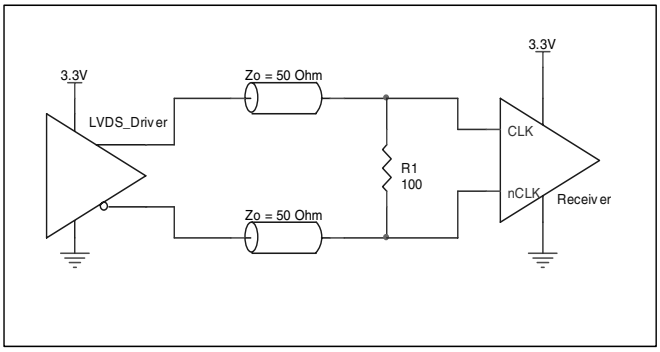


Figure 3D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

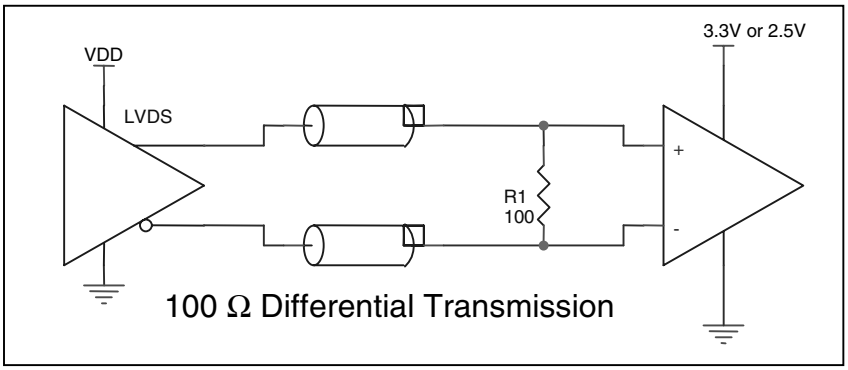


Figure 4. Typical LVDS Driver Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS874001I-02.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS874001I-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (60mA + 10mA) = **242.55mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 20mA = **69.3mW**

Total Power$_{_MAX}$ = 242.55mW + 69.3mW = **311.85mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.312W * 66.6°C/W = 105.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS874001I-02 is: 1608

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

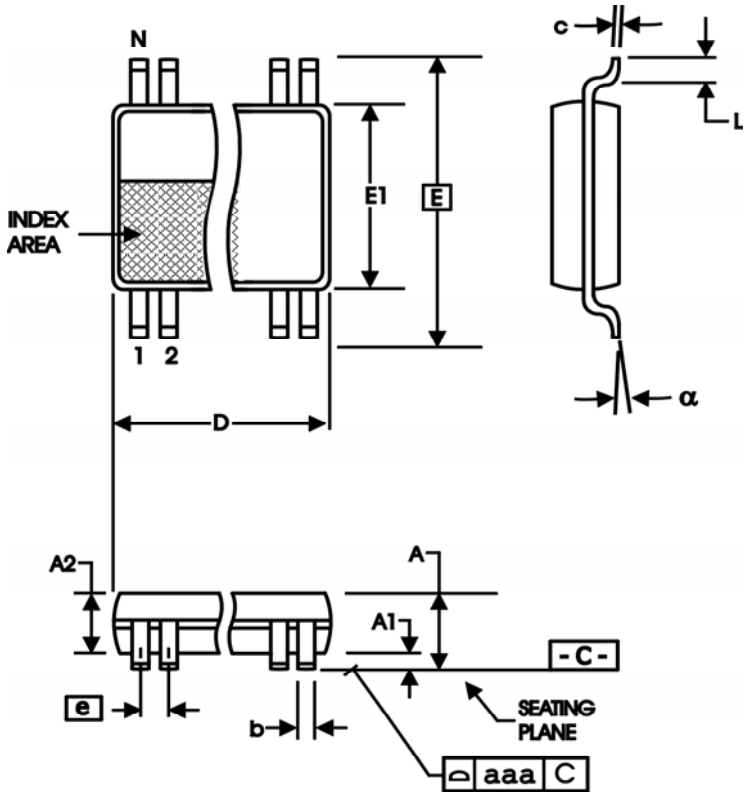


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS874001AGI-02	TBD	20 Lead TSSOP	tube	-40°C to 85°C
ICS874001AGI-02T	TBD	20 Lead TSSSOP	2500 tape & reel	-40°C to 85°C
ICS874001AGI-02LF	ICS4001AI02L	20 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS874001AGI-02LFT	ICS4001AI02L	20 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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