128Kx8 SRAM

*PRELIMINARY **

PLASTIC PLUS™ FEATURES

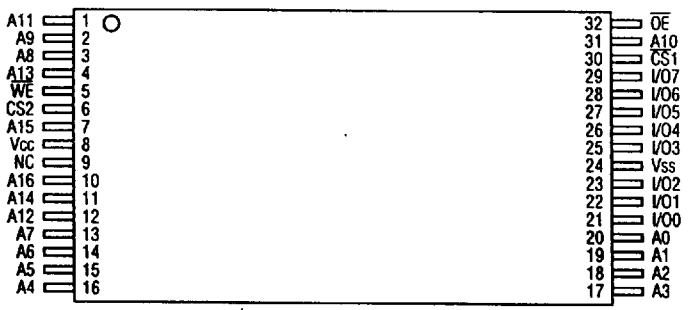
- Access Times 55, 70, 85nS
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard Packages:
  - 32 Pin 600mil Plastic DIP
  - 32 Lead 525mil Plastic SOP
  - 32 Lead TSOP(I) Forward and Reverse
- Electrical and Speed Characteristics for:
  - Military Temperature (-55°C to +125°C)
  - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycle Available
- Organized as 128K x 8
- 5 Volt Power Supply
- Low Power CMOS, 35mW typ.
- Battery Back-Up Operation
- Reliability Test Data Available:
  - High Temperature Operating Life
  - High Temperature Storage
  - Pressure Cooker Test
  - Wet High Temperature Operating Life
  - Thermal Shock
  - Temperature Cycling

* *This data sheet describes a product under development and is subject to change without notice.*

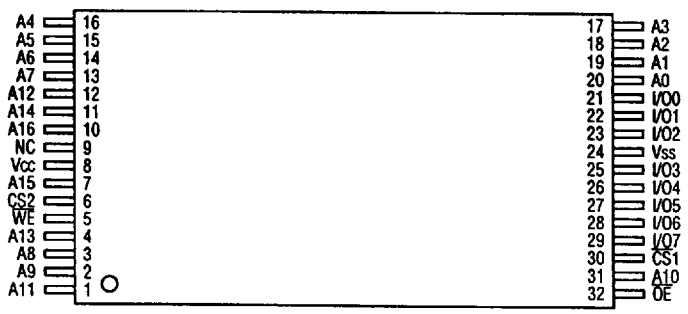
Plastic SRAM

PIN CONFIGURATIONS

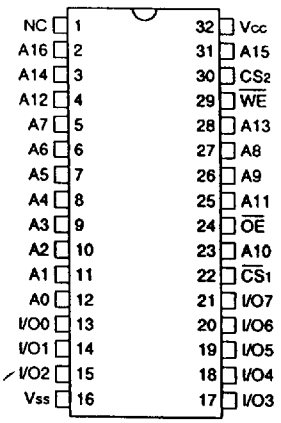
TSOP(I) FORWARD
TOP VIEW



TSOP(I) REVERSE
TOP VIEW



DIP
SOP
TOP VIEW



PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS_1}$ - CS_2	Chip Selects
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC} + 0.5	V
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	VccCurrent
H	X	X	X	Power Down	High-Z	I_{SB}, I_{SBL}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SBL}
L	H	H	H	Out Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	6	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	8	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS_1}$ = V_{IH}, CS_2 = V_{IL}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		30	mA
Standby Current	I_{SB}	$\overline{CS_1}$ = V_{IH}, CS_2 = $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		0.25	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		V

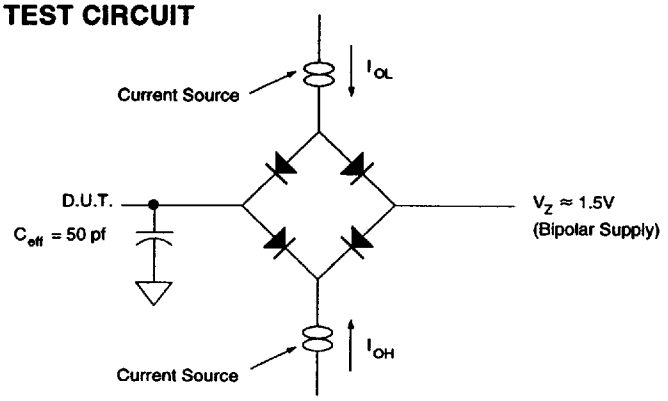
NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} -0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS_1}$ Controlled: $\overline{CS_1} \geq V_{CC}$ - 0.2V, $CS_2 \geq V_{CC}$ - 0.2V CS_2 Controlled: $CS_2 \leq$ 0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR}	V_{CC} = 3V		3	180	µA

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	-55		-70		-85		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		85		nS
Address Access Time	t_{AA}		55		70		85	nS
Output Hold from Address Change	t_{OH}	5		5		5		nS
Chip Select Access Time	t_{ACS}		55		70		85	nS
Output Enable to Output Valid	t_{OE}		25		35		45	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	10		10		10		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}[1]		20		25		30	nS
Output Disable to Output in High Z	t_{OHZ}[1]		20		25		30	nS

1. This parameter is guaranteed by design but not tested.

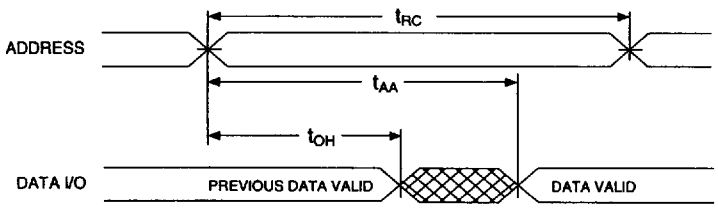
AC CHARACTERISTICS

(VCC = 5.0V, TA = -55°C to +125°C)

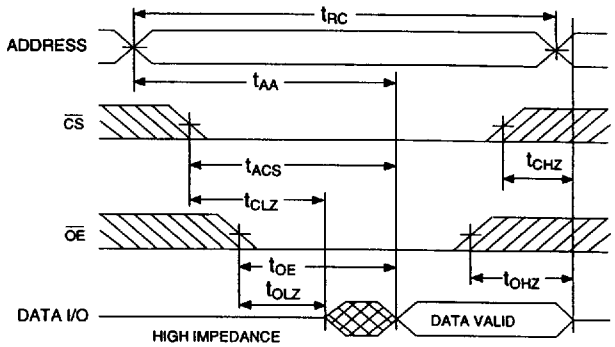
Parameter Write Cycle	Symbol	-55		-70		-85		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		nS
Chip Select to End of Write	t_{CW}	45		60		70		nS
Address Valid to End of Write	t_{AW}	50		60		70		nS
Data Valid to End of Write	t_{DW}	25		30		35		nS
Write Pulse Width	t_{WP}	40		50		55		nS
Address Setup Time	t_{AS}	0		0		0		nS
Address Hold Time	t_{AH}	0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}[1]		20		25		30	nS
Data Hold Time	t_{DH}	0		0		0		nS

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM - READ CYCLE

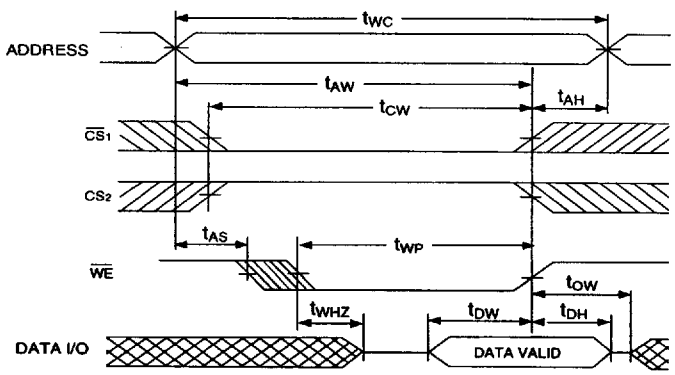


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



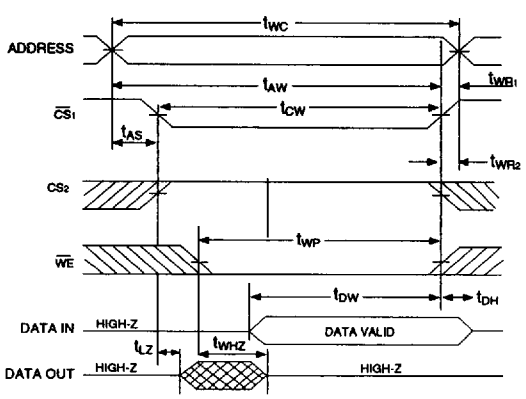
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE 1

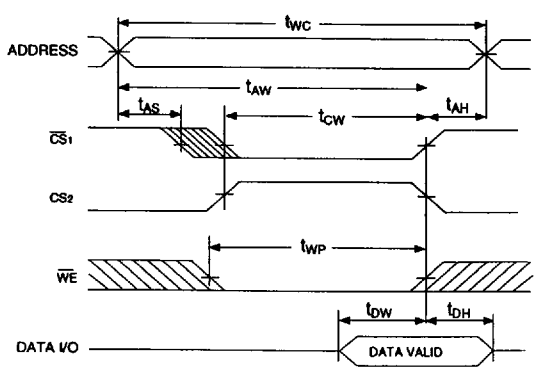


WRITE CYCLE 1 $\overline{WE}$ CONTROLLED

WRITE CYCLES 2 & 3

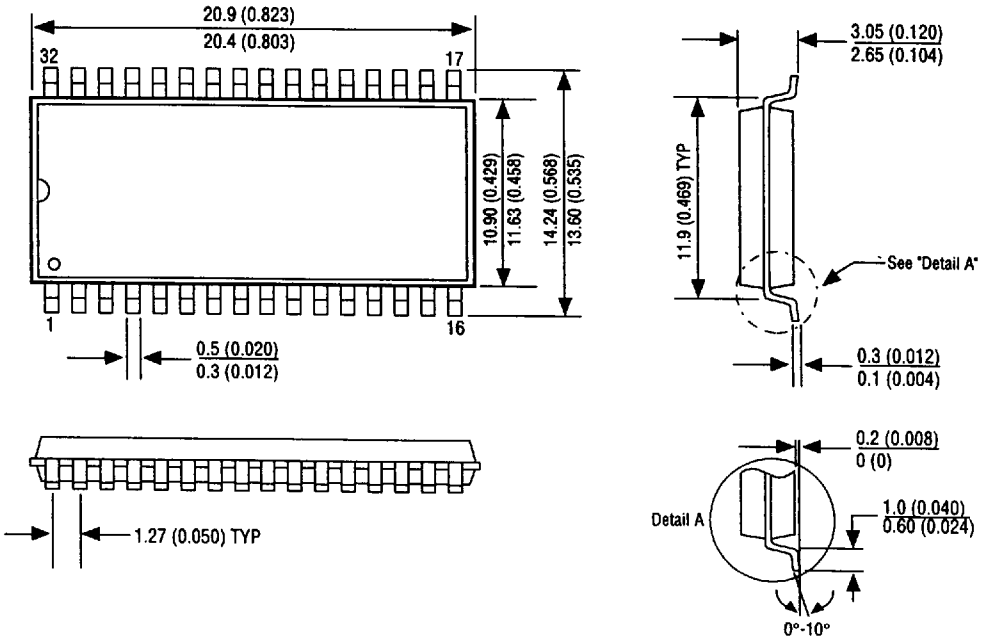


WRITE CYCLE 2, $\overline{CS_1}$ CONTROLLED



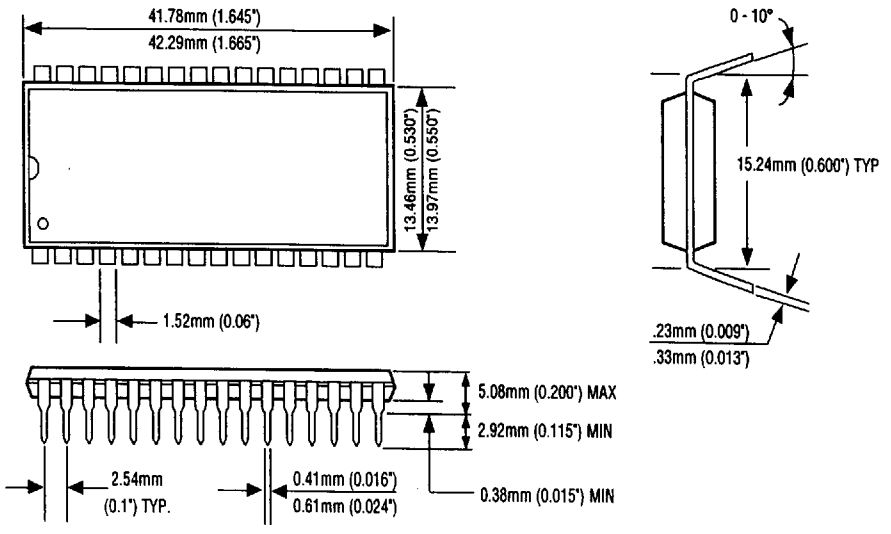
WRITE CYCLE 3, $\overline{CS_2}$ CONTROLLED

32 LEAD, PLASTIC SOP (525 mil) PACKAGE DIMENSION

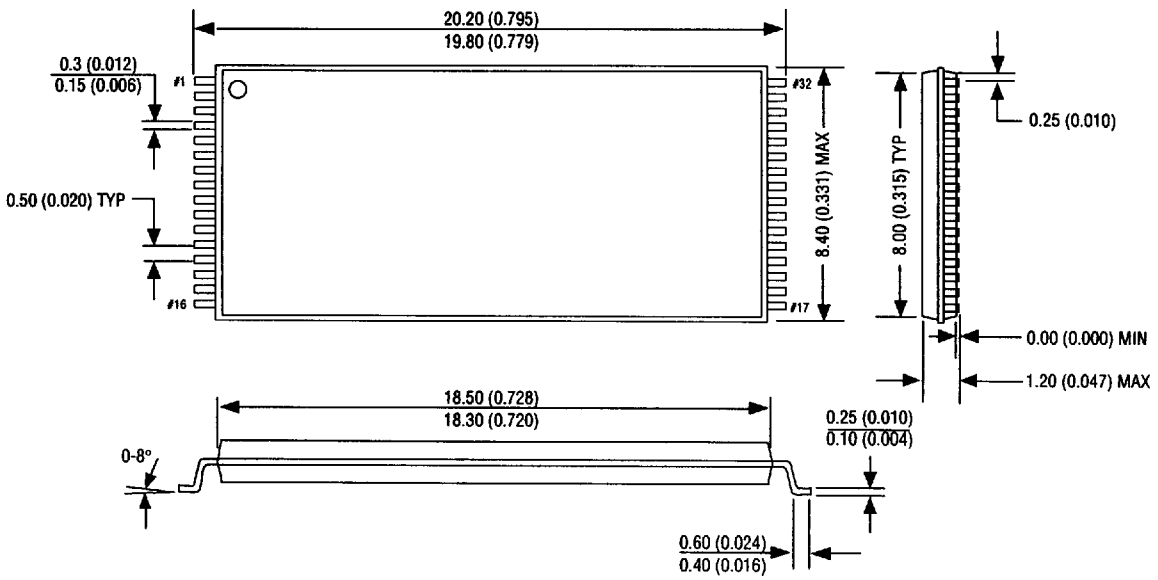


DIMENSIONS IN MILLIMETERS AND (INCHES)

32 PIN, PLASTIC DIP PACKAGE DIMENSION

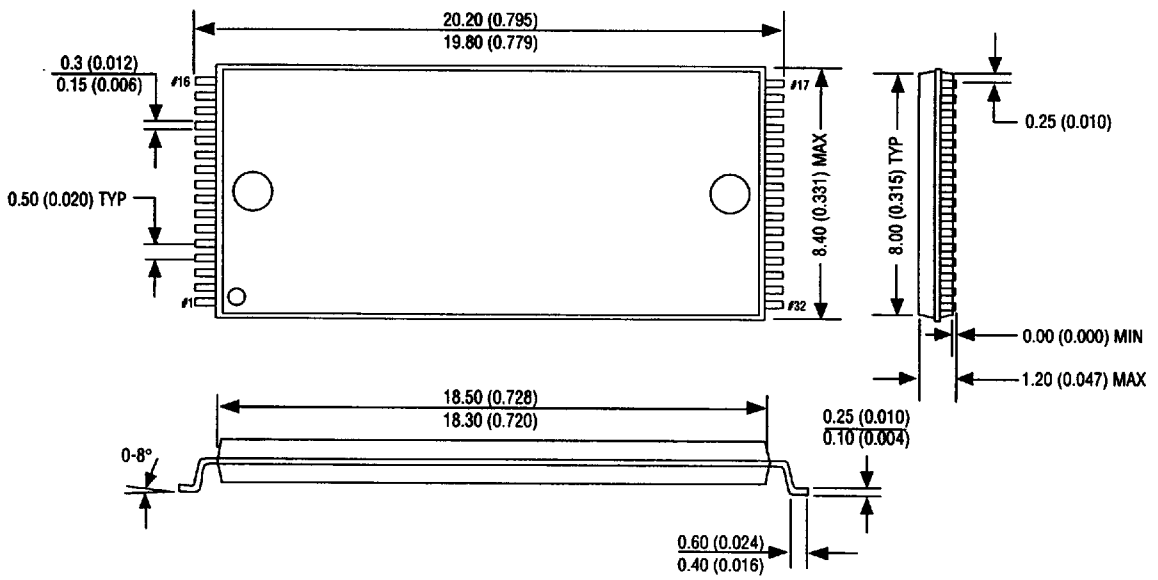


32 LEAD, PLASTIC TSOP I FORWARD PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, PLASTIC TSOP I REVERSE PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION