Q-TECH CORPORATION

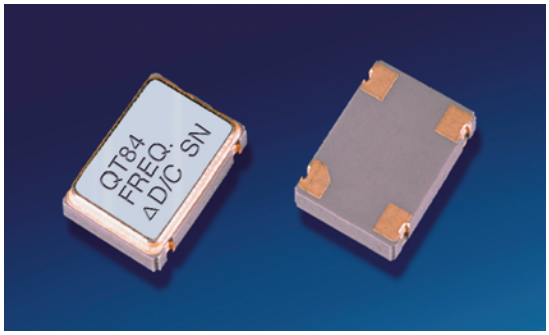
LOW PROFILE QT84

MINIATURE SMD CRYSTAL OSCILLATORS

1.8 to 5.0Vdc - 500kHz to 160MHz

Description

Q-Tech's surface mount 7 x 5 mm oscillator series consist of an IC 5Vdc, 3.3Vdc, 2.5Vdc, 1.8Vdc clock square wave generator and a miniature strip AT quartz crystal built in a low profile ceramic package with gold plated contact pads. This is the smallest package Q-Tech has ever offered for High Reliability applications.



Features

- Made in the USA
- ECCN: EAR99
- Broad frequency range from 500kHz to 160MHz
- Small footprint
- LVHCMOS, HCMOS, and TTL compatible
- 5.0Vdc, 3.3Vdc, 2.5Vdc, 1.8Vdc supply
- Able to meet 36000G shock, half sine, 0.5ms
- Wide operating temperature range
- Tri-State Output (Option D)
- Hermetically sealed ceramic package
- Fundamental and 3rd Overtone designs
- Full or partial military screening tests available
- Tape and reel packaging
- Lead free tinning available

Ordering Information

(Sample part number)

QT84HCD10M-50.000MHz

Q	T	84	HC	D	10	M	-	50.000MHz

Solder Dip Option:
T = Standard
S = Solder Dip (*)
G = Solder Dip (*)

Package

Logic & Supply Voltage:
HC = HCMOS +5.0V
L = LVHCMOS +3.3V
N = LVHCMOS +2.5V
R = LVHCMOS +1.8V
See notes (**)

Tristate Option:
Blank = No Tristate
D = Tristate

Output Frequency

Screening Option:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

Frequency vs. Temperature Code:

7	= ± 75ppm	at	-55ºC	to +125ºC
10	= ± 100ppm	at	-55ºC	to +125ºC
11	= ± 50ppm	at	-40ºC	to +85ºC
17	= ± 75ppm	at	-60ºC	to +125ºC
18	= ± 100ppm	at	-60ºC	to +125ºC

See notes (**)

Available for temperatures up to +200ºC with Q-Tech MCM number.

(*) Hot Solder Dip options for an additional cost:

S = Sn60/Pb40 per MIL-PRF 55310

G = Lead free Alloy SAC305 (96.5% Sn, 3% Ag, 0.5% Cu)

(**) Notes

- Supply voltage, frequency stability vs. temperature codes may not be available in all frequencies.
- For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Applications

- Designed to meet today's requirements for low voltage applications
- High shock applications
- Gun launched munitions and systems
- Smart munitions
- Instrumentation
- Navigation
- Avionics
- Microprocessor clock

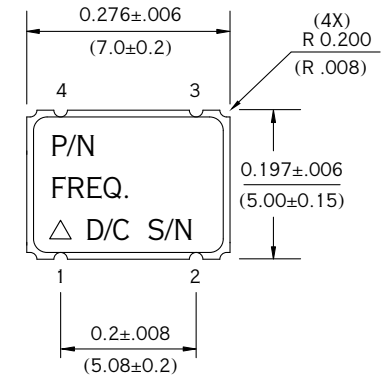
Specifications subject to change without prior notice.

Electrical Characteristics

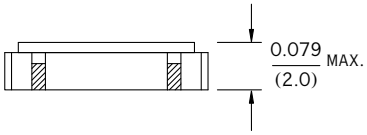
Parameters	HC	L	N	R
Output frequency range (Fo)	**500kHz — 50.000MHz**	**500kHz — 160.000MHz**	**500kHz — 133.000MHz**	**500kHz — 100.000MHz**
Supply voltage (Vdd)	5.0Vdc ± 10%	3.3Vdc ± 10%	2.5Vdc ± 10%	1.8Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	7.0Vdc	5.0Vdc		
Frequency stability (ΔF/ΔT)	See Option codes			
Operating temperature (Topr)	See Option codes			
Storage temperature (Tsto)	-62ºC to + 125ºC			
Operating supply current (Idd) (No Load)	20 mA max. - 500kHz ~ < 16MHz 25 mA max. - 16MHz ~ < 32MHz 35 mA max. - 32MHz ~ < 50MHz	6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ < 130MHz 50 mA max. - 130MHz ~ ≤160MHz	6 mA max. - 500kHz ~ < 40MHz 15 mA max. - 40MHz ~ < 60MHz 25 mA max. - 60MHz ~ < 85MHz 35 mA max. - 85MHz ~ ≤ 133MHz	4 mA max. - 500kHz ~ < 40MHz 10 mA max. - 40MHz ~ < 50MHz 20 mA max. - 50MHz ~ < 85MHz 25 mA max. - 85MHz ~ ≤ 100MHz
Symmetry (50% of ouput waveform or 1.4Vdc for TTL)	45/55% max. - 500kHz ~ < 21MHz 40/60% max. - 21 ~ ≤ 50MHz	45/55% max. - 500kHz ~ < 21MHz 40/60% max. - 21 ~ ≤ 160MHz	45/55% max. - 500kHz ~ < 21MHz 40/60% max. - 21 ~ ≤ 133MHz	45/55% max. - 500kHz~ < 21MHz 40/60% max. - 21 ~ ≤ 100MHz
Rise and Fall times (with typical load)	6ns max. - Fo < 40MHz 3ns max. - Fo ≥ 40 - 50MHz (between 10% to 90%)	6ns max. - 500kHz ~ < 40MHz 3ns max. - 40 ~ ≤ 160MHz (between 10% to 90%)	5ns max. - 500kHz ~ < 40MHz 3ns max. - 40 ~ ≤ 133MHz (between 10% to 90%)	5ns max. - 500kHz ~ < 40MHz 3ns max. - 40 ~ ≤ 100MHz (between 10% to 90%)
Output Load	**15pF // 10kohms** 50pF max. or 10TTL	**15pF // 10kohms** (30pF max. for F ≤ 50MHz)	**15pF // 10kohms**	
Start-up time (Tstup)	10ms max.			
Output voltage (Voh/Vol)	0.9 x Vdd min.; 0.1 x Vdd max.	0.9 x Vdd min.; 0.1 x Vdd max.		
Output Current (Ioh/Iol)	± 24mA max.	± 4mA max.		
Enable/Disable Tristate function Pin 1	VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance		VIH ≥ 0.7 x Vdd Oscillation; VIL ≤ 0.3 x Vdd High Impedance	
Jitter RMS 1σ (at 25ºC)	See Page 5			
Aging (at 70ºC)	± 5ppm max. first year / ± 2ppm max. per year thereafter			

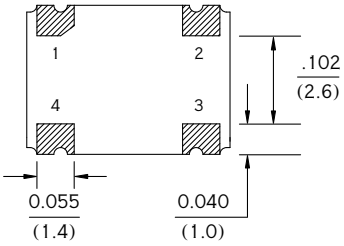
Package Outline and Pin Connections

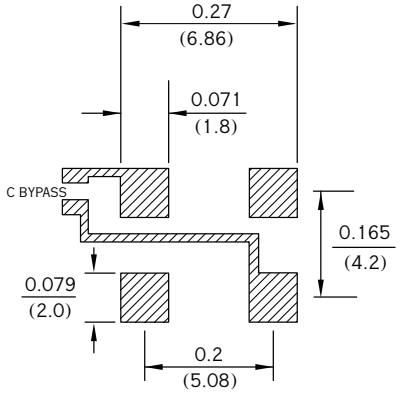
Dimensions are in inches (mm)



Pin No.	Function
1	TRISTATE or N/C
2	GND/CASE
3	OUTPUT
4	VDD







An external bypass capacitor 0.01µF is required between Vdd and GND

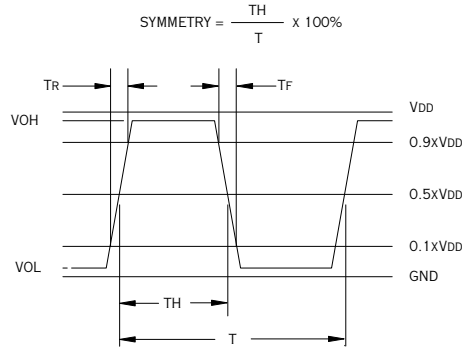
Package Information

- Package material: 91% AL_2O_3
- Weight: .15g typ., 2g max.
- Termination pads (4x): Tungsten
- Termination finish: Nickel Underplate: 100µ ~ 250µ inches
  Gold Plated: 50µ ~ 80µ inches
  Hot Solder Dip Sn60/Pb40 Finish (optional per P.O)
  Lead Free Tinning (SAC305) finish (optional per P.O)

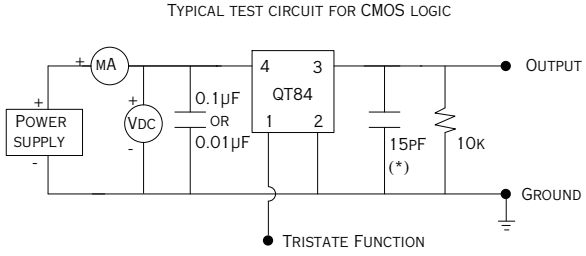
Marking Information

Line 1: P/N (QT84L9M)
Line 2: Frequency (500.000K)
Line 3: ESD Symbol + D/C (YYWW) + S/N

Output Waveform (Typical)

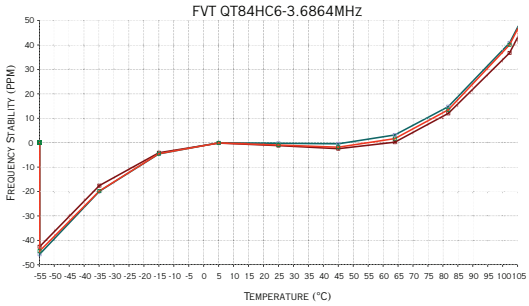


Test Circuit

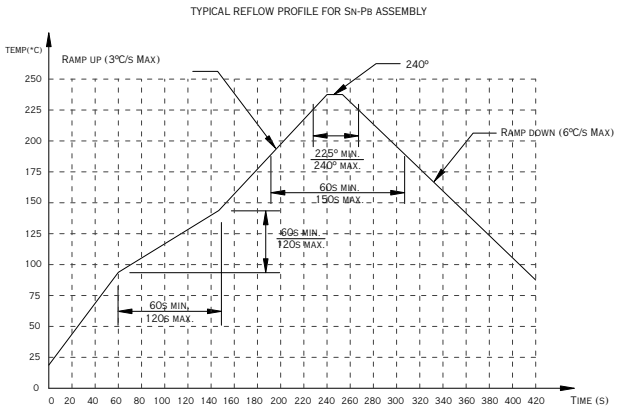


The Tristate function on pin 1 has a built-in pull-up resistor so it can be left floating or tied to Vdd without deteriorating the electrical performance.

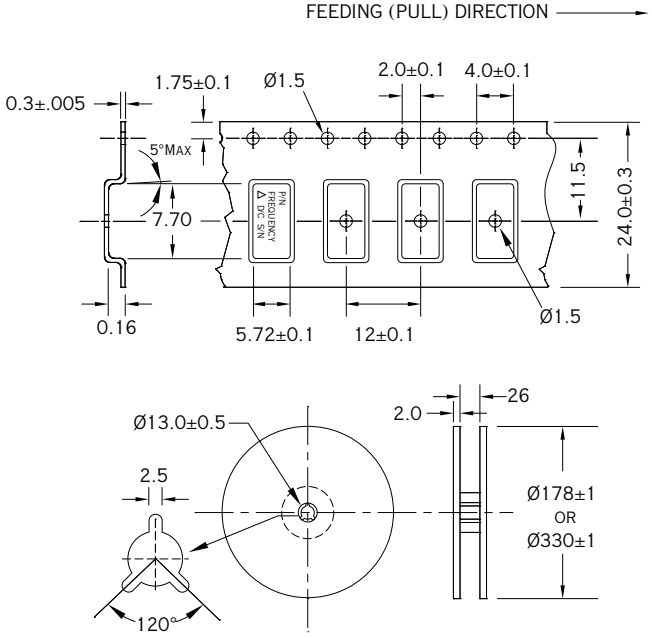
Frequency vs. Temperature Curve



Reflow Profile



Embossed Tape and Reel Information for QT84



Dimensions are in mm. Tape is compliant to EIA-481-A.

Reel size (Diameter in mm)	Qty per reel (pcs)
178	1,000

Environmental and Mechanical Specifications

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Resistance to solder heat	MIL-STD-202, Method 210, Cond. B
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1 HBM 0 to 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

Jitter And Phase Noise

As data rate increases, effect of jitter becomes critical with its budget tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random jitter (RJ) and deterministic jitter (DJ) components.
Random Jitter (RJ) is theoretically unbounded and Gaussian in distribution, while Deterministic Jitter (DJ) is bounded and does not follow any predictable distribution.

Q-Tech utilizes the EZJIT Plus jitter analysis software with Noise reduction software that supports Agilent Infinium real-time oscilloscope. Measure at its maximum sampling rate 40Gs/s and memory depth, we can separate the signal's aggregate total jitter into Random Jitter (RJ) and Deterministic Jitter (DJ).

Since Random Jitter is unbounded and Gaussian in style, the Total Jitter is a function of Bit Error Rate (BER).

TJ = RJ + DJ

Where:

RJ = RJ(rms) x 2α + DJ(p-p)

BER	α
10E-3	3.1
10E-6	4.75
10E-9	6
10E-12	7.0

Typical Jitter at BER=10E-12

Frequency	DJ (p-p) ps	RJ (rms) ps	TJ ps
16MHz (5.0V)	2.7	3.6	54.3
32MHz (3.3V)	1.97	1.13	18.1
40MHz (3.3V)	2.2	1.14	18.5
50MHz (5.0V)	1.65	1.18	18.4
100MHz (3.3V)	1.25	0.95	14.8
125MHz (3.3V)	1.15	0.96	14.9

Figure 1: Jitter Analysis of a QT84LD-40MHZ

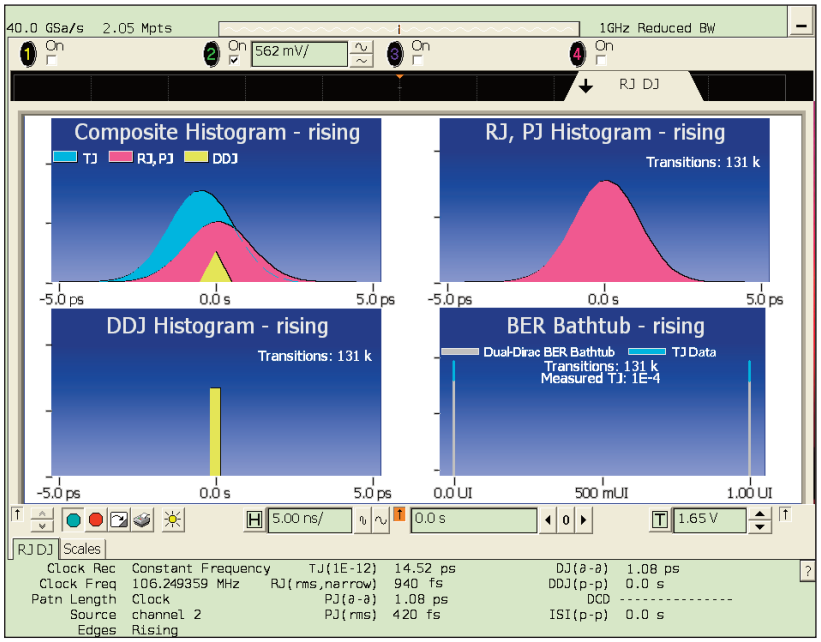


Figure 2: Jitter Analysis of a QT84L-106.25MHZ

Typical Phase Noise

Frequency	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	Phase Jitter (ps) *
16MHz	-91	-122	-147	-158	-162	-166	0.79
32MHz	-77	-109	-133	-141	-145	-153	0.33
40MHz	-79	-110	-130	-141	-145	-152	0.31
125MHz	-74	-106	-133	-141	-146	-153	0.15

Phase Noise and Phase Jitter Integration

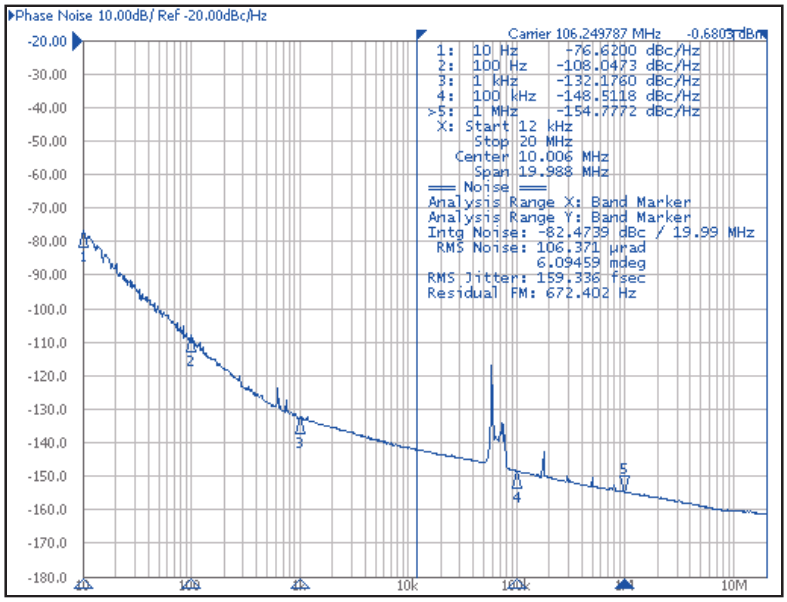
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

Symbol	Definition
$\int \mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi(f)=(180/\Pi)x\sqrt{2\int \mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = Sφ (f)/(fosc.360°)	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT84L11, 3.3Vdc, 106.25MHz clock at offset frequencies 10Hz to 1MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



QT84L11, 3.3Vdc, 106.25MHz

Revision History

ECO	REV	REVISION SUMMARY	Page
10452	E	Change date code marking format to YYWW (year/week) Corrected landing pattern dimensions	3
10623	F	Add Solder Dip option G	1
		Modified Package Material From 90% AL2O3 to 91% AL_2O_3	3
10720	G	Features: Modified 36000G shock to half sine, 0.5ms Ordering Information: Added Frequency vs. Temperature code 17 & 18	1
		Change Rise and Fall Time from 30MHz to 40MHz	2