MOTOROLA

Military 54F27

Advance Information

Triple 3-Input NOR Gate

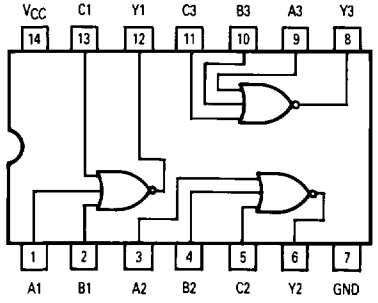
ELECTRICALLY TESTED PER:
MPG54F27

AVAILABLE AS:

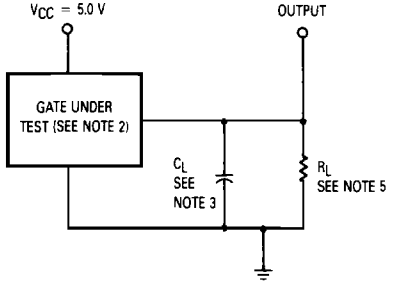
1) JAN: *
2) SMD: *
3) 883C: *

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



AC TEST CIRCUIT



NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR = 1.0 MHz and duty cycle = 50%.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 499\ \Omega \pm 5.0\%$.
6. The outputs are measured one at a time with one transition per measurement.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
A1	1	1	2	GND
B1	2	2	3	GND
A2	3	3	4	GND
B2	4	4	6	GND
C2	5	5	8	GND
Y2	6	6	9	V_{CC}
GND	7	7	10	GND
Y3	8	8	12	V_{CC}
A3	9	9	13	GND
B3	10	10	14	GND
C3	11	11	16	GND
Y1	12	12	18	V_{CC}
C1	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs			Output
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant

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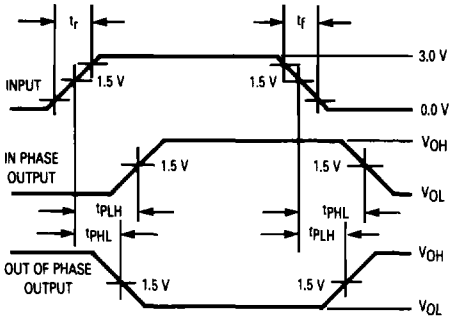
This document contains information on a new product. Specifications and information herein are subject to change without notice.

WAVEFORMS


t_r
t_f
3.0 V
INPUT
1.5 V
1.5 V
0.0 V
V_{OH}
IN PHASE OUTPUT
1.5 V
1.5 V
V_{OL}
t_{PLH}
t_{PHL}
t_{PHL}
t_{PLH}
V_{OH}
OUT OF PHASE OUTPUT
1.5 V
1.5 V
V_{OL}

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{OUT} = 0 V.
I_{CCH}	Power Supply Current		5.5		5.5		5.5	mA	V_{CC} = 5.5 V, V_{IN} = 0 V.
I_{CCL}	Power Supply Current		12		12		12	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs = 0 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay /Data-Output A or B to Y	1.0	4.5	1.0	5.5	1.0	5.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH}	Propagation Delay /Data-Output A or B to Y	1.2	5.0	1.0	6.0	1.0	6.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

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