

	<h1>Tentative</h1>	<b>DRA4144W</b>	
		Total pages	page

# DRA4144W

Silicon PNP epitaxial planar type

For digital circuits

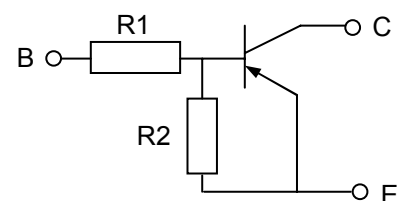
Marking Symbol : LK

Package Code : NS-B1-B-B

## Absolute Maximum Ratings $T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	VCBO	-50	V
Collector-emitter voltage (Base open)	VCEO	-50	V
Collector current	IC	-100	mA
Total power dissipation	PT	300	mW
Junction temperature	Tj	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

## Internal Connection



Resistance value	R1	47	k $\Omega$
	R2	22	k $\Omega$
Pin name	1.	Emitter	
	2.	Collector	
	3.	Base	

## Electrical Characteristics $T_a = 25\text{ }^\circ\text{C} \pm 3\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	VCBO	IC = -10 $\mu\text{A}$ , IE = 0	-50			V
Collector-emitter voltage (Base open)	VCEO	IC = -2 mA, IB = 0	-50			V
Collector-base cutoff current (Emitter open)	ICBO	VCB = -50 V, IE = 0			-0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	ICEO	VCE = -50 V, IB = 0			-0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	IEBO	VEB = -6 V, IC = 0			-0.2	mA
Forward current transfer ratio	hFE	VCE = -10 V, IC = -5 mA	60			-
Collector-emitter saturation voltage	VCE(sat)	IC = -10 mA, IB = -0.5 mA			-0.25	V
Input voltage	Vi(on)	VCE = -0.2 V, IC = -5 mA	-4.4			V
	Vi(off)	VCE = -5 V, IC = -100 $\mu\text{A}$			-1.2	V
Input resistance	R1		-30%	47	+30%	k $\Omega$
Resistance ratio	R1/R2		1.70	2.14	2.60	-

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

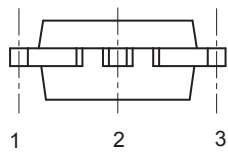
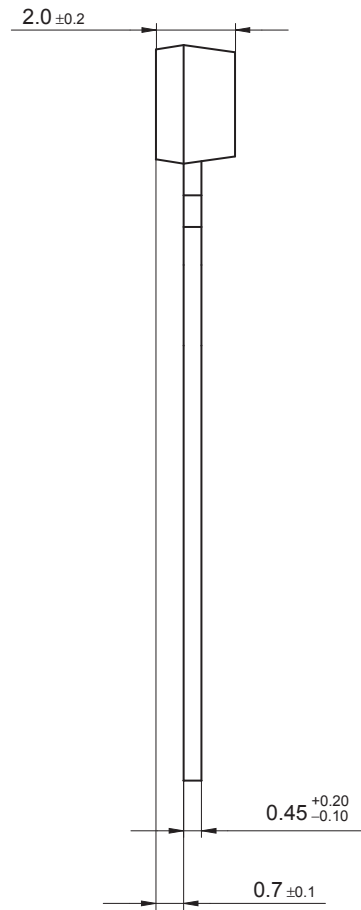
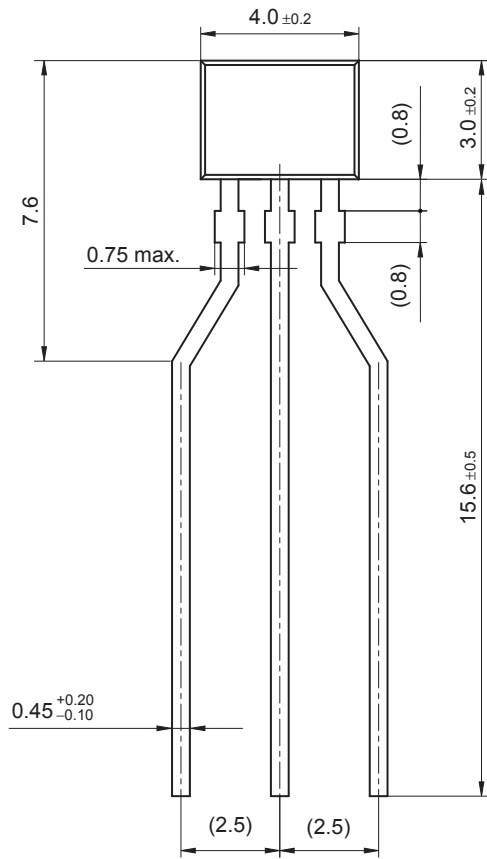
## Packing

Radial type : 5 000 pcs / carton

2010.2.22	2010.9.1	
Prepared	Revised	

NS-B1-B-B

Unit: mm



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