First-in First-out (FIFO) 4K x 9 CMOS Memory

FEATURES

- First-in, First-out dual port memory
  - 4K x 9 organization
- Very high speed independent of depth/width
  - 25ns cycle times
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or width
- Low power consumption
  - Active: 150mA (max)
  - Power Down: 15mA (max)
- Half-full flag capability in standalone mode
- Empty and full warning flags
- Auto retransmit capability in standalone mode
- High performance 1.2 micron CMOS technology
- Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC

DESCRIPTION

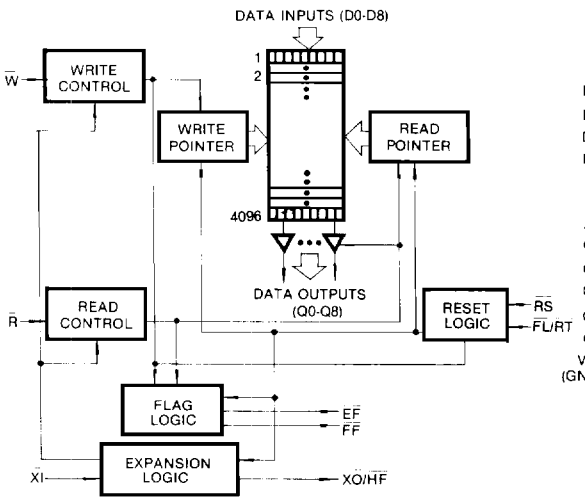
The KM75C04A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

No address information is required for KM75C04A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 25nsec (40MHz).

The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

The KM75C04A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)