



Features

- Automatic power-down when deselected
- Output Enable (\overline{OE}) feature (7C166)
- CMOS for optimum speed/power
- High speed
– 15 ns t_{AA}
- Low active power
– 633 mW
- Low standby power
– 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and three-state drivers. The CY7C166 has an active low output enable (\overline{OE}) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the chip enable (\overline{CE}) and write enable (\overline{WE}) inputs are both LOW (and the output enable (\overline{OE}) is LOW for the 7C166). Data

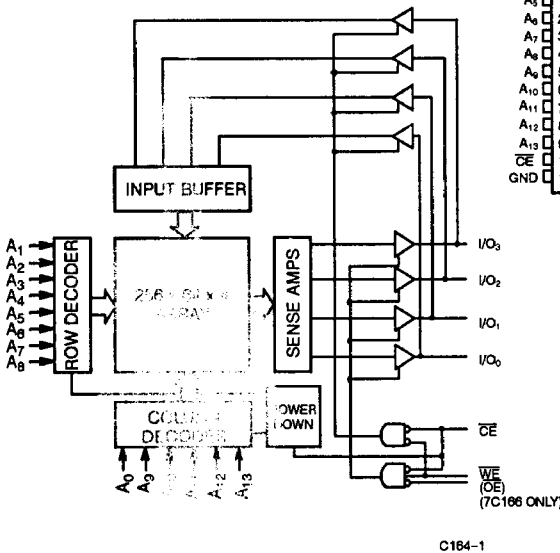
on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable (\overline{CE}) LOW (and \overline{OE} LOW for 7C166), while write enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

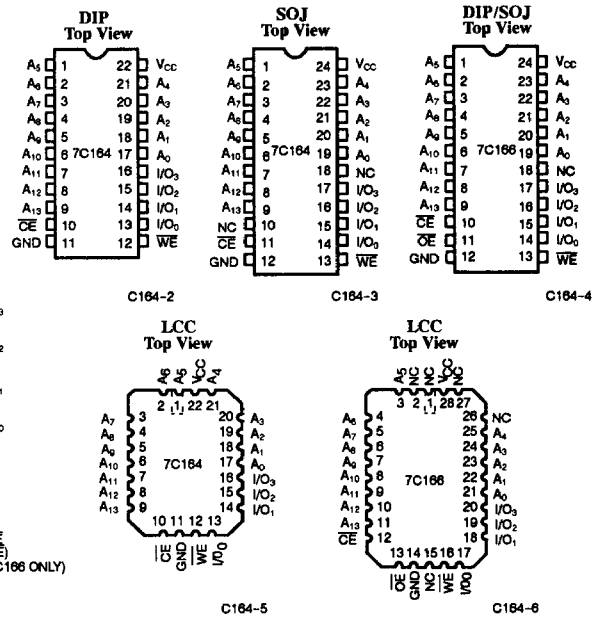
The I/O pins stay in high-impedance state when chip enable (\overline{CE}) is HIGH, or write enable (\overline{OE}) is HIGH for 7C166). A die coat is used to insure alpha immunity.

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Logic Block Diagram



Pin Configurations



Selection Guide

	7C164-15 7C166-15	7C164-20 7C166-20	7C164-25 7C166-25	7C164-35 7C166-35	7C164-45 7C166-45
Maximum Access Time (ns)	15	20	25	35	45
Maximum Operating Current (mA)	115	80	70	70	50
Maximum Standby Current (mA)	40/20	40/20	20/20	20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
Output Current into Outputs (Low)	20 mA

Static Discharge Voltage	> 2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C164-15 7C166-15		7C164-20 7C166-20		7C164-25,35 7C166-25,35		7C164-45 7C166-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		-3.0	0.8	-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[2]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		115		80		70		50	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current ^[3]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		40		20		20	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current ^[3]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20		20	mA

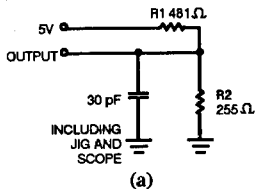
Capacitance^[4]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	5	pF
C _{OUT}	Output Capacitance		7	pF

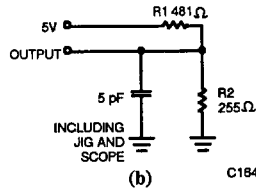
Notes:

- V_{IL} min. = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

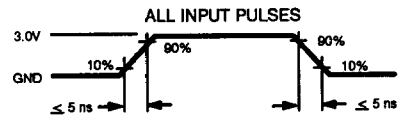


(a)



(b)

C184-7



Equivalent to: THEVENIN EQUIVALENT
 OUTPUT ——— 187Ω ——— 1.73V

C184-8

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Switching Characteristics Over the Operating Range^[5]

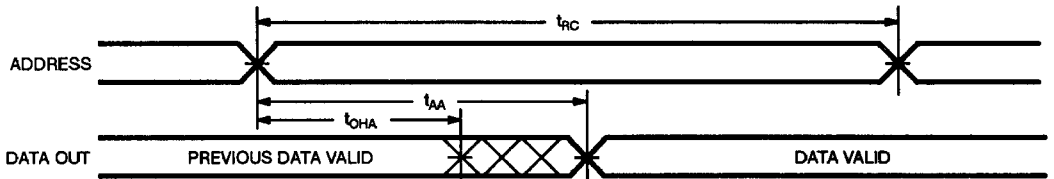
Parameters	Description	7C164-15 7C166-15		7C164-20 7C166-20		7C164-25 7C166-25		7C164-35 7C166-35		7C164-45 7C166-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		5		5		5		5		ns
t_{ACE}	\overline{CE} LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	\overline{OE} LOW to Data Valid	7C166	10		10		12		15		20	ns
t_{LZOE}	\overline{OE} LOW to Low Z	7C166	3		3		3		3		3	ns
t_{HZOE}	\overline{OE} HIGH to High Z	7C166	8		8		10		12		15	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]		3		5		5		5		5	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[6,7]		8		8		10		15		15	ns
t_{PU}	\overline{CE} LOW to Power-Up		0		0		0		0		0	ns
t_{PD}	\overline{CE} HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE^[8]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	\overline{CE} LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]		5		5		5		5		5	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6,7]		7		7		7		10		15	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) in AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

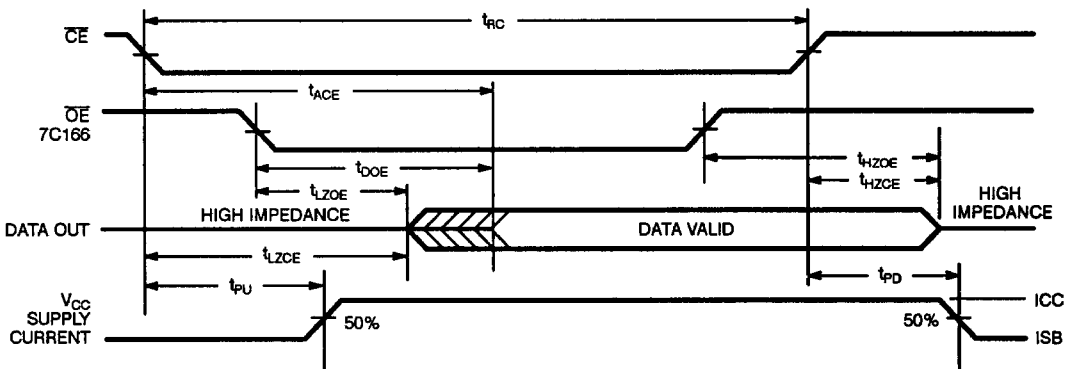
Switching Waveforms

Read Cycle No. 1^[9, 10]



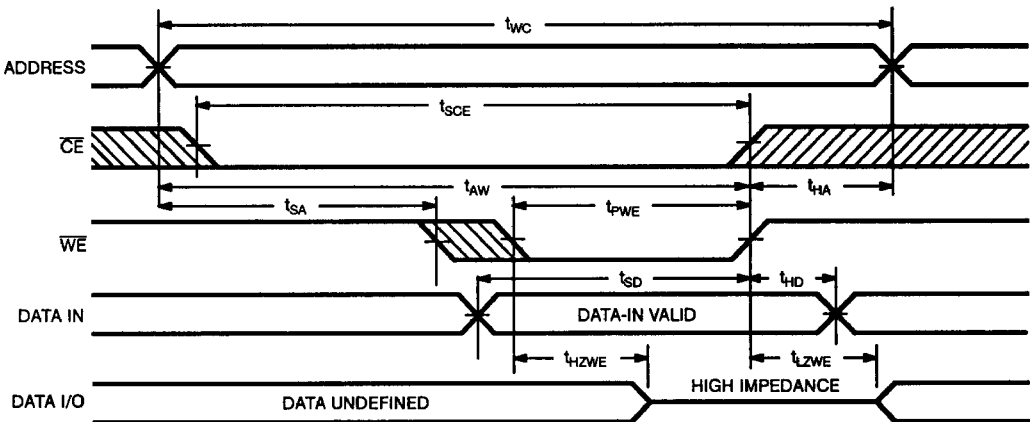
C164-9

Read Cycle No. 2^[9, 11]



C164-10

Write Cycle No. 1 (\overline{WE} Controlled)^[8, 12]



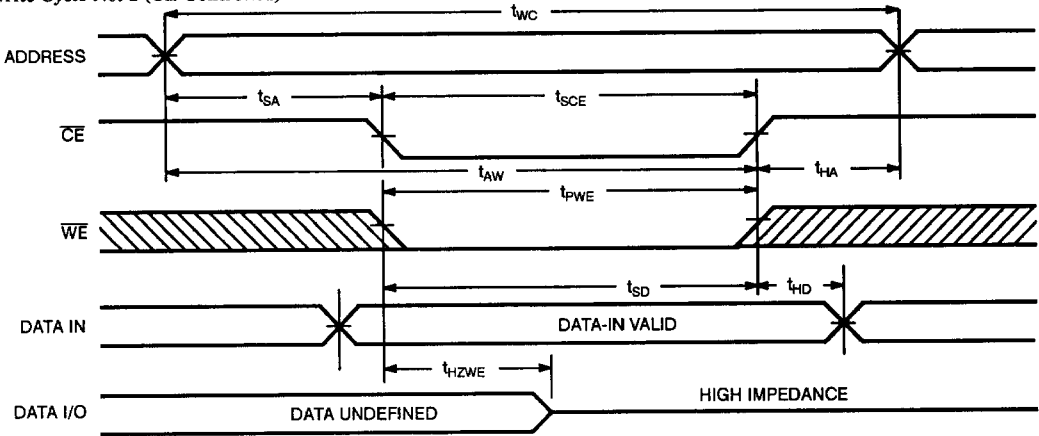
C164-11

Notes:

9. \overline{WE} is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE} = V_{IL}$. (7C166: $\overline{OE} = V_{IL}$ also).
11. Address valid prior to or coincident with \overline{CE} transition low.
12. 7C166 only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

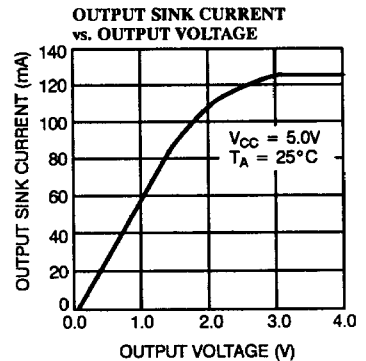
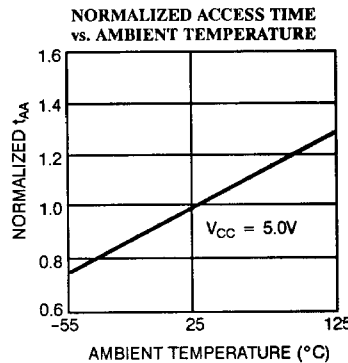
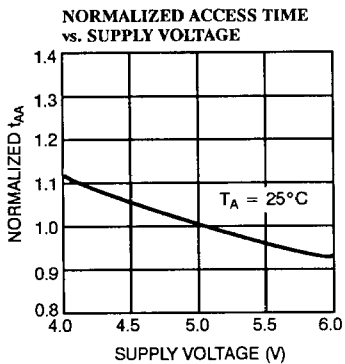
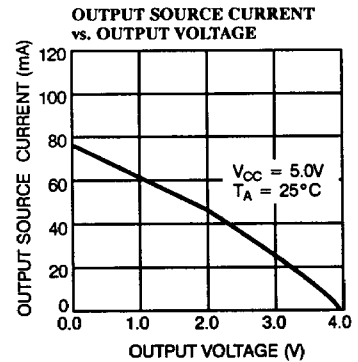
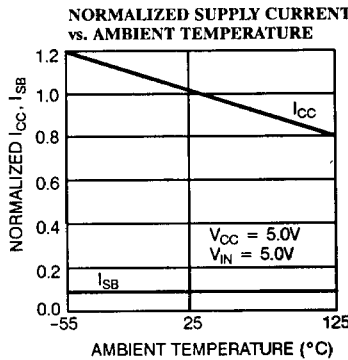
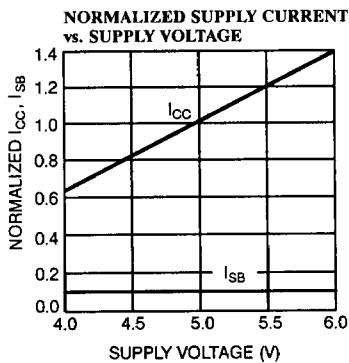
Write Cycle No. 2 (CE Controlled)^[8, 12, 13]



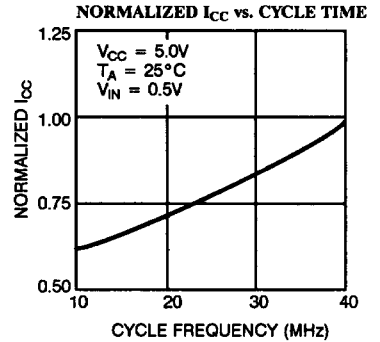
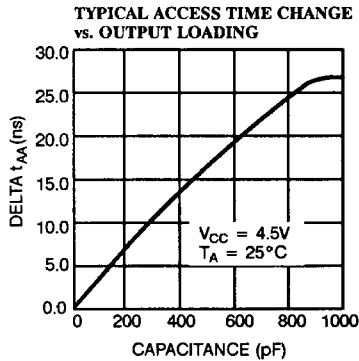
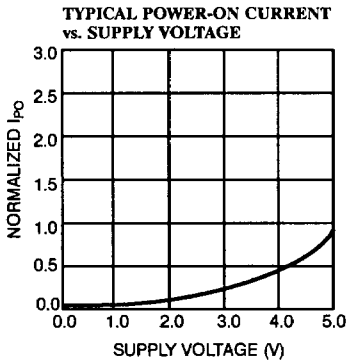
C164-12

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Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)



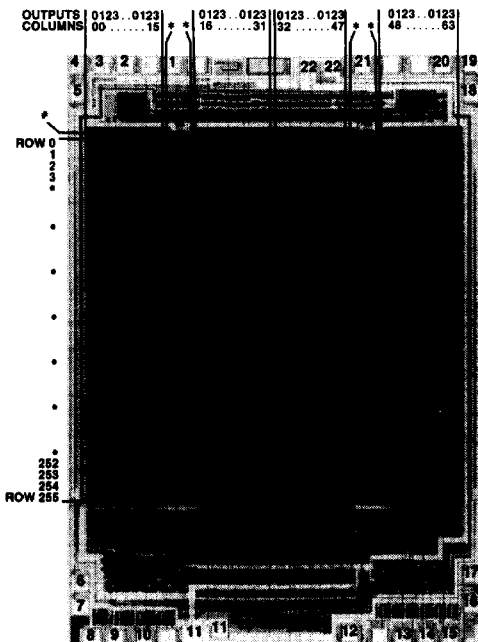
7C164 Truth Table

\overline{CE}	\overline{WE}	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7C166 Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Write

Bit Map



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y5	6
A11	Y4	7
A12	Y0	8
A13	Y1	9
A0	Y2	17
A1	Y3	18
A2	X0	19
A3	X1	20
A4	X2	21

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C164-15PC	P9	Commercial
	CY7C164-15VC	V13	
	CY7C164-15DC	D10	
	CY7C164-15LC	L52	
20	CY7C164-20PC	P9	Commercial
	CY7C164-20VC	V13	
	CY7C164-20DC	D10	
	CY7C164-20LC	L52	
25	CY7C164-25PC	P9	Commercial
	CY7C164-25VC	V13	
	CY7C164-25DC	D10	
	CY7C164-25LC	L52	
35	CY7C164-35PC	P9	Commercial
	CY7C164-35VC	V13	
	CY7C164-35DC	D10	
	CY7C164-35LC	L52	
45	CY7C164-45PC	P9	Commercial
	CY7C164-45VC	V13	
	CY7C164-45DC	D10	
	CY7C164-45LC	L52	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C166-15PC	P13	Commercial
	CY7C166-15VC	V13	
	CY7C166-15DC	D14	
	CY7C166-15LC	L54	
20	CY7C166-20PC	P13	Commercial
	CY7C166-20VC	V13	
	CY7C166-20DC	D14	
	CY7C166-20LC	L54	
25	CY7C166-25PC	P13	Commercial
	CY7C166-25VC	V13	
	CY7C166-25DC	D14	
	CY7C166-25LC	L54	
35	CY7C166-35PC	P13	Commercial
	CY7C166-35VC	V13	
	CY7C166-35DC	D14	
	CY7C166-35LC	L54	
45	CY7C166-45PC	P13	Commercial
	CY7C166-45VC	V13	
	CY7C166-45DC	D14	
	CY7C166-45LC	L54	

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