RFD12N06RLE, RFD12N06RLESM RFP12N06RLE

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

January 1994

Features

- 12A, 60V
- $r_{DS(on)} = 0.135\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

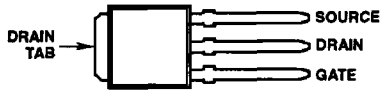
Description

These N-channel logic-level ESD protected power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

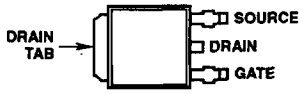
The RFD12N06RLE is supplied in the JEDEC TO-251, RFD12N06RLESM in the JEDEC TO-252, and RFP12N06-RLE in the JEDEC TO-220AB plastic package.

Packages

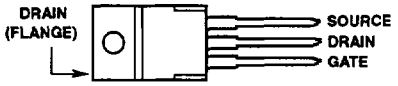
RFD12N06RLE (TO-251)
TOP VIEW



RFD12N06RLESM (TO-252)
TOP VIEW

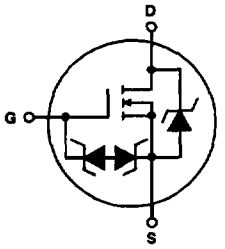


RFP12N06RLE (TO-220AB)
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	12	A
Pulsed Drain Current	I_{DM}	26	A
Gate-Source Voltage	V_{GS}	+10	-5V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Above T_C = +25°C, Derate Linearly		0.32	W/°C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve Electrostatic Discharge Rating, ESD, MIL-STD-883, Category B(2)		2	KV
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

File Number **2407.2**

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFD12N06RLE RFD12N06RLESM RFP12N06RLE Min	Max	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA V_{GS} = 0 V		60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 0.25 mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V T_C = 150°C		— —	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10 V V_{GS} = -5 V		— —	10 10	μA
On Resistance	$r_{DS(on)}$	V_{GS} = 5.0 V, I_D = 12 A V_{GS} = 4.0 V, I_D = 12 A		— —	0.135 0.160	Ω
Turn-On Time	$t_{(on)}$	See Fig. 13		—	60	ns
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 6 A		12 (typ)	—	ns
Rise Time	t_r	R_L = 5.0 Ω		20 (typ)	—	ns
Turn-Off Delay Time	$t_{d(off)}$	Ig1 = Ig2 = 0.4 A		24 (typ)	—	ns
Fall Time	t_f	$V_{GS(clamp)}$ = +5 V, -0.6 V		12 (typ)	—	ns
Turn-Off Time	$t_{(off)}$			—	60	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-10 V	V_{DD} = 48 V I_D = 12 A R_L = 4.0 Ω	—	40	nC
Gate Charge at 5 Volts	$Q_{g(5)}$	V_{GS} = 0-5 V		—	20	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0-1 V		—	1.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 12 A, V_{DS} = 15 V		—	4.0	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30 V, I_D = 6 A L = 0.2 uH, Ig1 = Ig2 = 0.4 A $V_{GS(clamp)}$ = +5.0 V, -0.6 V R_L = 5.0 Ω		—	10	μJ
Thermal Resistance Junction to Case	RθJC			—	3.125	°C/W
Thermal Resistance Junction to Ambient	RθJA	TO-251 & TO-252 packages TO-220 package		— —	100 80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Forward Voltage	V_{SD}	I_{SD} = 12A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 12 A dI_F/dt = 100 A/μs	—	200	ns

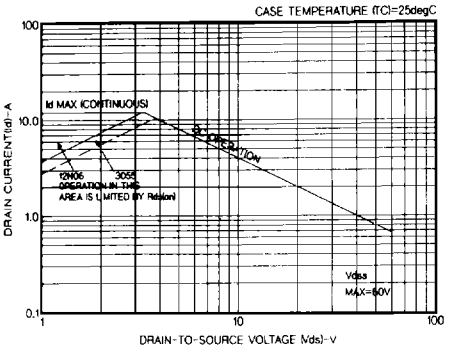


Fig. 1 - Safe-operating area curve. (Curves must be derated linearly with increase in case temperature.)

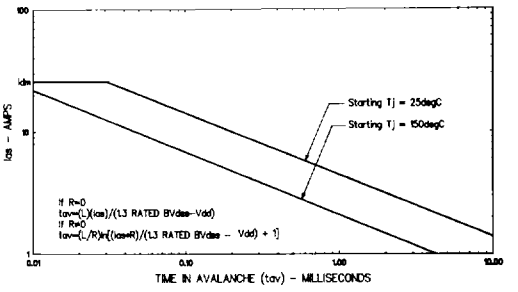


Fig. 2 - Unclamped-inductive-switching. Safe-operating-area. (Single pulse UIS SOA.)

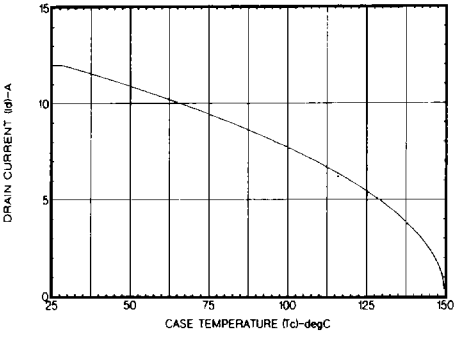


Fig. 3 - Maximum continuous drain current vs. temperature.

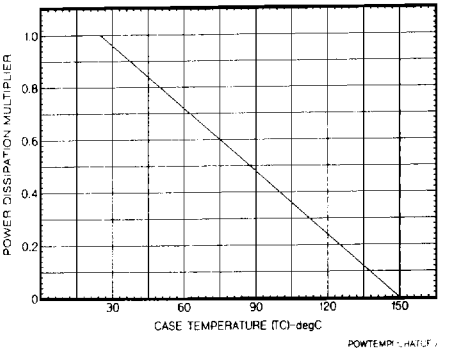


Fig. 4 - Normalized power dissipation vs. temperature derating curve.

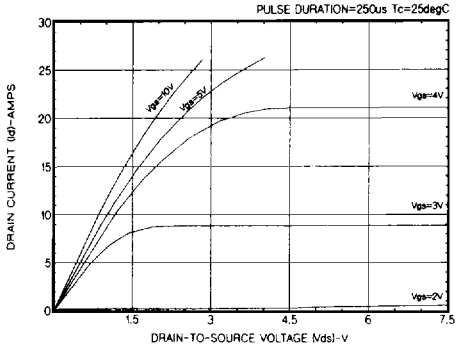


Fig. 5 - Typical saturation characteristics.

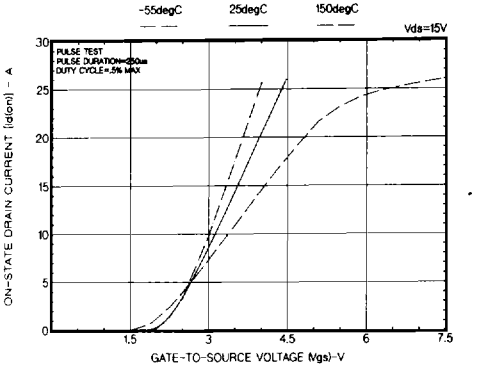


Fig. 6 - Typical transfer characteristics.

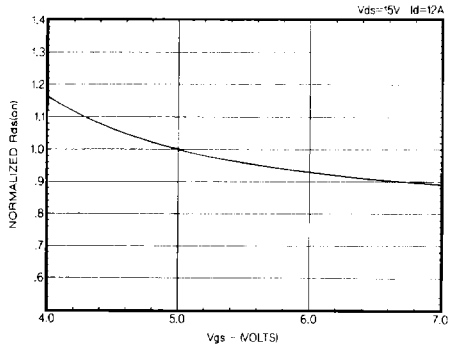


Fig. 7 - Normalized $r_{DS}(on)$ vs. V_{gs}.

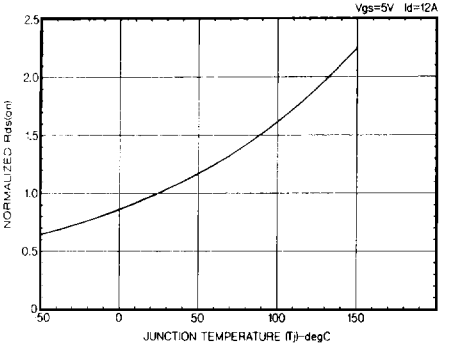


Fig. 8 - Normalized $r_{DS(on)}$ vs. junction temperature.

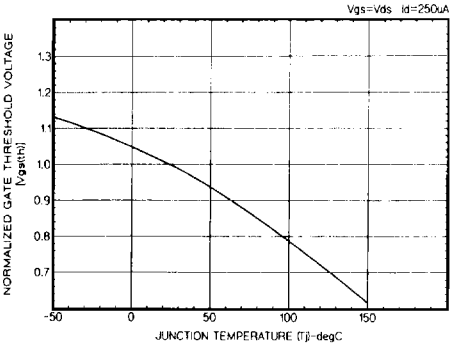


Fig. 9 - Normalized gate threshold voltage vs. temperature.

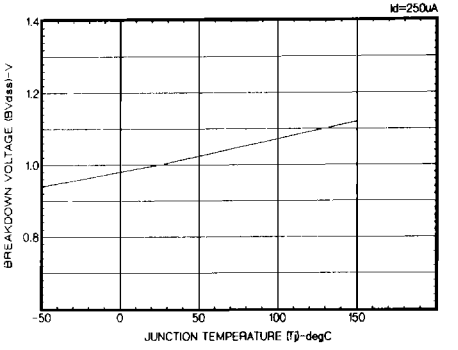


Fig. 10 - Normalized drain source breakdown voltage vs. temperature.

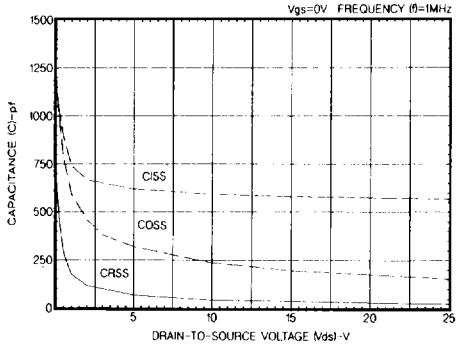


Fig. 11 - Typical capacitance vs. voltage.

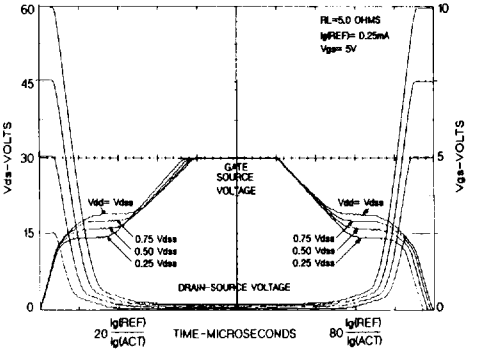


Fig. 12 – Typical switching waveforms for constant gate current. Refer to Harris application notes AN7254 and AN-7260.

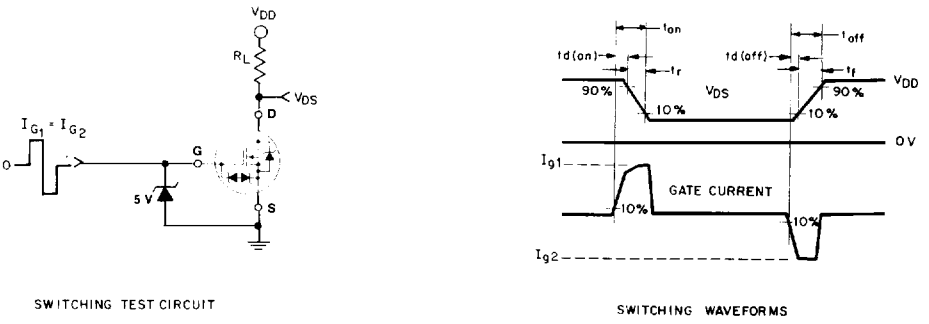


Fig. 13 - Resistive switching.

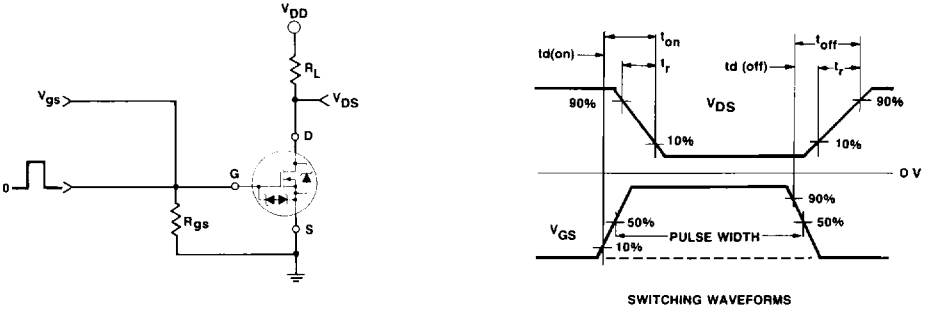


Fig. 14 - Resistive switching.

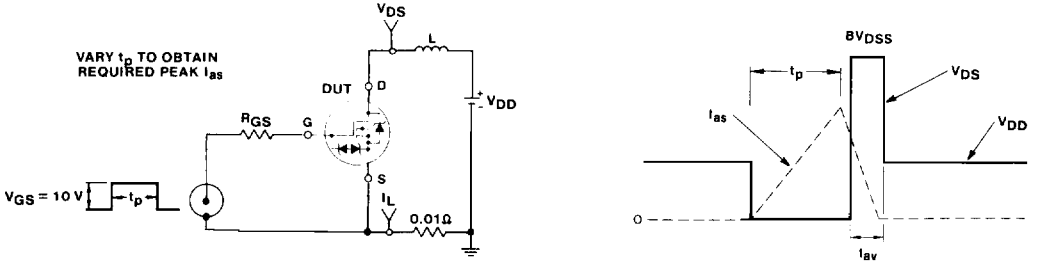


Fig. 15 - Unclamped inductive switching test.