General Description

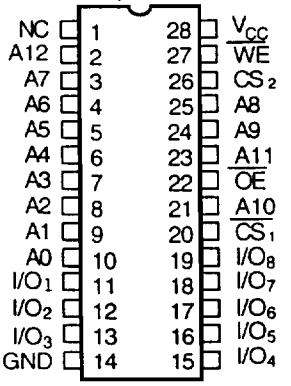
The HM6264L is a 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates from a single 5 volt supply. It is built with high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Features

* High speed - 45/55/70/90 ns(MAX.).
* Low Power consumption :
  HM6264 : 150mW (Typ.)(f=1MHz) operating.
  10μW (Typ.)standby.
* Single 5V power supply.
* Fully static operation.
* All inputs and outputs directly TTL compatible.
* Three-state outputs.
* Data retention supply voltage : 2.0-5.5V.
* Package : HM6264LP - 28 pin 600 mil - plastic DIP.
  HM6264LK - 28 pin 300 mil - plastic Skinny DIP.
  HM6264LM - 28 pin 300 mil - plastic SOP.
  HM6264LWM - 28 pin 330 mil - plastic SOP.
  HM6264LH - Chip Form.

Pin Assignment

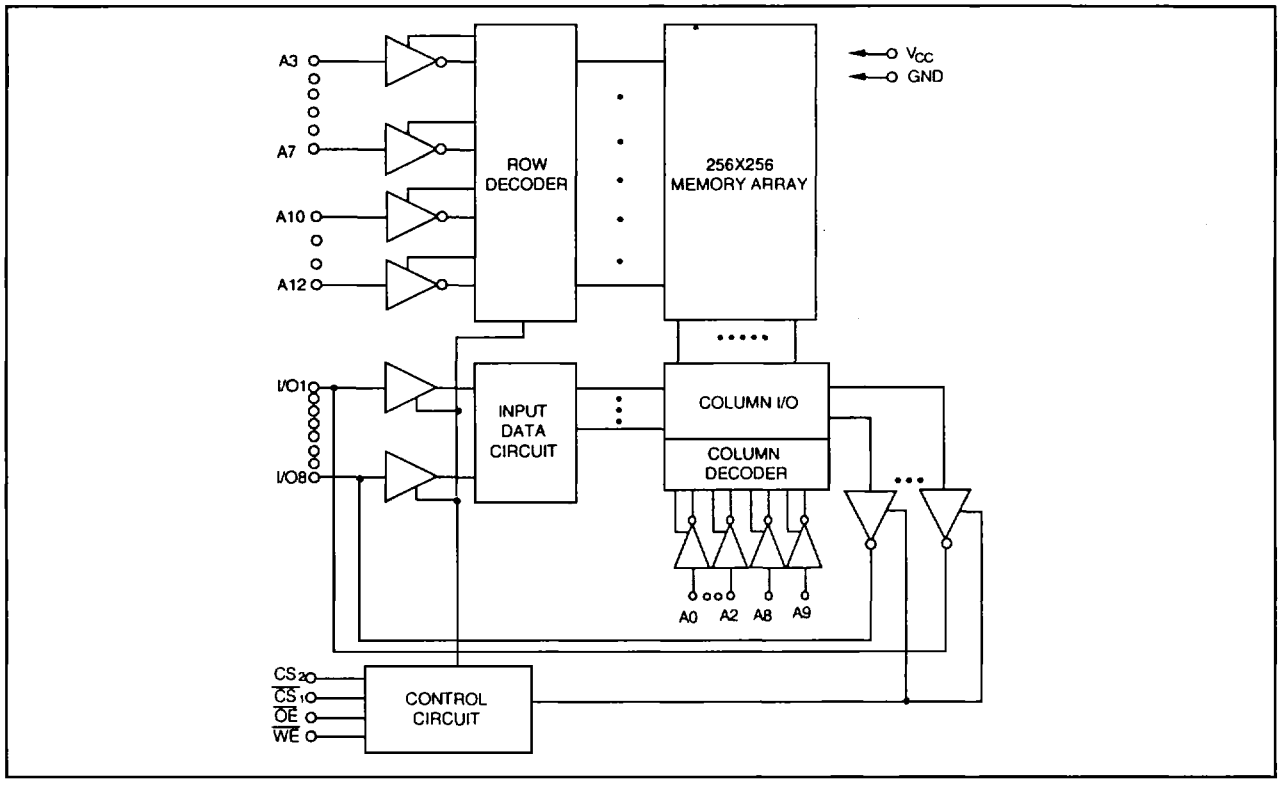
HM6264LP, HM6264LM
HM6264LK, HM6264LWM



Pin Description

A_0-A_{12}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1 - I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER	$\overline{CS_1}$	CHIP SELECT ONE
GND	GROUND	CS_2	CHIP SELECT TWO
NC	NO CONNECTION		

Block Diagram



Absolute Maximum Ratings

Parameter	Sym.	Rating	Units
Terminal Voltage With Respect to GND	V_{TERM}	-0.3 to 7.0	V
Temp under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_T	1.0	W

* Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operation Range

Range	Ambient Temperature	V_{CC}
Commerical	0°C to +70°C	5V±10%

Recommended DC Operating Conditions (T_A=0 to +70°C)

Parameter	Sym.	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low Voltage	V_{IL}	-0.3	0	0.8	V

D.C. Electrical Characteristics

(V_{CC}=5V±10% , GND=0V , T_A=0 to +70°C)

Parameter	Sym.	6264L-45 Min	Typ(1)	Max	6264L-55 Min	Typ(1)	Max	6264L-70 Min	Typ(1)	Max	6264L-90 Min	Typ(1)	Max	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	1	-	-	1	-	-	1	-	-	1	µA	V_{IN}=GND toV_{CC}
Output Leakage	I_{LO}	-	-	1	-	-	1	-	-	1	-	-	1	µA	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL} or, $\overline{OE}$=V_{IH},$\overline{WE}$=V_{IL} $V_{I/O}$=GND toV_{CC}
Operating Power Supply Current	I_{CC}	-	30	50	-	30	50	-	30	50	-	30	50	mA	$\overline{CS_1}$=V_{IL},CS_2=V_{IH}, $I_{I/O}$=0mA
Dynamic Operating Current	I_{CC1}	-	30	50	-	30	50	-	30	50	-	30	50	mA	tcycle=1µs
	I_{CC2}	-	55	80	-	50	70	-	45	60	-	40	60	mA	tcycle=T_{AA} Min. Duty Cycle =100%,$\overline{CS_1}$=V_{IL} CS_2=V_{IH}
Standby Power Supply Current	I_{SB}	-	1	3	-	1	3	-	1	3	-	1	3	mA	$\overline{CS_1}$=V_{IH},I_{IO}=0mA
	I_{SB1}	-	2	100	-	2	100	-	2	100	-	2	100	µA	$\overline{CS_1}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V
	I_{SB2}	-	2	100	-	2	100	-	2	100	-	2	100	µA	CS_2≤0.2V ,V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V
Output Voltage	V_{OL}	-	-	0.4	-	-	0.4	-	-	0.4	-	-	0.4	V	I_{OL}=8mA
(1)	V_{OH}	2.4	-	-	2.4	-	-	2.4	-	-	2.4	-	-	V	I_{OH}=-4mA

Note : Typical limits are at V_{CC}=5.0V,T_A=25°C and specified loading.

Truth Table

Mode	$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O Operation	V_{CC} Current
Not Selected (Power Down)	X	H	X	X	High Z	I_{SB} , I_{SB1}
	X	X	L	X	High Z	I_{SB} , I_{SB2}
Output Disable	H	L	H	H	High Z	I_{CC} , I_{CC1}
Read	H	L	H	L	D_{OUT}	I_{CC} , I_{CC1}
Write	L	L	H	X	D_{IN}	I_{CC} , I_{CC1}

Capacitance*

(T_A=25°C , f=1.0MHz)

Parameter	Sym.	Max.	Unit	Conditions
Input Capacitance	C_{IN}	8	pF	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	10	pF	$V_{I/O}$=0V

* This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate and CL=30pF (see Fig.1 and Fig.2)

* This parameter is periodically sampled and not 100% tested.

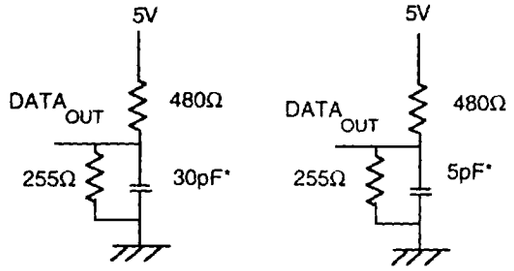


Figure 1. Output Load Figure 2. Output Load for (t_{OLZ},t_{CLZ} t_{OHZ},t_{WHZ},t_{CHZ},t_{OW})
*Including scope and jig

AC Electrical Characteristics

over the operating range

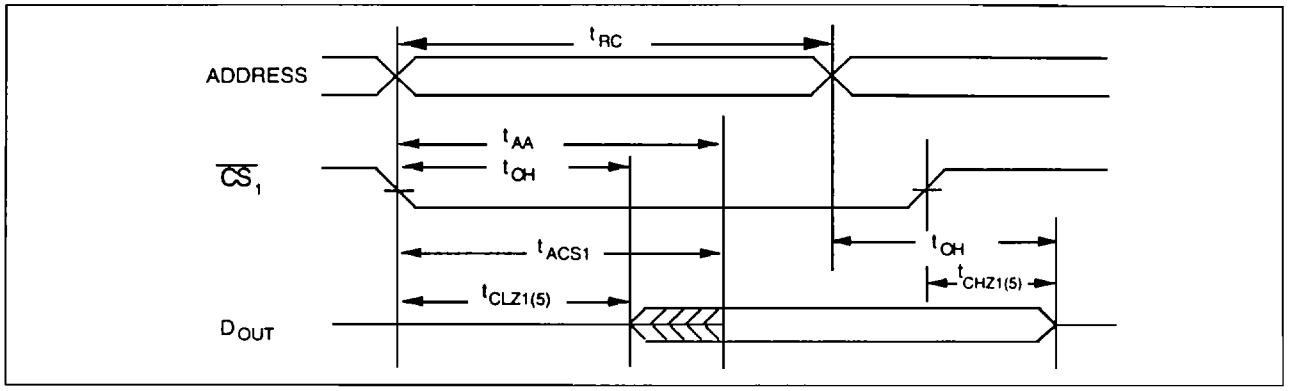
Parameter		Sym.	6264L-45 Min.	6264L-45 Max.	6264L-55 Min.	6264L-55 Max.	6264L-70 Min.	6264L-70 Max.	6264L-90 Min.	6264L-90 Max.	Unit
Read Cycle											
Read Cycle Time		t_{RC}	45	-	55	-	70	-	90	-	ns
Address Access Time		t_{AA}	-	45	-	55	-	70	-	90	ns
Chip Select Access Time	$\overline{CS_1}$	t_{ACS1}	-	45	-	55	-	70	-	90	ns
	CS_2	t_{ACS2}	-	45	-	55	-	70	-	90	ns
Output Enable to Output Valid		t_{OE}	-	20	-	25	-	30	-	35	ns
Chip Selection to Output in Low Z	$\overline{CS_1}$	t_{CLZ1}	5	-	5	-	5	-	5	-	ns
	CS_2	t_{CLZ2}	5	-	5	-	5	-	5	-	ns
Output Enable to Output in Low Z		t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	$\overline{CS_1}$	t_{CHZ1}	0	20	0	25	0	30	0	35	ns
	CS_2	t_{CHZ2}	0	20	0	25	0	30	0	35	ns
Output Disable to Output in High Z		t_{OHZ}	0	20	0	25	0	30	0	35	ns
Output Hold from Address Change		t_{OH}	10	-	10	-	10	-	10	-	ns
Write Cycle											
Write Cycle Time		t_{WC}	45	-	55	-	70	-	90	-	ns
Chip Selection to End of Write		$t_{CW1,2}$	40	-	45	-	45	-	80	-	ns
Address Set-upTime		t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write		t_{AW}	40	-	50	-	60	-	80	-	ns
Write Pulse Width		t_{WP}	35	-	40	-	45	-	50	-	ns
Write Recovery Time	$\overline{CS_1}$,$\overline{WE}$	t_{WR1}	0	-	0	-	0	-	0	-	ns
	CS_2	t_{WR2}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z		t_{WHZ}	0	20	0	25	0	30	0	35	ns
Data to Write Time Overlap		t_{DW}	20	-	25	-	30	-	35	-	ns
Data Hold from Write Time		t_{DH}	0	-	0	-	0	-	0	-	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	20	0	25	0	30	0	35	ns
Output Active from End of Write		t_{OW}	5	-	5	-	5	-	5	-	ns

Note s: $t_{CHZ1,2}$,t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not refered to output voltage levels.

Timing Waveforms

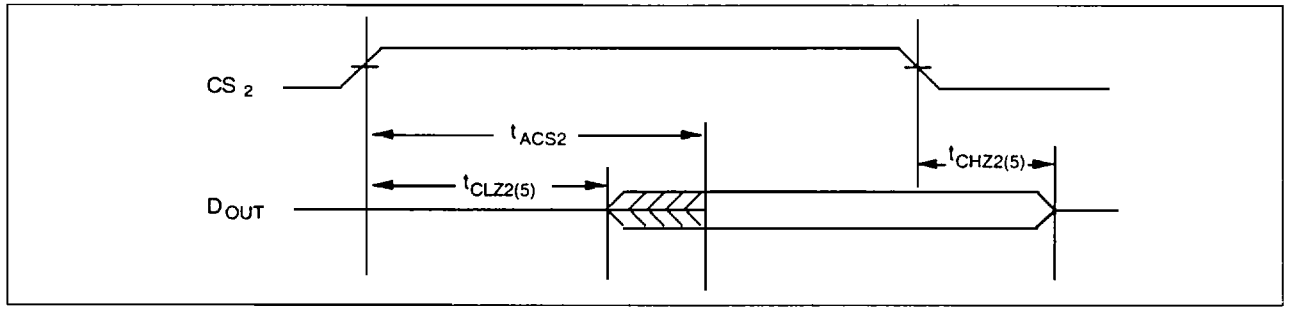
Read Cycle 1

Note (1,2,3,5)



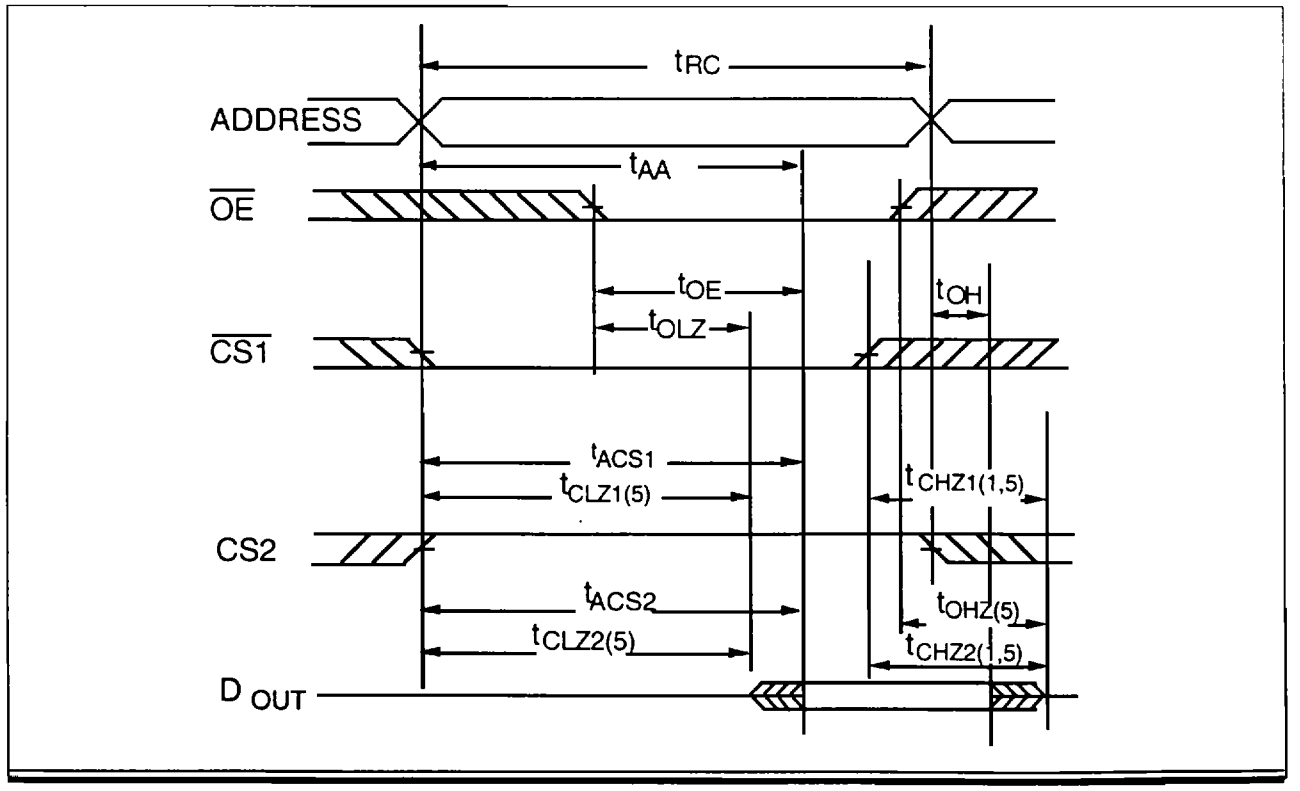
Read Cycle 2

Note (1,3,6,7)



Read Cycle 3

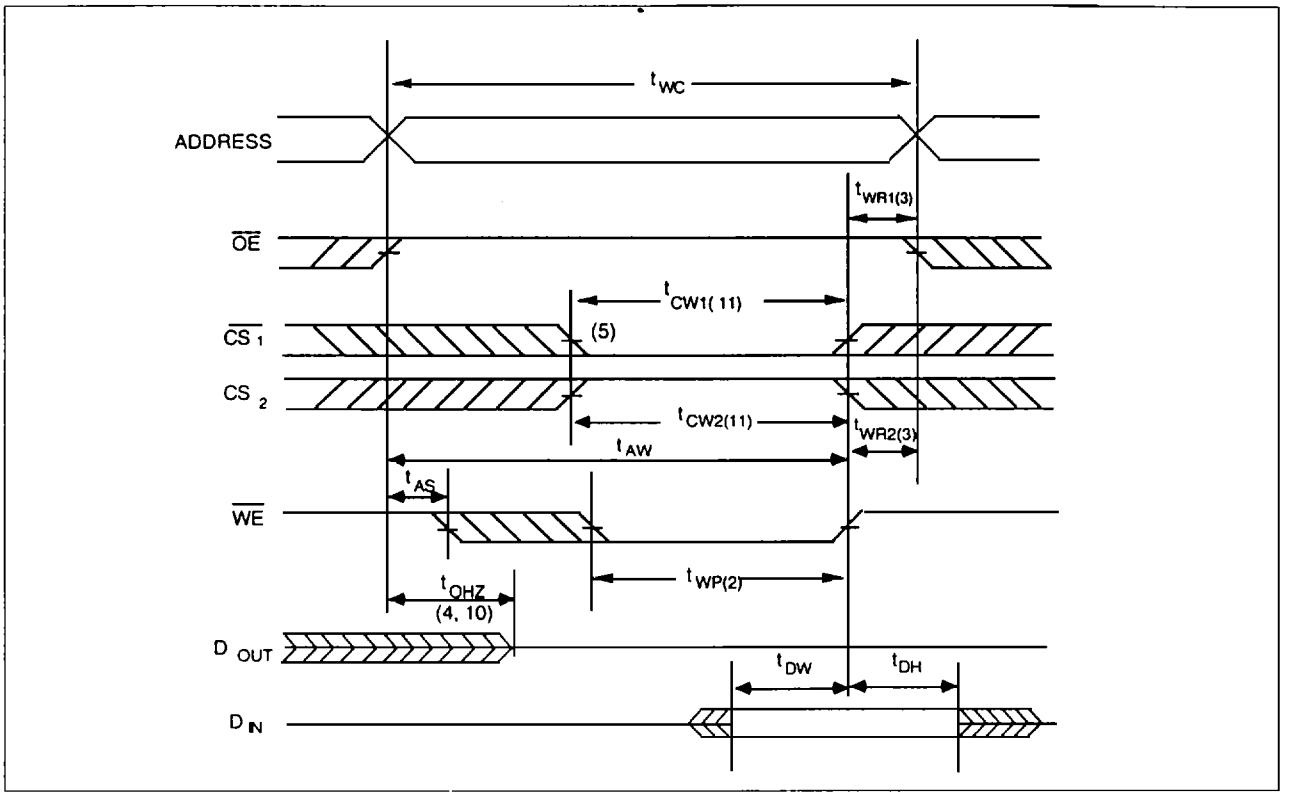
Note (1)



Notes :1. $\overline{WE}$ is High for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS_1}$ transition low.
3. $\overline{OE}=V_{IL}$.
4. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
5. CS_2 is high.
6. $\overline{CS_1}$ is low.
7. Address valid prior to or coincident with CS_2 transition high.

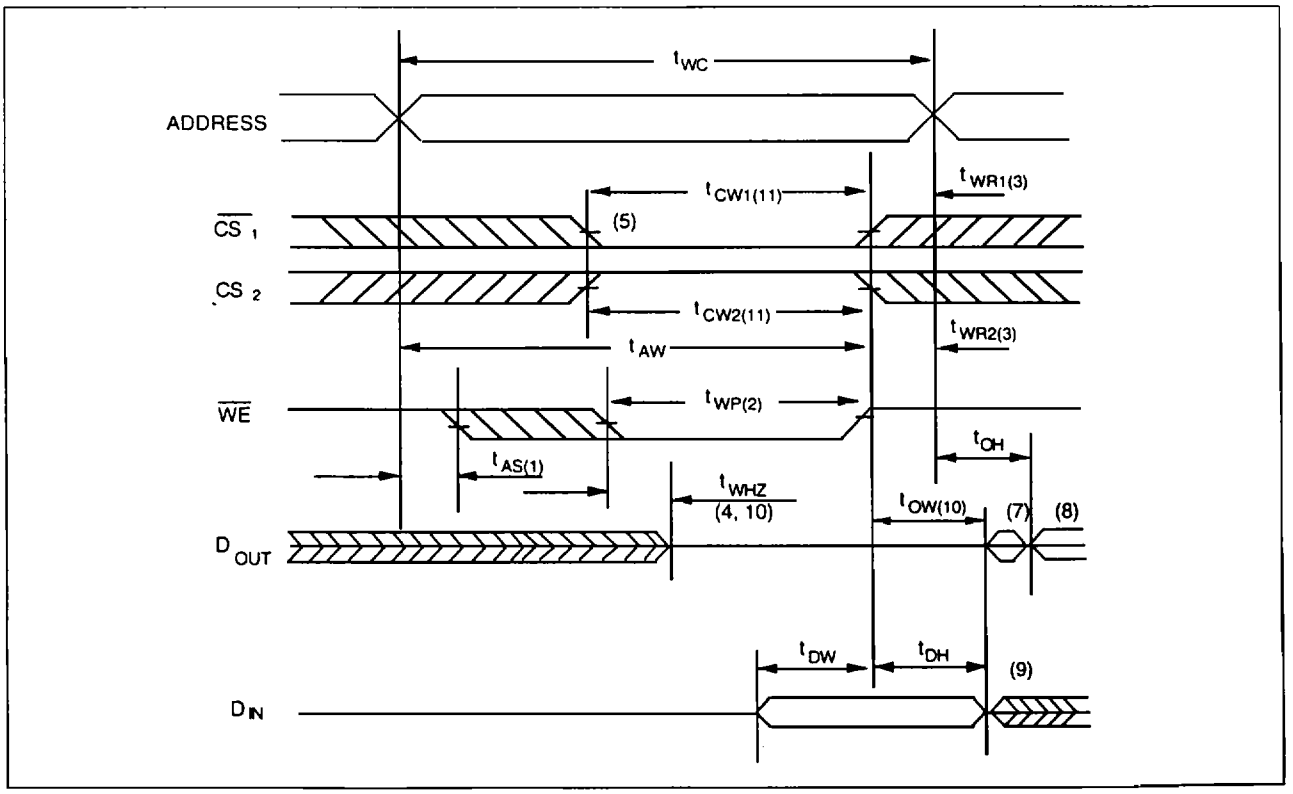
Timing Waveforms of Write Cycle 1

Note (1).



Write Cycle 2

Note (6).



Notes : 1. t_{AS} is measured from the address valid to the beginning of write.
2. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 to the end of write cycle.
4. During this period, I/O pins are in the output state so that the data input signals to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals to the outputs must not be applied to I/O pins.
10 . Transition is measured ±500mV from steady state. This parameter is sampled and 100% tested.
11. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

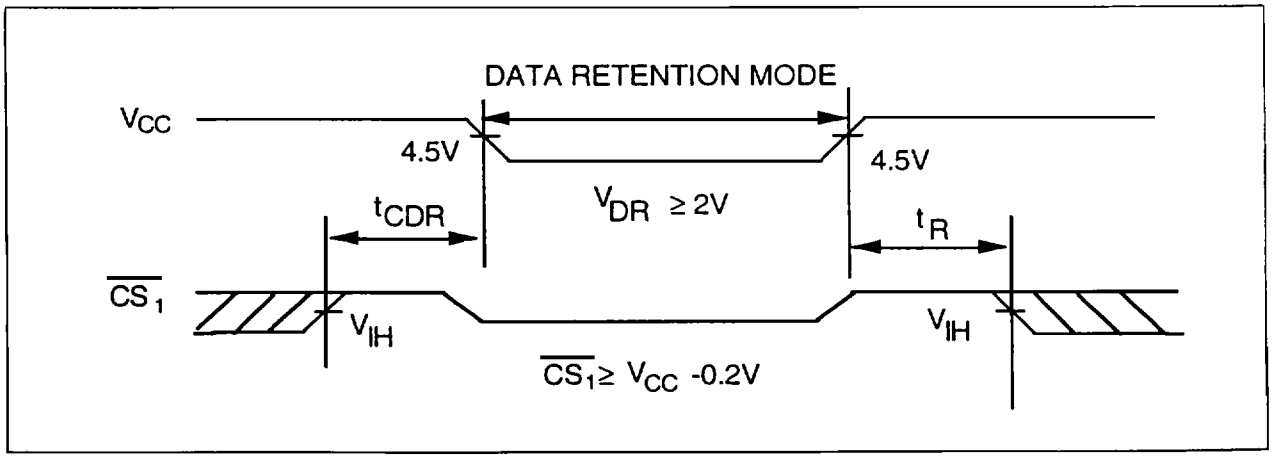
Data Retention Characteristics

(T_A=0 to + 70°C ; L version only)

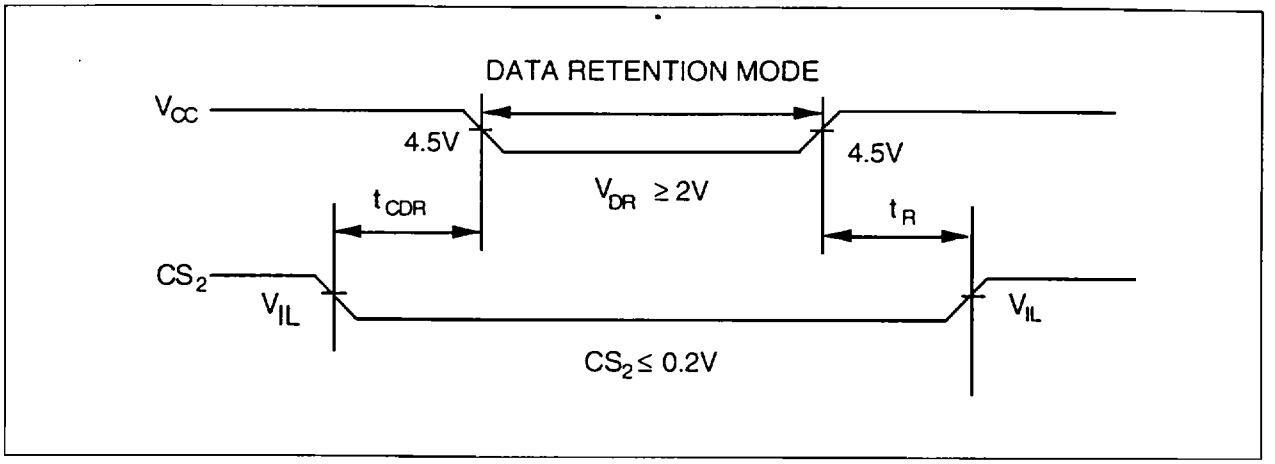
Parameter	Sym.	Min.	Typ(1)	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR1}	2.0	-	5.5	V	$\overline{CS_1}\geq V_{CC}$-0.2V, $V_{IN}\geq V_{CC}$-0.2V,or $V_{IN}\leq$0.2V
	V_{DR2}	2.0	-	5.5	V	$CS_2\leq$0.2V, $V_{IN}\geq V_{CC}$-0.2V, or $V_{IN}\leq$0.2V
Data retention Current	I_{CCDR1}	-	2	50	µA	$\overline{CS_1}\geq V_{CC}$-0.2V, $V_{IN}\geq V_{CC}$-0.2V ,or $V_{IN}\leq$o.2V
	I_{CCDR2}	-	2	50	µA	$CS_2\leq$0.2V, $V_{IN}\geq V_{CC}$-0.2V, or $V_{IN}\leq$0.2V
Chip Deselect to Data Retention Time	t_{CDR}	0	-	-	ns	See Retention
Operation Recovery Time	t_R	$t_{RC(2)}$	-	-	ns	Waveform

1. V_{CC}=2V, T_A=+25°C.
2. t_{RC}=Read Cycle Time.

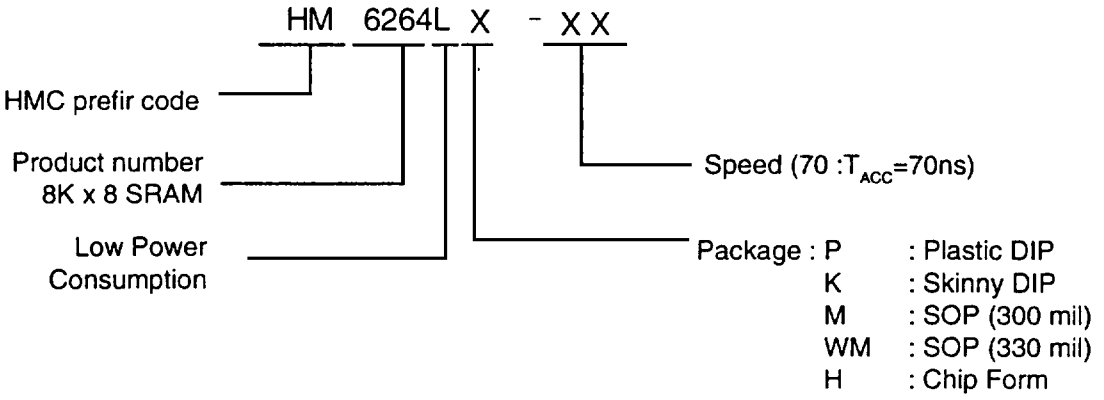
Low V_{CC} Data Retention Waveform (1) ($\overline{CS_1}$ Controlled)



Low V_{CC} Data Retention Waveform (2) (CS_2 Controlled)

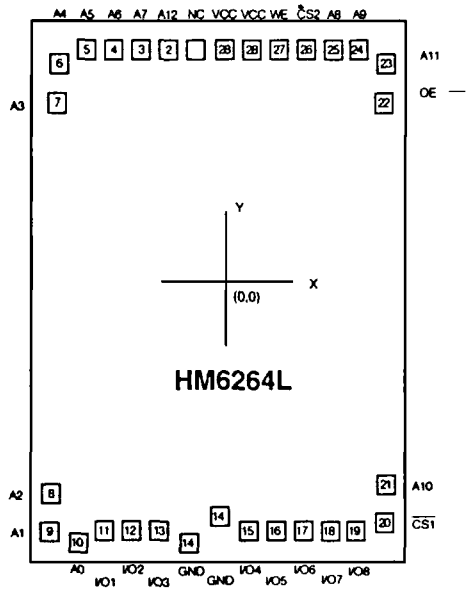


Ordering Information



Order Number	Access Time (ns)	Operation Current (mA)	Standby Current (μA)	Package Type
HM6264LP-45	45	80	100	
HM6264LP-55	55	70	100	28L DIP
HM6264LP-70	70	60	100	
HM6264LP-90	90	60	100	
HM6264LK-45	45	80	100	
HM6264LK-55	55	70	100	28L
HM6264LK-70	70	60	100	Skinny DIP
HM6264LK-90	90	60	100	
HM6264LM-45	45	80	100	
HM6264LM-55	55	70	100	28LSOP
HM6264LM-70	70	60	100	(300 mil)
HM6264LM-90	90	60	100	
HM6264LWM-45	45	80	100	
HM6264LWM-55	55	70	100	28LSOP
HM6264LWM-70	70	60	100	(330 mil)
HM6264LWM-90	90	60	100	

Pad Diagram

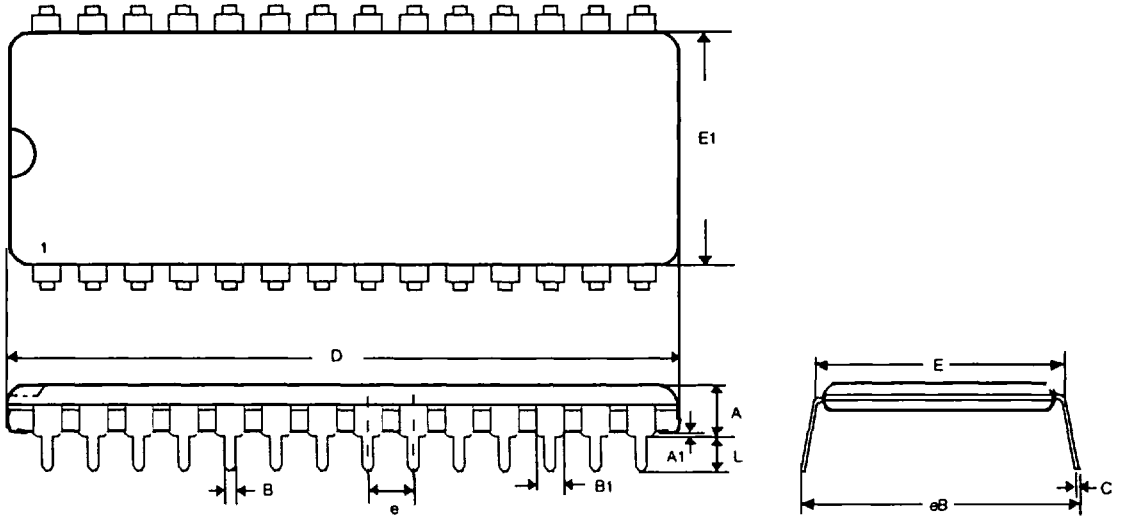


Pin No.	Name	X	Y
1	NC	-160.1	1702.8
2	A12	-349.0	1702.8
3	A7	-509.0	1702.8
4	A6	-689.0	1702.8
5	A5	-849.0	1702.8
6	A4	-1029.0	1641.3
7	A3	-1030.0	1405.1
8	A2	-1030.0	-1449.7
9	A1	-1030.0	-1683.5
10	A0	-850.0	-1745.0
11	I/O1	-687.7	-1711.8
12	I/O2	-514.9	-1711.8
13	I/O3	-342.1	-1711.8
14	GND	-162.1	-1745.0
14	GND	-38.0	-1588.6
15	I/O4	168.3	-1711.8
16	I/O5	341.1	-1711.8
17	I/O6	513.9	-1711.8
18	I/O7	686.7	-1711.8
19	I/O8	859.5	-1711.8
20	CS1	1030.0	-1683.5
21	A10	1030.0	-1449.7
22	OE	1030.0	1405.1
23	A11	1016.4	1641.3
24	A9	836.4	1702.8
25	A8	674.4	1702.8
26	CS2	496.4	1702.8
27	WE	336.4	1702.8
28	V_{CC}	159.9	1702.8
28	V_{CC}	-0.1	1702.8

Chip Size : 2390 x 3820 μm
Note : The substrate must be connected to V_{SS} in PCB layout artwork.

Package Information

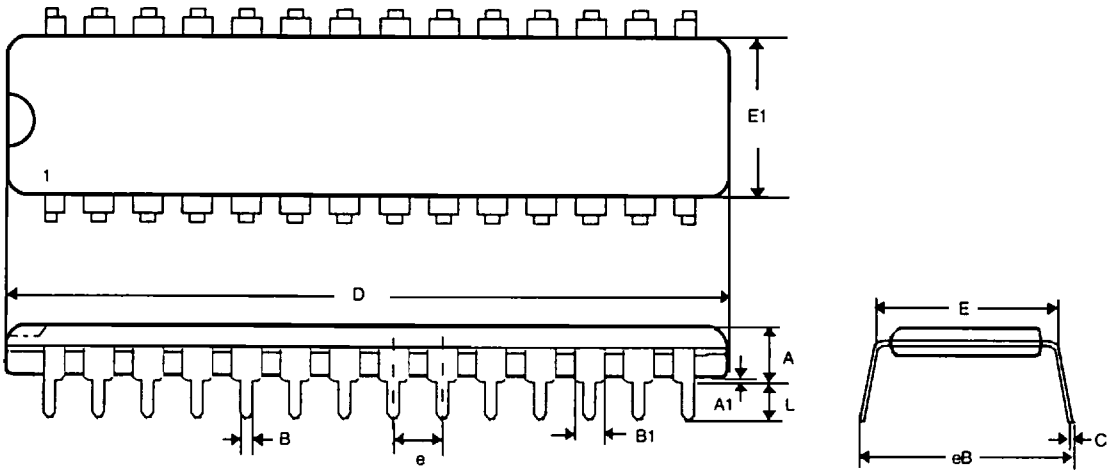
28 Lead Plastic Dual - Inline Package



Notes :
1. DIM D & E1 do not include mold flash or protrusions.
2. DIM eB measured at the lead tip with the leads unconstrained.

DIM	MILIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	----	6.350	----	.250
A1	0.381	----	.015	----
B	0.356	0.558	.014	.022
B1	1.016	1.778	.040	.070
C	0.204	0.381	.008	.015
D	35.56	37.85	1.400	.490
E	15.24	15.88	.600	.625
E1	13.21	14.73	.520	.580
e	2.286	2.794	.090	.110
eB	- - - -	17.78	- - - -	.700
L	2.921	5.080	.115	.200

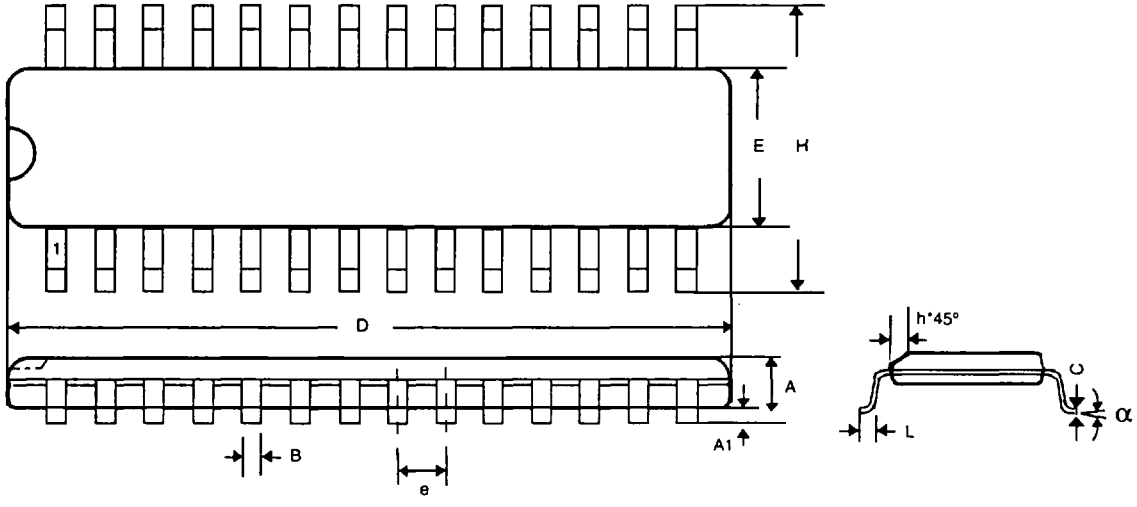
28 Lead Plastic Skinny DIP



Notes :
1. DIM D & E1 do not include mold flash or protrusions.
2. DIM eB measured at the lead tips with the leads unconstrained.

DIM	MILIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	----	5.334	----	.210
A1	0.254	----	.010	----
B	0.356	0.558	.014	.022
B1	1.150	1.778	.045	.070
C	0.204	0.381	.008	.015
D	35.54	35.81	1.360	1.410
E	7.62	8.255	.300	.325
E1	6.6	7.366	.260	.290
e	2.286	2.794	.090	.110
eB	----	10.92	----	.430
L	2.921	4.064	.115	.160

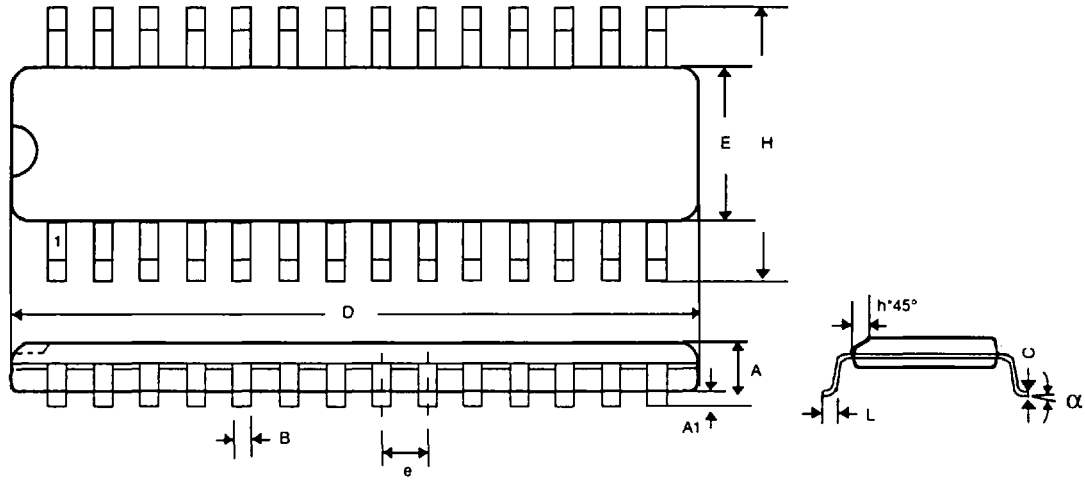
28 Lead Plastic Small Outline Package



Notes :
1. DIM D & E do not include mold flash or protrusions protrusions shall not exceed 0.15mm/.006in.
2. Controlling dimension : millimeter.

DIM	MILIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	.0926	.1043
A1	0.10	0.30	.0040	.0118
B	0.35	0.49	.0138	.0192
C	0.23	0.32	.0091	.0125
D	17.70	18.10	.6969	.7125
E	7.40	7.60	.2914	.2992
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	.25	0.75	.010	.029
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

28 Lead Plastic SOP Width Body 330 mil



Notes :
1. DIM D & E do not include mold flash or protrusions protrusions shall not exceed 0.15mm/.006in.
2. Controlling dimension : millimeter/inch.

DIM	MILIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.5	2.9	.0984	.114
A1	0.1	0.3	.004	.0118
B	0.35	0.49	.0138	.0192
C	0.15	0.28	.006	.011
D	17.8	18.3	.700	.712
E	8.3	8.6	.327	.338
e	1.27 BSC		.050 BSC	
H	11.5	12.1	.453	.476
h	.25	0.75	.010	.029
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°