FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11305-5E

MEMORY

CMOS

1 M × 16 BIT HYPER PAGE MODE DYNAMIC RAM

MB8116165B-50/-60

CMOS 1,048,576 × 16 Bit Hyper Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB8116165B is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB8116165B features a “hyper page” mode of operation whereby high-speed random access of up to 256 × 16 bits of data within the same row can be selected. The MB8116165B DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB8116165B is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB8116165B is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB8116165B are not critical and all inputs are TTL compatible.

■ PRODUCT LINE & FEATURES

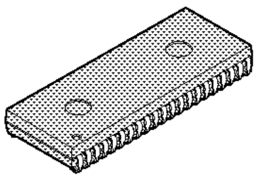
Parameter		MB8116165B-50	MB8116165B-60
$\overline{RAS}$ Access Time		50 ns max.	60 ns max.
Random Cycle Time		84 ns min.	104 ns min.
Address Access Time		25 ns max.	30 ns max.
$\overline{CAS}$ Access Time		15 ns max.	15 ns max.
Hyper Page Mode Cycle Time		20 ns min.	25 ns min.
Low Power Dissipation	Operating Current	660 mW max.	550 mW max.
	Standby Current	11 mW max. (TTL level) / 5.5 mW max. (CMOS level)	

- 1,048,576 words × 16 bits organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are TTL compatible
- 4,096 refresh cycles every 65.6 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Hyper Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

MB8116165B-50/-60

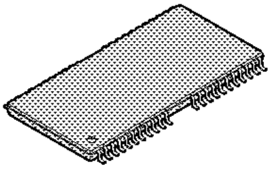
■ PACKAGE

Plastic SOJ Package



(LCC-42P-M01)

Plastic TSOP(II) Package



(FPT-50P-M06)
(Normal Bend)

Package and Ordering Information

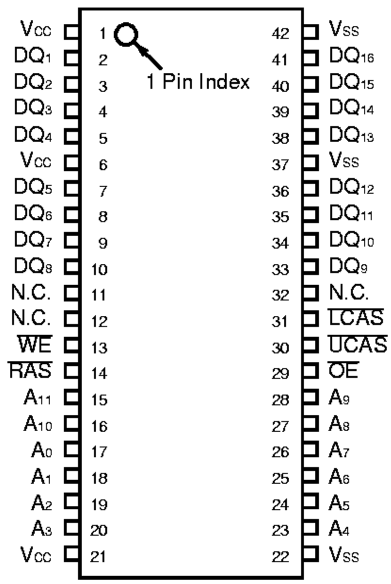
– 42-pin plastic (400 mil) SOJ, order as MB8116165B-xxPJ
– 50-pin plastic (400 mil) TSOP(II) with normal bend leads, order as MB8116165B-xxPFTN

■ PIN ASSIGNMENTS AND DESCRIPTIONS

42-Pin SOJ

(TOP VIEW)

<LCC-42P-M01>



Designator	Function
A_0 to A_{11}	Address inputs row : A_0 to A_{11} column : A_0 to A_7 refresh : A_0 to A_{11}
$\overline{RAS}$	Row address strobe
$\overline{LCAS}$	Lower column address strobe
$\overline{UCAS}$	Upper column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_1 to DQ_{16}	Data Input/Output
V_{CC}	+5.0 volt power supply
V_{SS}	Circuit ground
N.C.	No connection

50-Pin TSOP (II)

(TOP VIEW)

<Normal Bend: FPT-50P-M06>

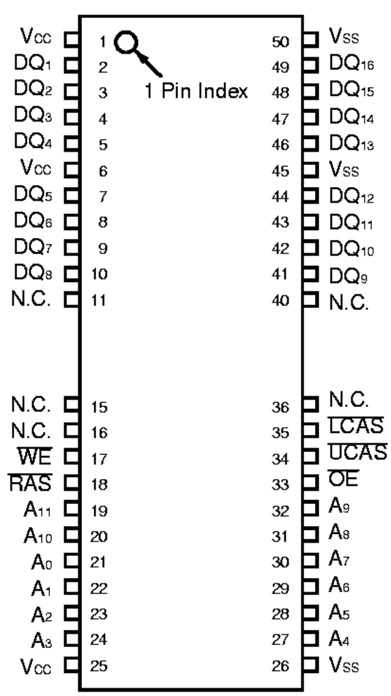


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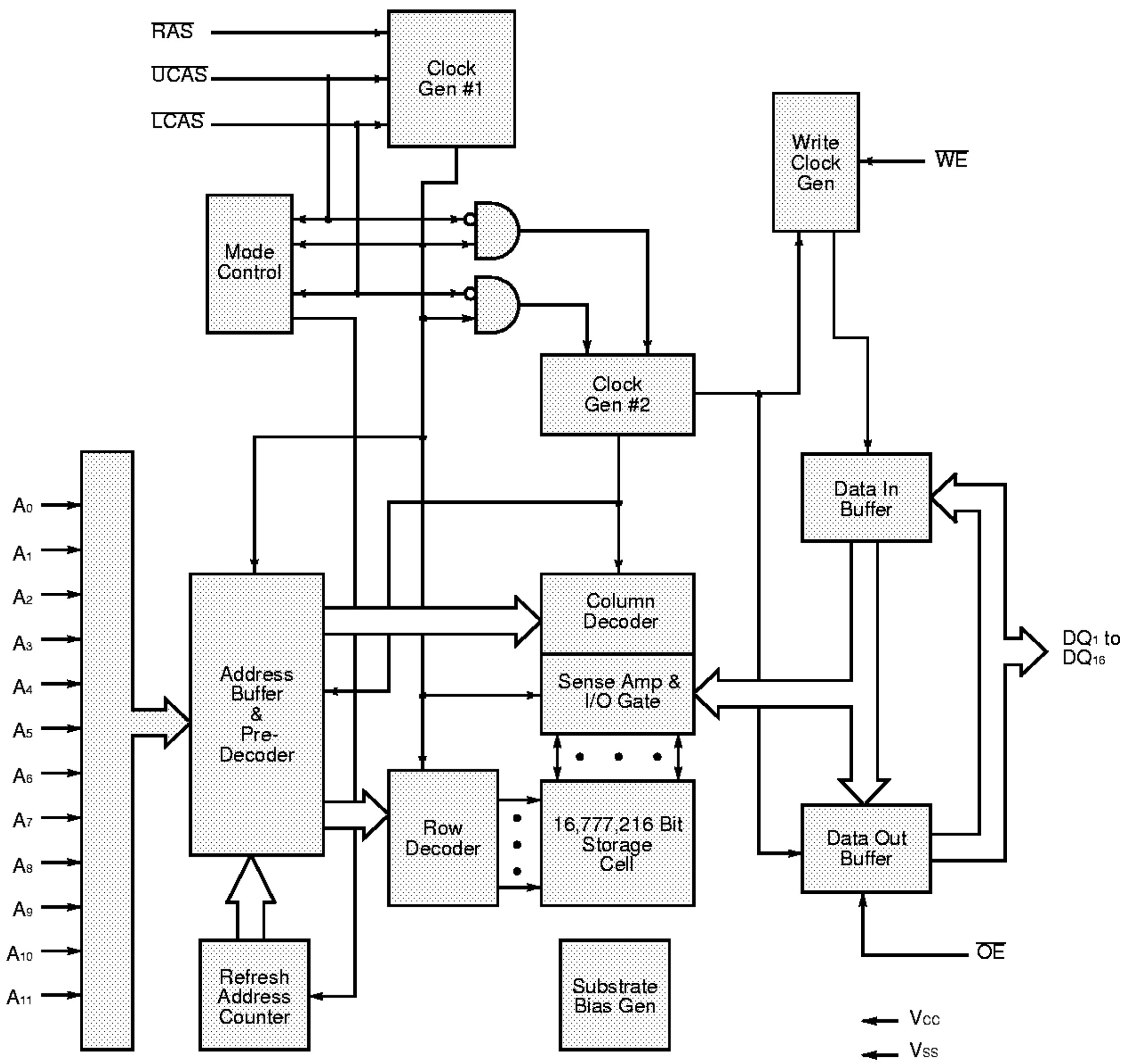
Fig. 1 – MB8116165B DYNAMIC RAM - BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address Input		Input/Output Data				Refresh	Note
	RAS	LCAS	UCAS	WE	OE	Row	Column	DQ_1 to DQ_8		DQ_9 to DQ_{16}			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	
RAS-only Refresh Cycle	L	H	H	X	X	Valid	X	—	High-Z	—	High-Z	Yes	
CAS-before-RAS Refresh Cycle	L	L	L	X	X	X	X	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H→L	L H L	H L L	H→X	L	X	X	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept.

X : "H" or "L"
* : It is impossible in Hyper Page Mode.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A_0 to A_{11}) are available, the column and row inputs are separately strobed by LCAS or UCAS and RAS as shown in Figure 1. First, twelve row address bits are input on pins A_0-through-A_{11} and latched with the row address strobe (RAS) then, eight column address bits are input and latched with the column address strobe (LCAS or UCAS). Both row and column addresses must be stable on or before the falling edges of RAS and LCAS or UCAS, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of WE. When WE is active Low, a write cycle is initiated; when WE is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways: an early write cycle, an OE (delayed) write cycle, and a read-modify-write cycle. The falling edge of WE or LCAS/UCAS, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of DQ_1 to DQ_8 is strobed by LCAS and DQ_9 to DQ_{16} is strobed by UCAS and the setup/hold times are referenced to each LCAS and UCAS because WE goes Low before LCAS/UCAS. In a delayed write or a read-modify-write cycle, WE goes Low after LCAS/UCAS; thus, input data is strobed by WE and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs and High-Z state are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.
t_{CAC} : from the falling edge of $\overline{LCAS}$ (for DQ_1 to DQ_8) $\overline{UCAS}$ (for DQ_9 to DQ_{16}) when t_{RCD} is greater than t_{RCD} (max).
t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max), and t_{RCD} (max) is satisfied.
t_{OEA} : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.
t_{OEZ} : from $\overline{OE}$ inactive.
t_{OFF} : from $\overline{CAS}$ inactive while $\overline{RAS}$ inactive.
t_{OFR} : from $\overline{RAS}$ inactive while $\overline{CAS}$ inactive.
t_{WEZ} : from $\overline{WE}$ active while $\overline{CAS}$ inactive.

The data remains valid before either $\overline{OE}$ is inactive, or both $\overline{RAS}$ and $\overline{LCAS}$ (and/or $\overline{UCAS}$) are inactive, or $\overline{CAS}$ is reactived. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

HYPER PAGE MODE OPERATION

The hyper page mode operation provides faster memory access and lower power dissipation. The hyper page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each page of memory (within column address locations), any of 256 × 16 bits can be accessed and, when multiple MB8116165Bs are used, $\overline{CAS}$ is decoded to select the desired memory page. Hyper page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted. Hyper page mode features that output remains valid when $\overline{CAS}$ is inactive until $\overline{CAS}$ is reactivated.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +7.0	V
Voltage of V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	–50 to +50	mA
Operating Temperature	T_{OPE}	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum rating conditions. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	*1	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
		V_{SS}	0	0	0		
Input High Voltage, All Inputs	*1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, All Inputs*	*1	V_{IL}	–0.3	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance, A_0 to A_{11}	C_{IN1}	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	5	pF
Input/Output Capacitance, DQ_1 to DQ_{16}	C_{DQ}	7	pF

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■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note 3

Parameter	Notes		Symbol	Condition	Value Min.	Value Typ.	Value Max.	Unit
Output High Voltage	*1		V_{OH}	I_{OH} = –5.0 mA	2.4	—	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = +4.2 mA	—	—	0.4	V
Input Leakage Current (Any Input)			$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC}; 4.5 V ≤ V_{CC} ≤ 5.5 V; V_{SS} = 0 V; All other pins not under test = 0 V	–10	—	10	µA
Output Leakage Current			$I_{DO(L)}$	0 V ≤ V_{OUT} ≤ V_{CC}; 4.5 V ≤ V_{CC} ≤ 5.5 V; Data out disabled	–10	—	10	µA
Operating Current (Average Power Supply Current)	*2	MB8116165B-50	I_{CC1}	$\overline{RAS}$ & $\overline{LCAS}$, $\overline{UCAS}$ cycling; t_{RC} = min	—	—	120	mA
		MB8116165B-60					100	
Standby Current (Power Supply Current)	*2	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = V_{IH}	—	—	2.0	mA
		CMOS Level		$\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ ≥ V_{CC} –0.2 V			1.0	
Refresh Current #1 (Average Power Supply Current)	*2	MB8116165B-50	I_{CC3}	$\overline{LCAS}$ = $\overline{UCAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	120	mA
		MB8116165B-60					100	
Hyper Page Mode Current	*2	MB8116165B-50	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{LCAS}$ = $\overline{UCAS}$ cycling; t_{HPC} = min	—	—	120	mA
		MB8116165B-60					100	
Refresh Current #2 (Average Power Supply Current)	*2	MB8116165B-50	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	120	mA
		MB8116165B-60					100	

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB8116165B-50		MB8116165B-60		Unit
				Min.	Max.	Min.	Max.	
1	Time between Refresh		t_{REF}	—	65.6	—	65.6	ms
2	Random Read/Write Cycle Time		t_{RC}	84	—	104	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	114	—	138	—	ns
4	Access Time from $\overline{RAS}$	*6,9	t_{RAC}	—	50	—	60	ns
5	Access Time from $\overline{CAS}$	*7,9	t_{CAC}	—	15	—	15	ns
6	Column Address Access Time	*8,9	t_{AA}	—	25	—	30	ns
7	Output Hold Time		t_{OH}	3	—	3	—	ns
8	Output Hold Time from $\overline{CAS}$		t_{OHC}	5	—	5	—	ns
9	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
10	Output Buffer Turn Off Delay Time	*10	t_{OFF}	—	13	—	15	ns
11	Output Buffer Turn Off Delay Time from $\overline{RAS}$	*10	t_{OFR}	—	13	—	15	ns
12	Output Buffer Turn Off Delay Time from $\overline{WE}$	*10	t_{WEZ}	—	13	—	15	ns
13	Transition Time		t_{T}	1	50	1	50	ns
14	$\overline{RAS}$ Precharge Time		t_{RP}	30	—	40	—	ns
15	$\overline{RAS}$ Pulse Width		t_{RAS}	50	100000	60	100000	ns
16	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	15	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	*21	t_{CRP}	5	—	5	—	ns
18	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*11,12,22	t_{RCD}	11	35	14	45	ns
19	$\overline{CAS}$ Pulse Width		t_{CAS}	7	—	10	—	ns
20	$\overline{CAS}$ Hold Time		t_{CSH}	38	—	40	—	ns
21	$\overline{CAS}$ Precharge Time (Normal)	*19	t_{CPN}	7	—	10	—	ns
22	Row Address Setup Time		t_{ASR}	0	—	0	—	ns
23	Row Address Hold Time		t_{RAH}	7	—	10	—	ns
24	Column Address Setup Time		t_{ASC}	0	—	0	—	ns
25	Column Address Hold Time		t_{CAH}	7	—	10	—	ns
26	Column Address Hold Time from $\overline{RAS}$		t_{AR}	18	—	24	—	ns
27	$\overline{RAS}$ to Column Address Delay Time	*13	t_{RAD}	9	25	12	30	ns
28	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	25	—	30	—	ns
29	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	18	—	23	—	ns
30	Read Command Setup Time		t_{RCS}	0	—	0	—	ns
31	Read Command Hold Time Referenced to $\overline{RAS}$	*14	t_{RRH}	0	—	0	—	ns

(Continued)

No.	Parameter	Notes	Symbol	MB8116165B-50		MB8116165B-60		Unit
				Min.	Max.	Min.	Max.	
32	Read Command Hold Time Referenced to CAS	*14	t_{RCH}	0	—	0	—	ns
33	Write Command Setup Time	*15,20	t_{WCS}	0	—	0	—	ns
34	Write Command Hold Time		t_{WCH}	7	—	10	—	ns
35	Write Command Hold Time from RAS		t_{WCR}	18	—	24	—	ns
36	WE Pulse Width		t_{WP}	7	—	10	—	ns
37	Write Command to RAS Lead Time		t_{RWL}	13	—	15	—	ns
38	Write Command to CAS Lead Time		t_{CWL}	7	—	10	—	ns
39	DIN Setup Time		t_{DS}	0	—	0	—	ns
40	DIN Hold Time		t_{DH}	7	—	10	—	ns
41	Data Hold Time from RAS		t_{DHR}	18	—	24	—	ns
42	RAS to WE Delay Time	*20	t_{RWD}	65	—	77	—	ns
43	CAS to WE Delay Time	*20	t_{CWD}	30	—	32	—	ns
44	Column Address to WE Delay Time	*20	t_{AWD}	40	—	47	—	ns
45	RAS Precharge Time to CAS Active Time (Refresh Cycles)		t_{RPC}	5	—	5	—	ns
46	CAS Setup Time for CAS-before-RAS Refresh		t_{CSR}	0	—	0	—	ns
47	CAS Hold Time for CAS-before-RAS Refresh		t_{CHR}	10	—	10	—	ns
48	Access Time from OE	*9	t_{OEA}	—	15	—	15	ns
49	Output Buffer Turn Off Delay from OE	*10	t_{OEZ}	—	13	—	15	ns
50	OE to RAS Lead Time for Valid Data		t_{OEL}	5	—	5	—	ns
51	OE to CAS Lead Time		t_{COL}	5	—	5	—	ns
52	OE Hold Time Referenced to WE	*16	t_{OEH}	5	—	5	—	ns
53	OE to Data In Delay Time		t_{OED}	13	—	15	—	ns
54	RAS to Data In Delay Time		t_{RDD}	13	—	15	—	ns
55	CAS to Data In Delay Time		t_{CDD}	13	—	15	—	ns
56	DIN to CAS Delay Time	*17	t_{DZC}	0	—	0	—	ns
57	DIN to OE Delay Time	*17	t_{DZO}	0	—	0	—	ns
58	OE Precharge Time		t_{OEP}	5	—	5	—	ns
59	OE Hold Time Referenced to CAS		t_{OECH}	7	—	10	—	ns
60	WE Precharge Time		t_{WPZ}	5	—	5	—	ns
61	WE to Data In Delay Time		t_{WED}	13	—	15	—	ns
62	Hyper Page Mode RAS Pulse Width		t_{RASP}	—	100000	—	100000	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	MB8116165B-50		MB8116165B-60		Unit
				Min.	Max.	Min.	Max.	
63	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	20	—	25	—	ns
64	Hyper Page Mode Read-Modify-Write Cycle Time		t_{HPRWC}	59	—	69	—	ns
65	Access Time from $\overline{CAS}$ Precharge	*9,18	t_{CPA}	—	30	—	35	ns
66	Hyper Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	7	—	10	—	ns
67	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	30	—	35	—	ns
68	Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	*20	t_{CPWD}	45	—	52	—	ns

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rates; the specified values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$, $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$ and $V_{IL} > -0.3$ V.
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$. I_{CC2} is specified during $\overline{RAS} = V_{IH}$ and $V_{IL} > -0.3$ V.

*3. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

*4. AC characteristics assume $t_T = 2$ ns.

*5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).

*6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig.2 and 3.

*7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*9. Measured with a load equivalent to two TTL loads and 100 pF.

*10. t_{OFF}, t_{OFR}, t_{WEZ} and t_{OEZ} are specified that output buffer change to high-impedance state.

*11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. t_{RCD} (min) $= t_{RAH}$ (min) $+ 2t_T + t_{ASC}$ (min).

*13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*16. Assumes that $t_{WCS} < t_{WCS}$ (min).

*17. Either t_{DZC} or t_{DZO} must be satisfied.

*18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both $\overline{UCAS}$ and $\overline{LCAS}$ from “L” to “H”). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).

*19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*20. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and DQ pin will maintain high-impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the DQ pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the DQ pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, t_{RAL}, and t_{CAL} specifications.

*21. The last $\overline{CAS}$ rising edge.

*22. The first $\overline{CAS}$ falling edge.

Fig. 2 – t_{RAC} vs. t_{RCD}

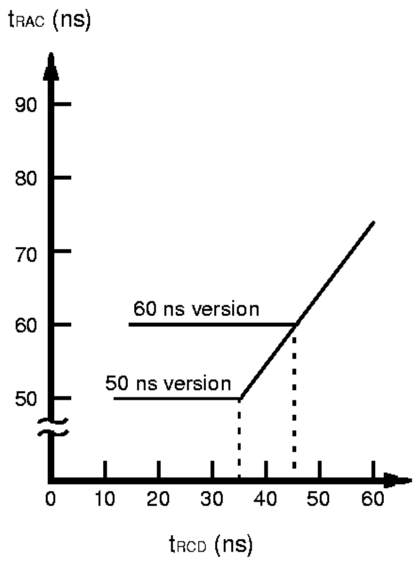


Fig. 3 – t_{RAC} vs. t_{RAD}

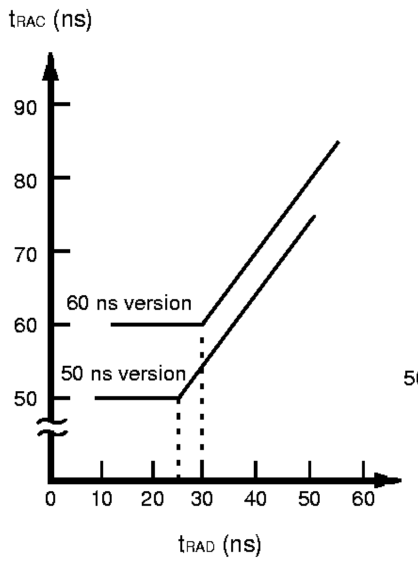


Fig. 4 – t_{CPA} vs. t_{CP}

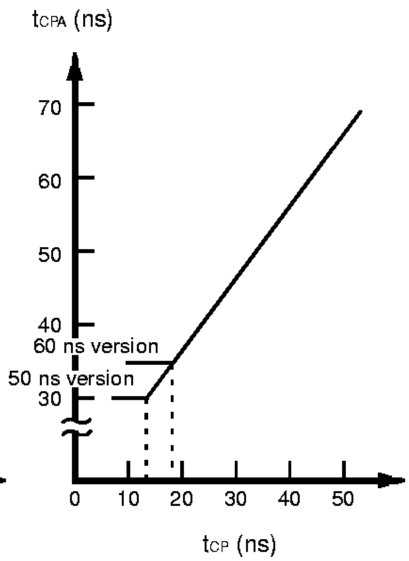
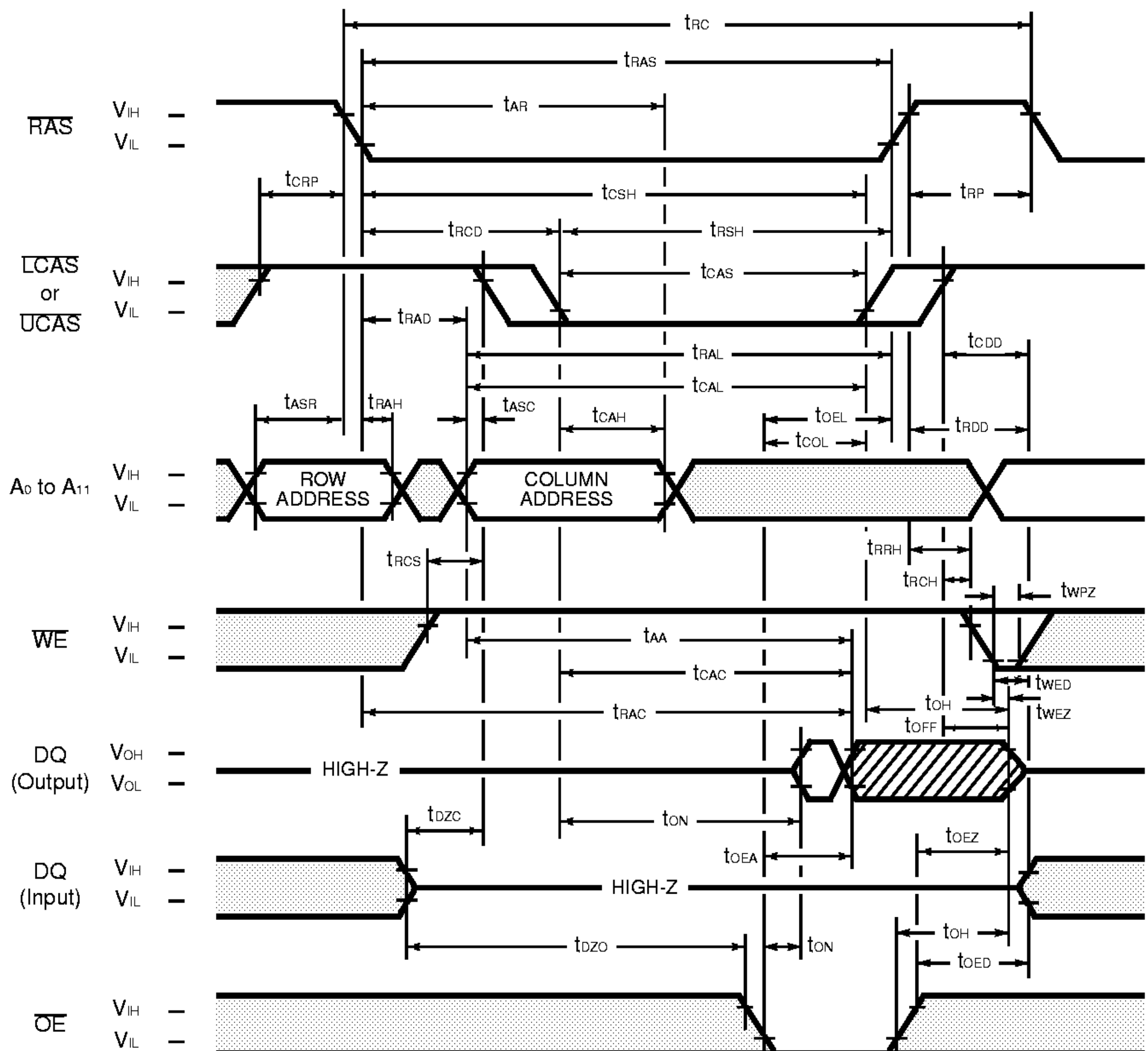


Fig. 5 – READ CYCLE



"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H"→"L" or "L"→"H" transition (Address and DQ)

Valid Data

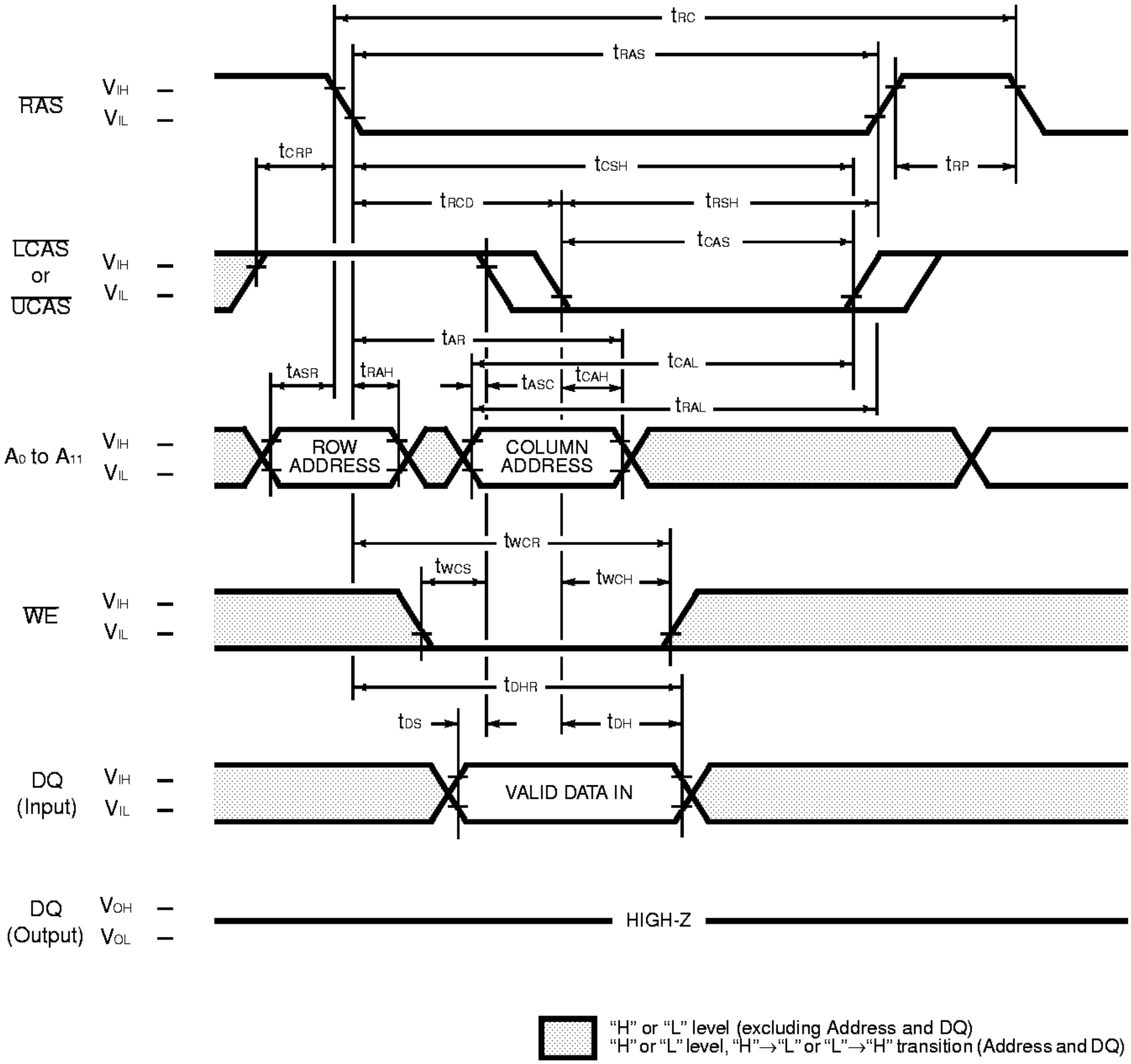
DESCRIPTION

To implement a read operation, a valid address is latched by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. DQ pins are valid when $\overline{RAS}$ and $\overline{CAS}$ are High or until $\overline{OE}$ goes High. The access time is determined by $\overline{RAS}$(t_{RAC}), $\overline{LCAS}$/$\overline{UCAS}$(t_{CAC}), $\overline{OE}$(t_{OEA}) or column addresses (t_{AA}) under the following conditions:

If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (whichever occurs later), access time = t_{OEA}.

However, if either $\overline{LCAS}$/$\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

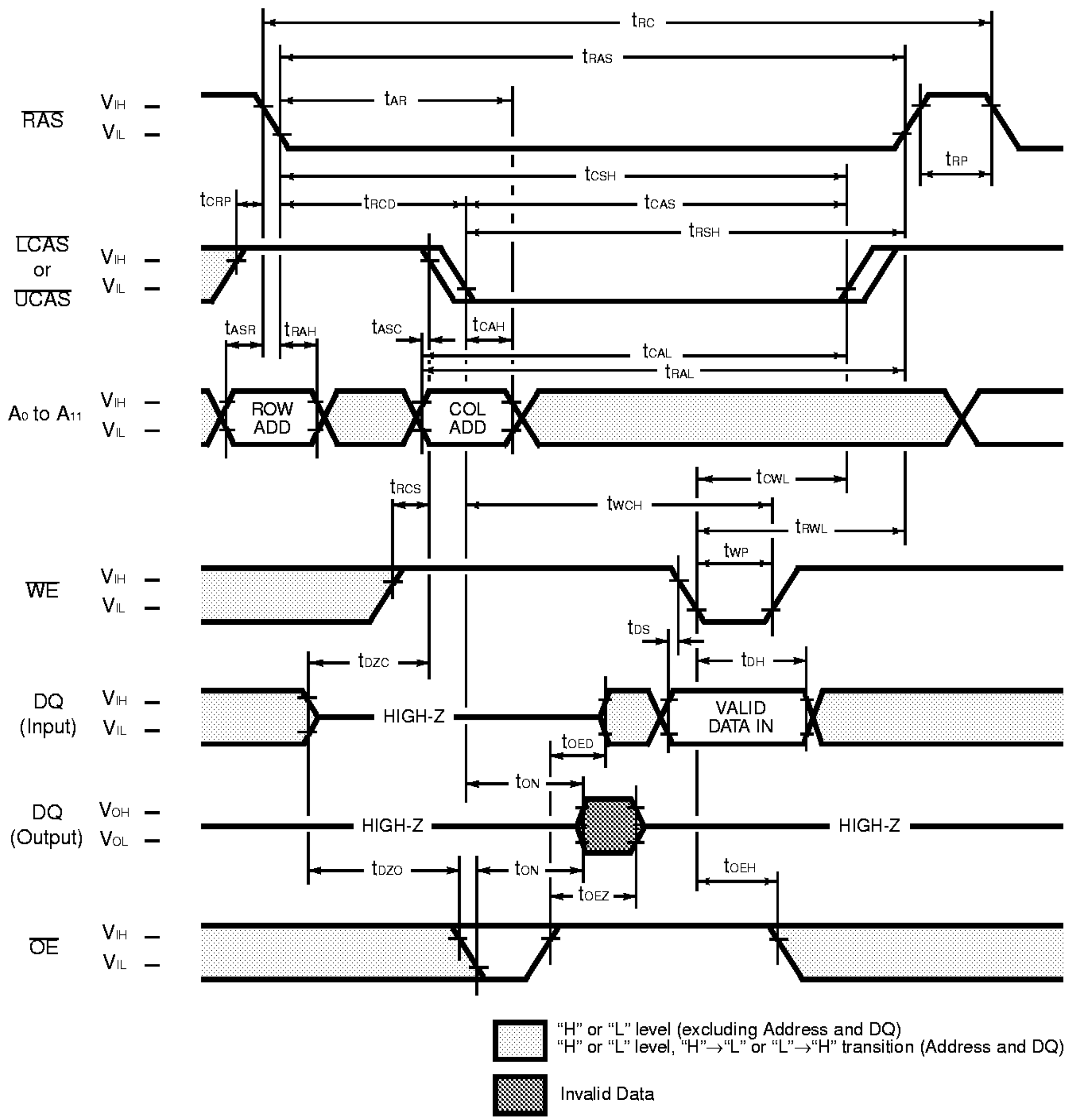
Fig. 6 – EARLY WRITE CYCLE



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

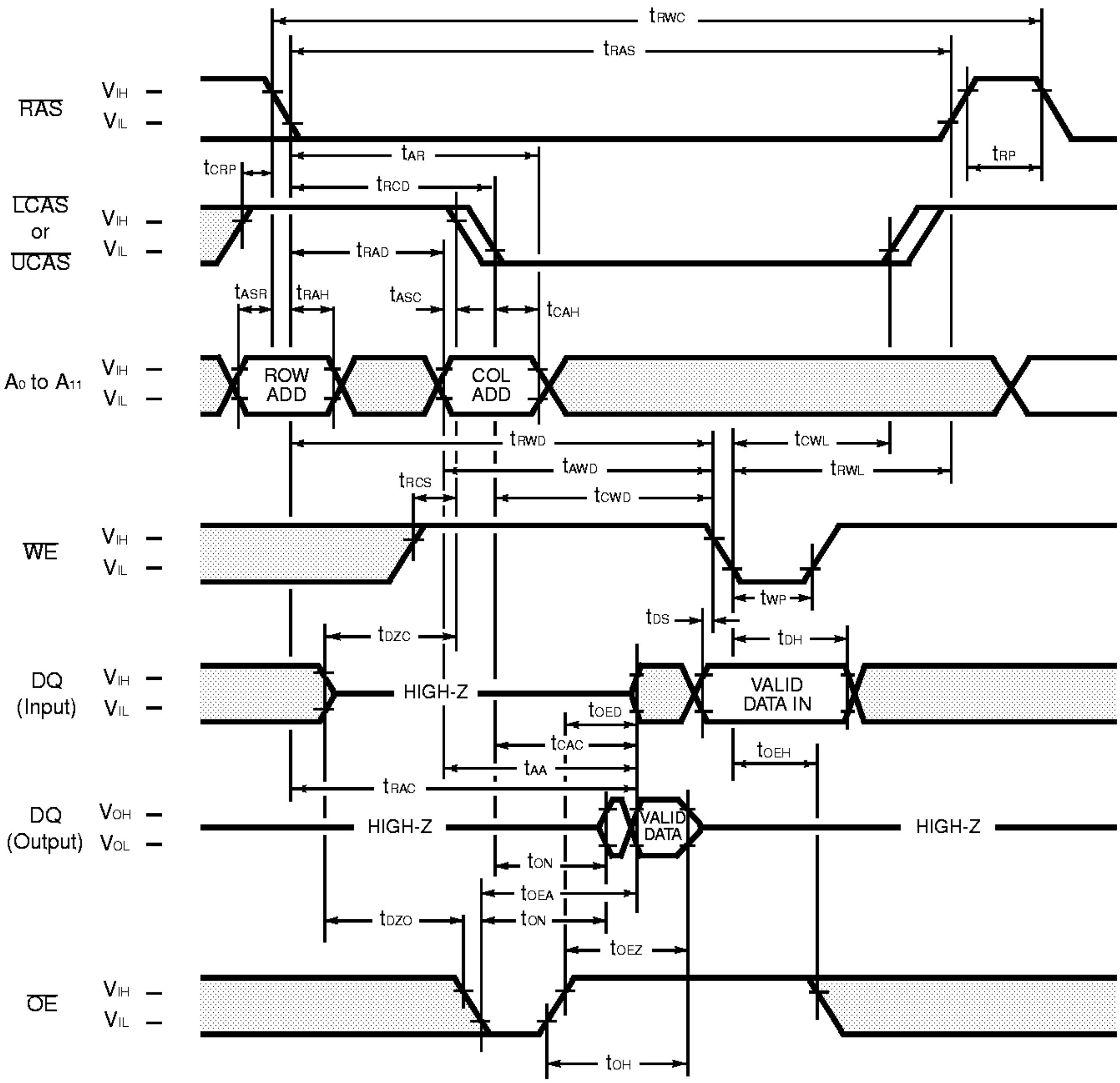
Fig. 7 – DELAYED WRITE CYCLE ($\overline{OE}$ CONTROL)



DESCRIPTION

In the delayed write cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins are latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low (t_{OED} + t_T + t_{DS}).

Fig. 8 – READ-MODIFY-WRITE CYCLE

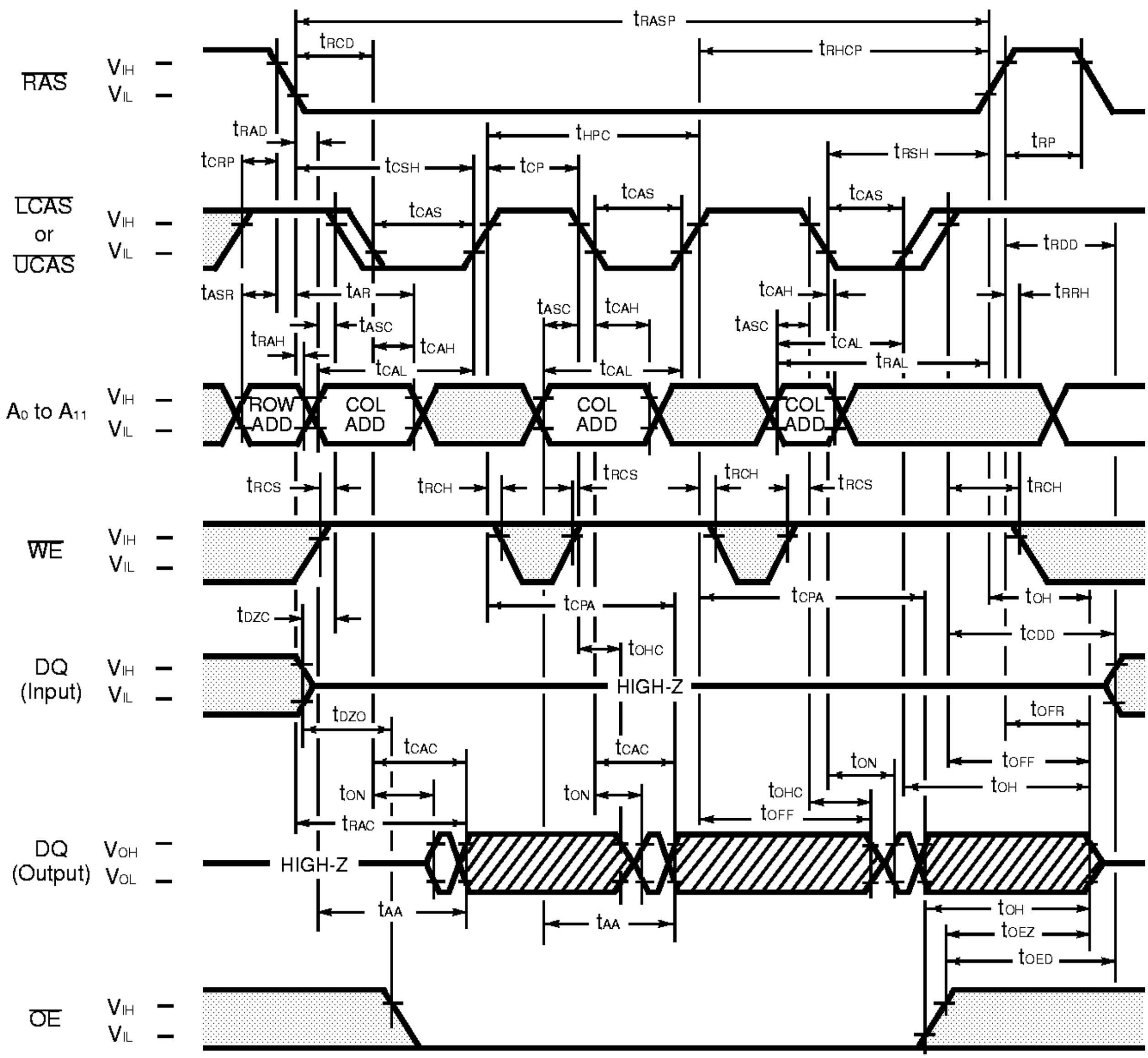


“H” or “L” level (excluding Address and DQ)
“H” or “L” level, “H”→“L” or “L”→“H” transition (Address and DQ)

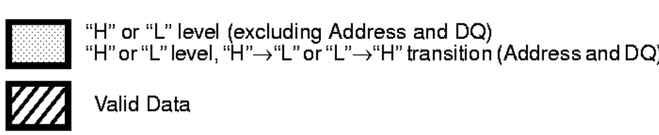
DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 9 – HYPER PAGE MODE READ CYCLE



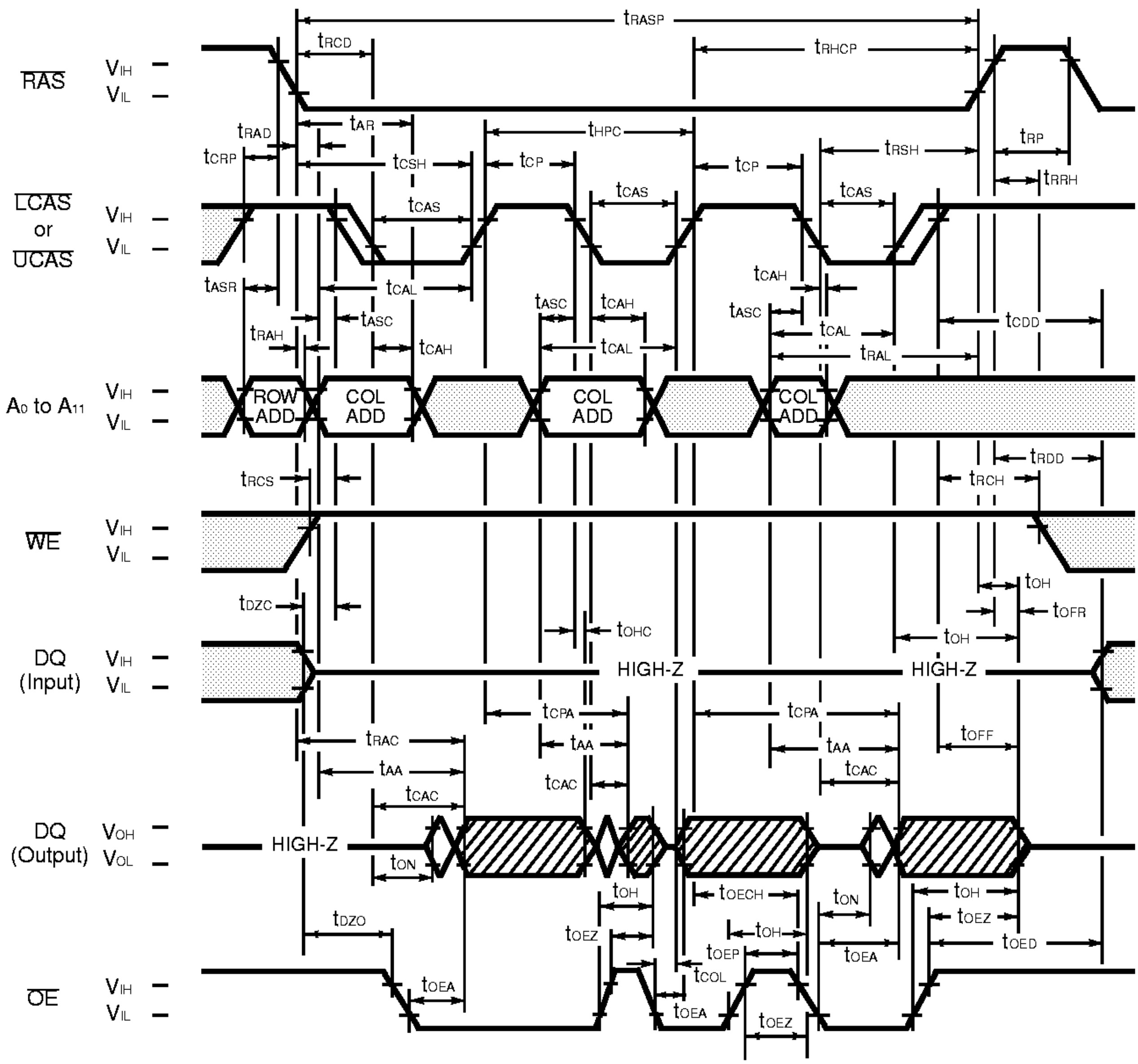
During one cycle is achieved, the input/output timing apply the same manner as the former cycle.



DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address.
This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The address time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.

Fig. 10 – HYPER PAGE MODE READ CYCLE ($\overline{\text{OE}}$ CONTROL)



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

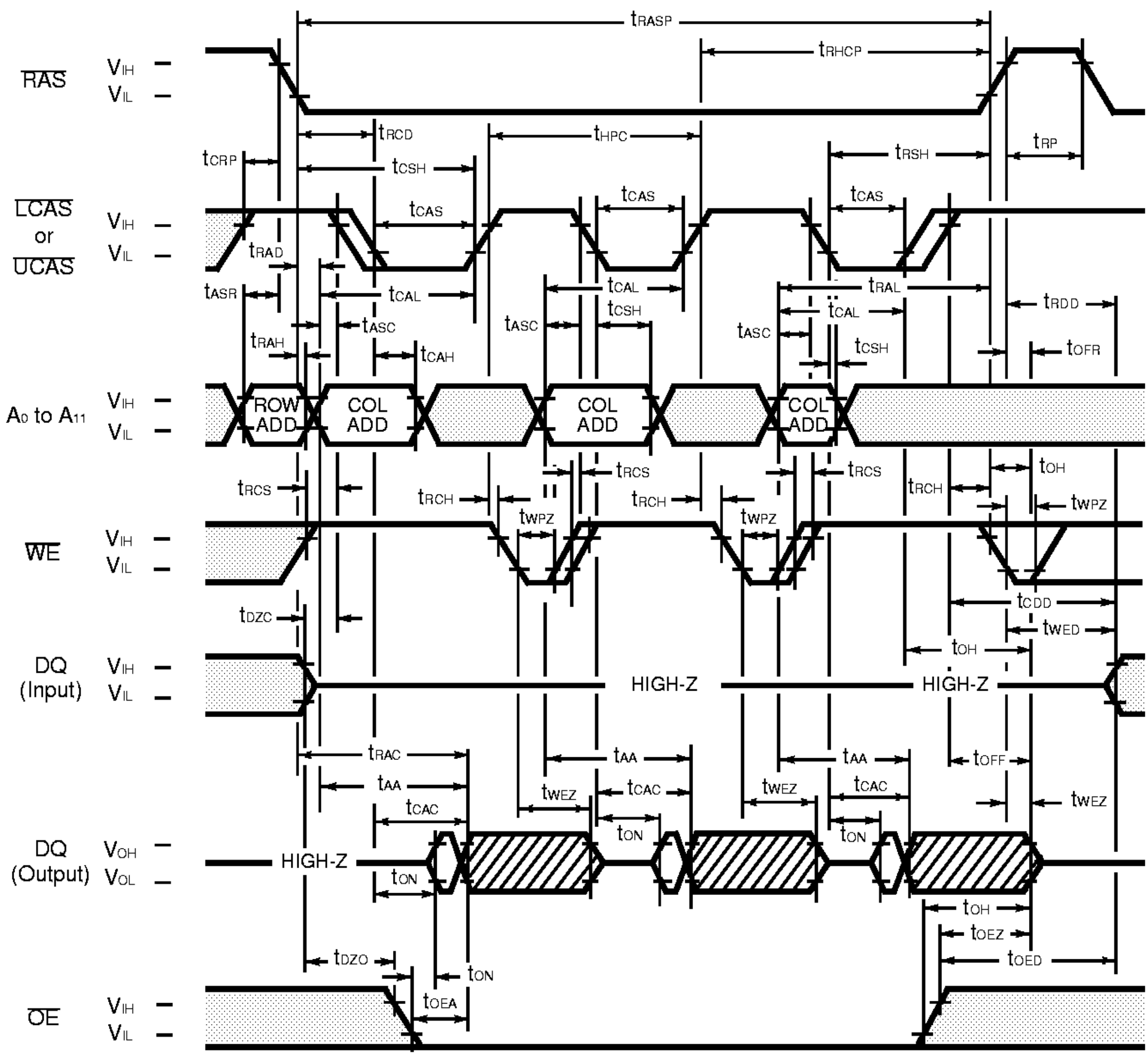
"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H"→"L" or "L"→"H" transition (Address and DQ)

Valid Data

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address.
This operation is performed by strobing in the row address and maintaining $\overline{\text{RAS}}$ at a Low level and $\overline{\text{WE}}$ at a High level during all successive memory cycles in which the row address is latched. The address time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.

Fig. 11 – HYPER PAGE MODE READ CYCLE (W̄Ē CONTROL)



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

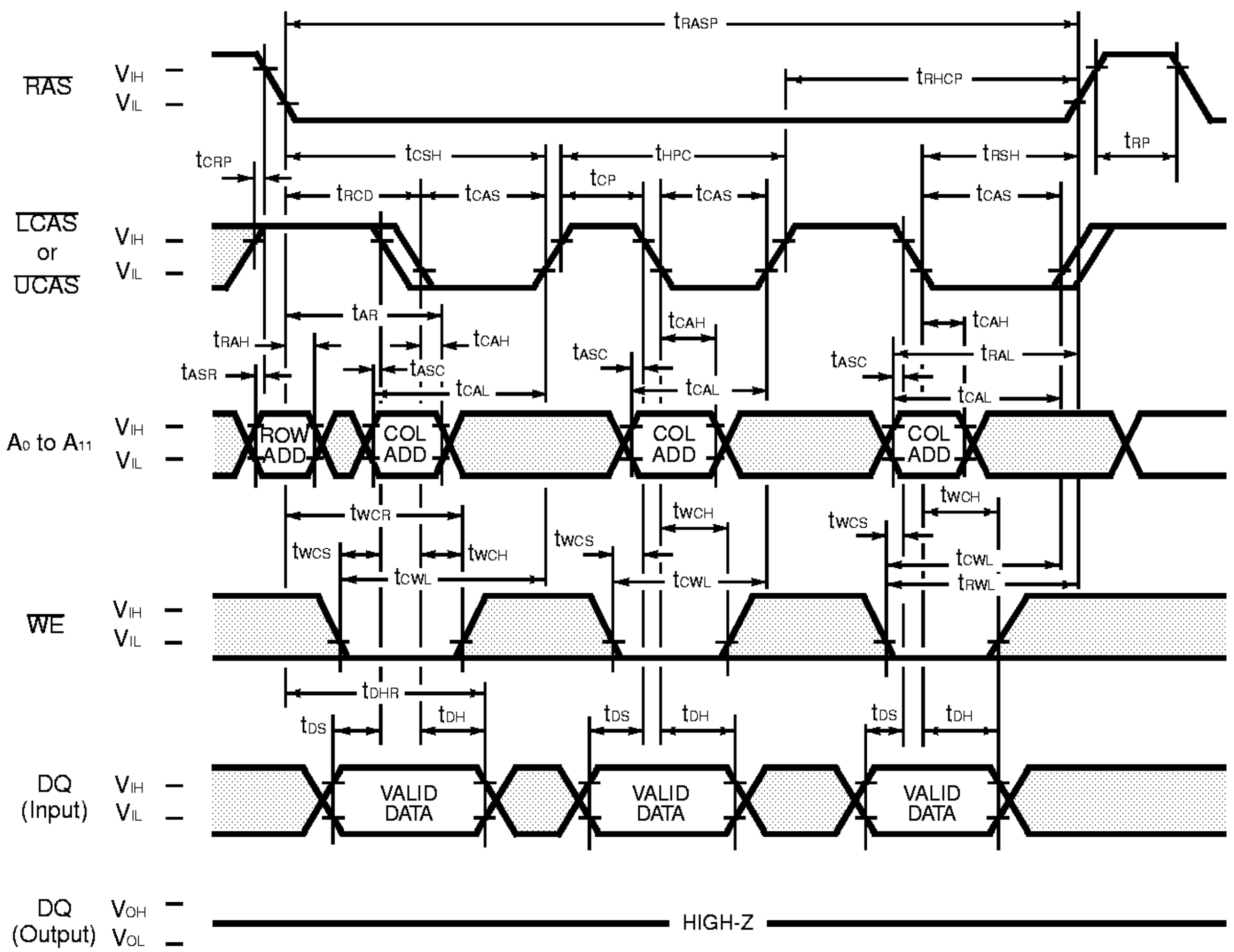
"H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H"→"L" or "L"→"H" transition (Address and DQ)

Valid Data

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address.
This operation is performed by strobing in the row address and maintaining R̄ĀS̄ at a Low level and W̄Ē at a High level during all successive memory cycles in which the row address is latched. The address time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.

Fig. 12 – HYPER PAGE MODE EARLY WRITE CYCLE



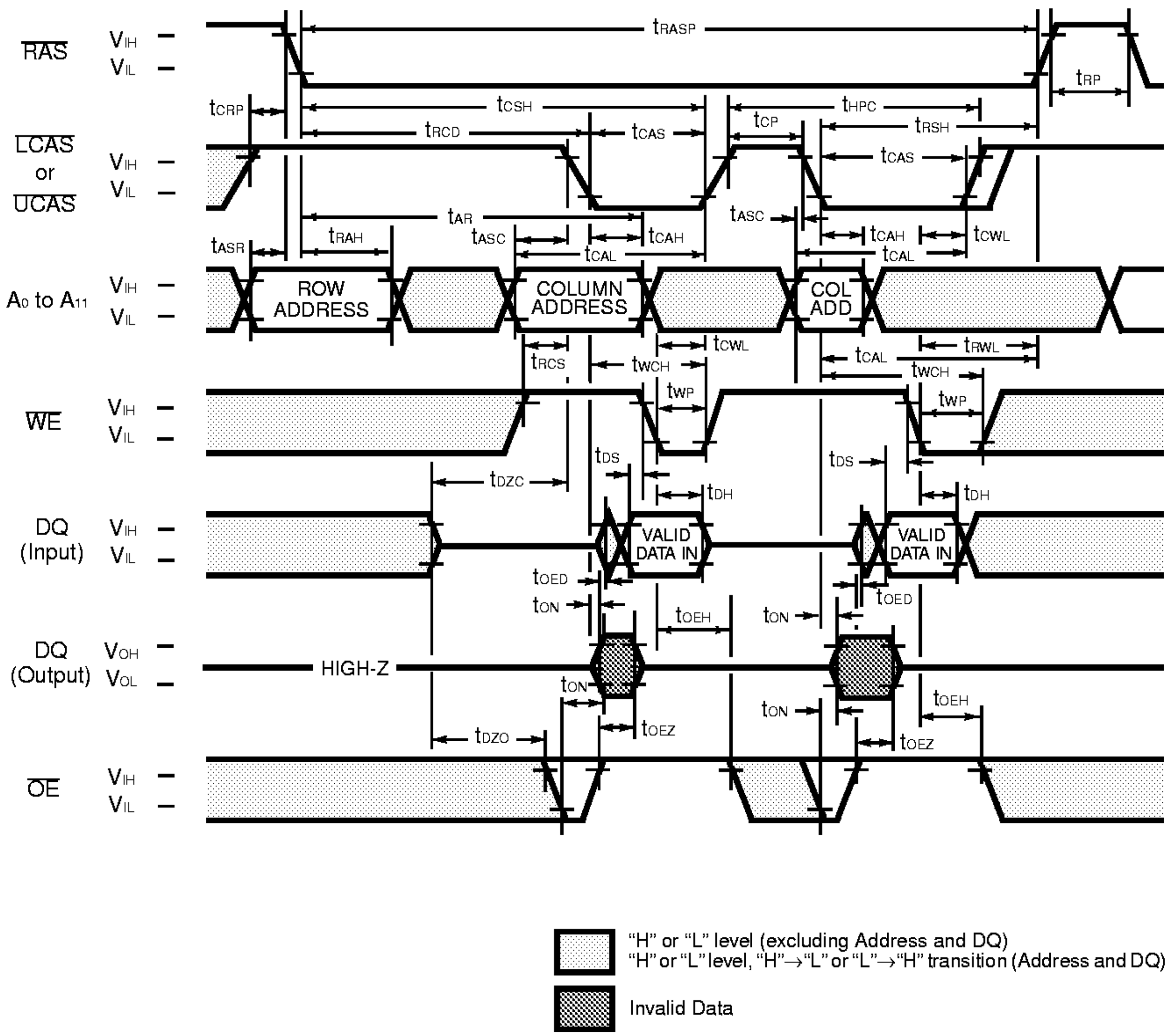
During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

▒ "H" or "L" level (excluding Address and DQ)
"H" or "L" level, "H"→"L" or "L"→"H" transition (Address and DQ)

DESCRIPTION

The hyper page mode early write cycle is executed in the same manner as the hyper page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ_1 to DQ_8 is latched on the falling edge of $\overline{LCAS}$ and one appearing on the DQ_9 to DQ_{16} is latched on the falling edge of $\overline{UCAS}$ and the data is written into the memory. During the hyper page mode early write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, t_{CWL} must be satisfied.

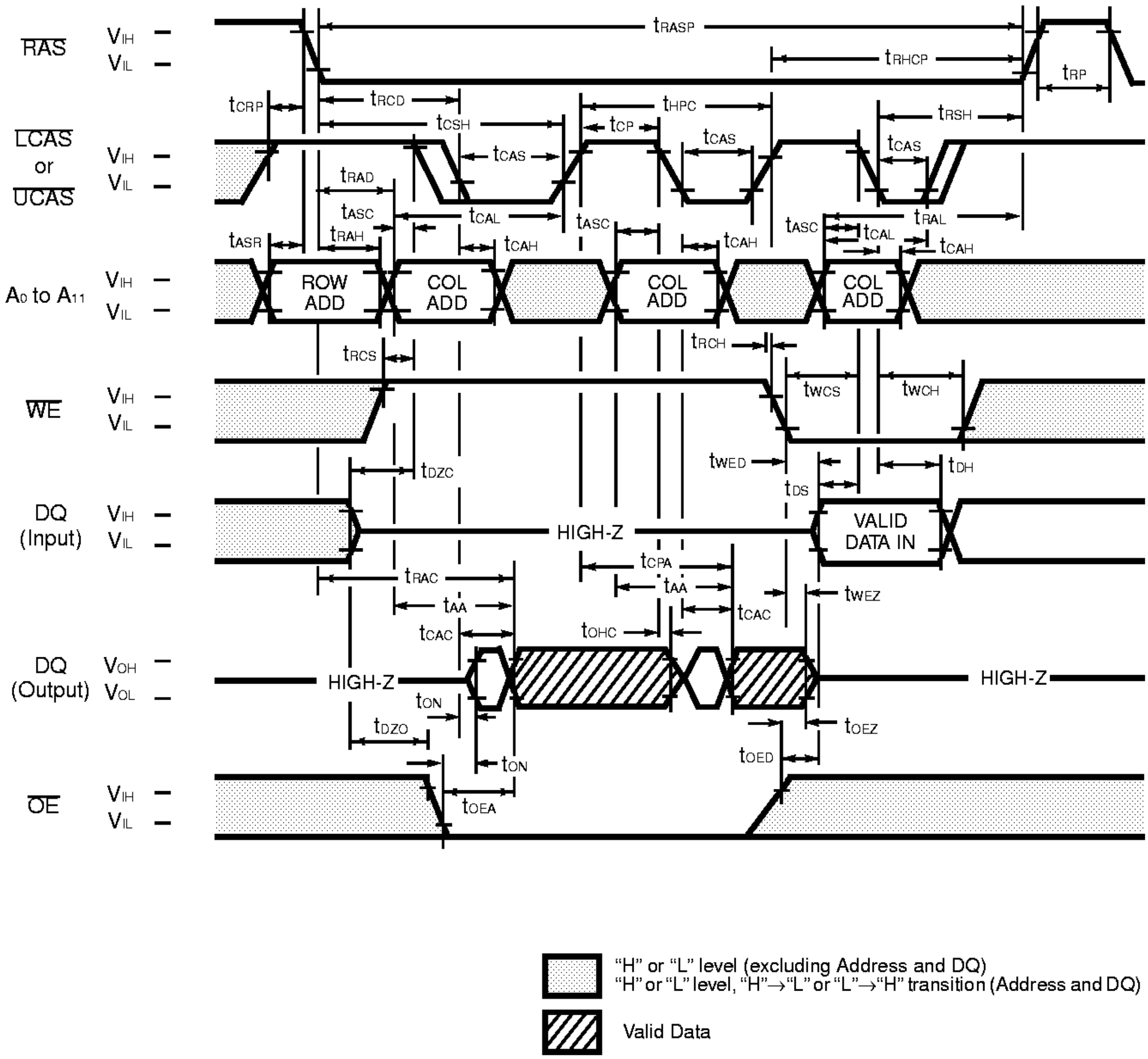
Fig. 13 – HYPER PAGE MODE DELAYED WRITE CYCLE



DESCRIPTION

The hyper page mode delayed write cycle is executed in the same manner as the hyper page mode early write cycle except for the states of WE and OE. Input data on the DQ pins are latched on the falling edge of WE and written into memory. In the hyper page mode delayed write cycle, OE must be changed from Low to High before WE goes Low (t_{OED} + t_T + t_{DS}).

Fig. 14 – HYPER PAGE MODE READ/WRITE MIXED CYCLE



DESCRIPTION

The hyper page mode performs read/write operations repetitively during one $\overline{RAS}$ cycle. At this time, t_{HPC} (min) is invalid.

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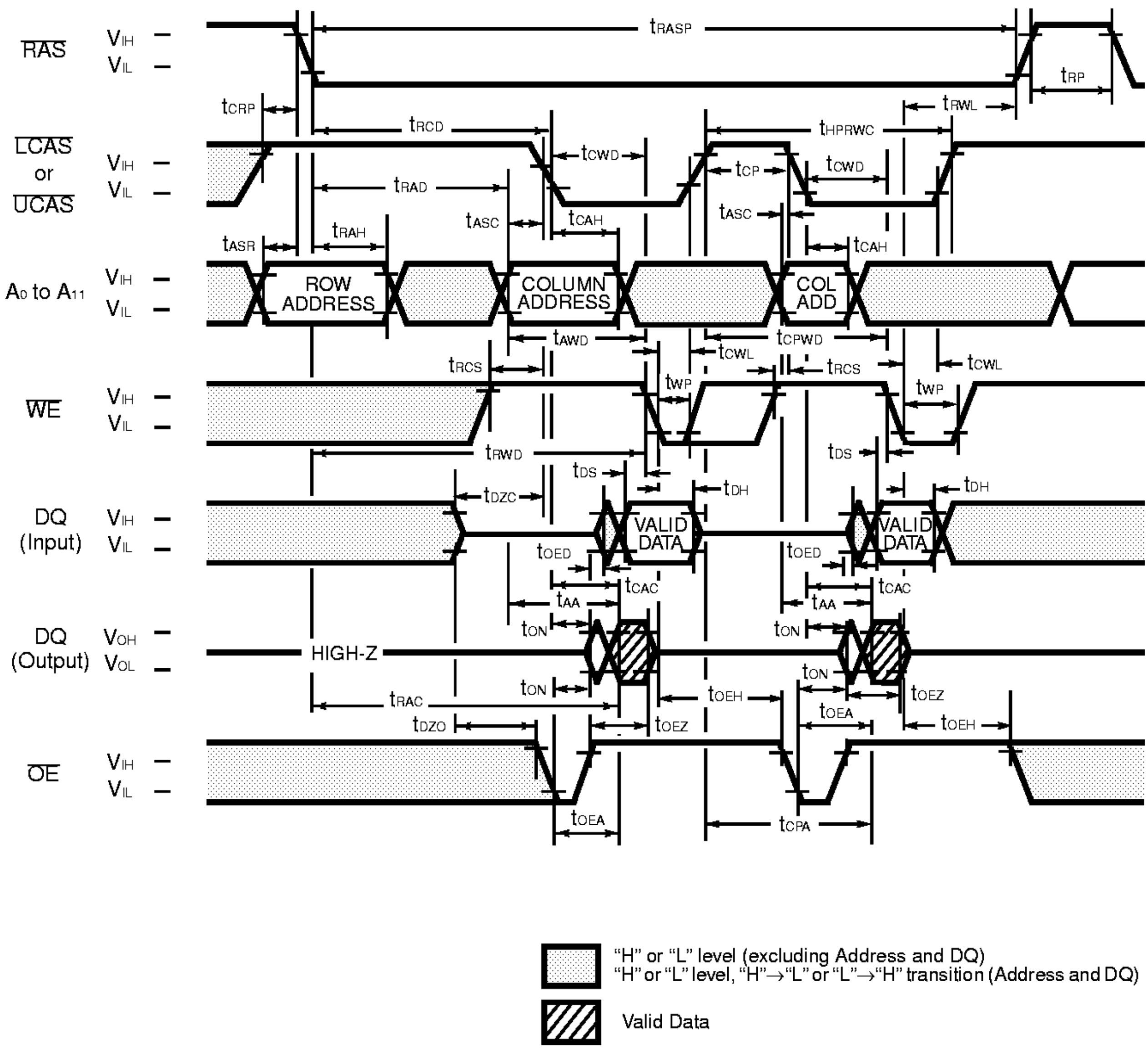
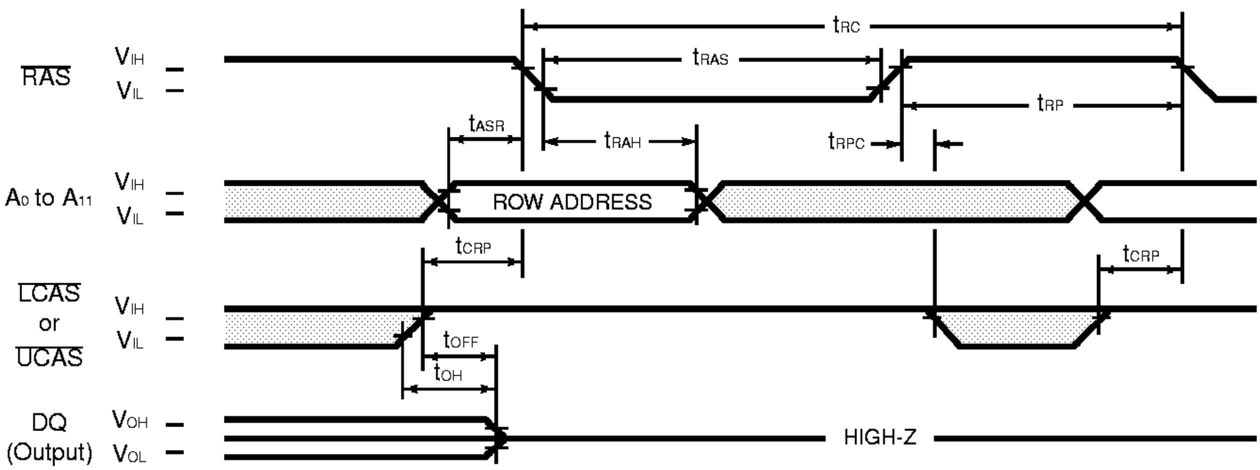
Fig. 15 – HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During the hyper page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input data appears at the DQ pins during a normal cycle.

Fig. 16 – RAS-ONLY REFRESH (WE = OE = “H” or “L”)



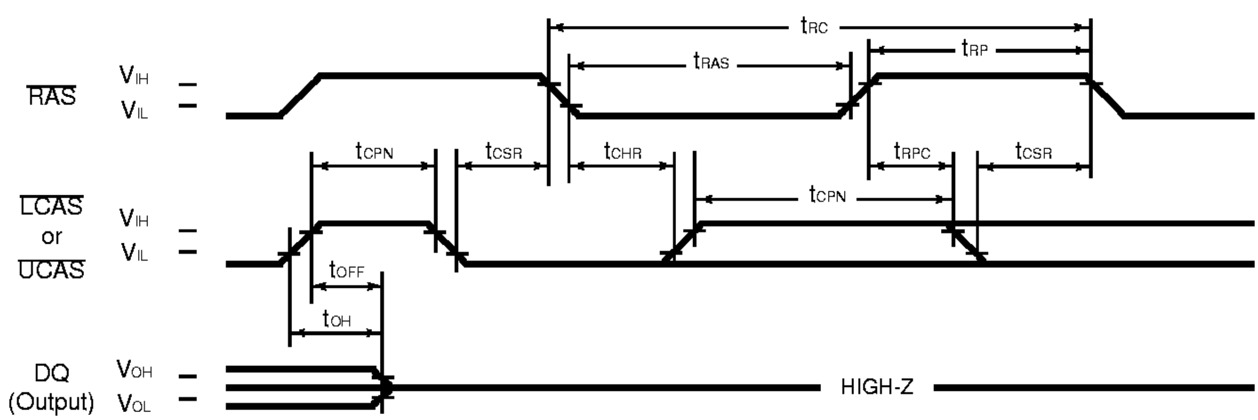
“H” or “L” level (excluding Address and DQ)
“H” or “L” level, “H”→“L” or “L”→“H” transition (Address and DQ)

DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 4,096 row addresses every 65.6-milliseconds. Three refresh modes are available: RAS-only refresh, CAS-before-RAS refresh, and hidden refresh.

RAS-only refresh is performed by keeping RAS Low and LCAS and UCAS High throughout the cycle; the row address to be refreshed is latched on the falling edge of RAS. During RAS-only refresh, DQ pins are kept in a high-impedance state.

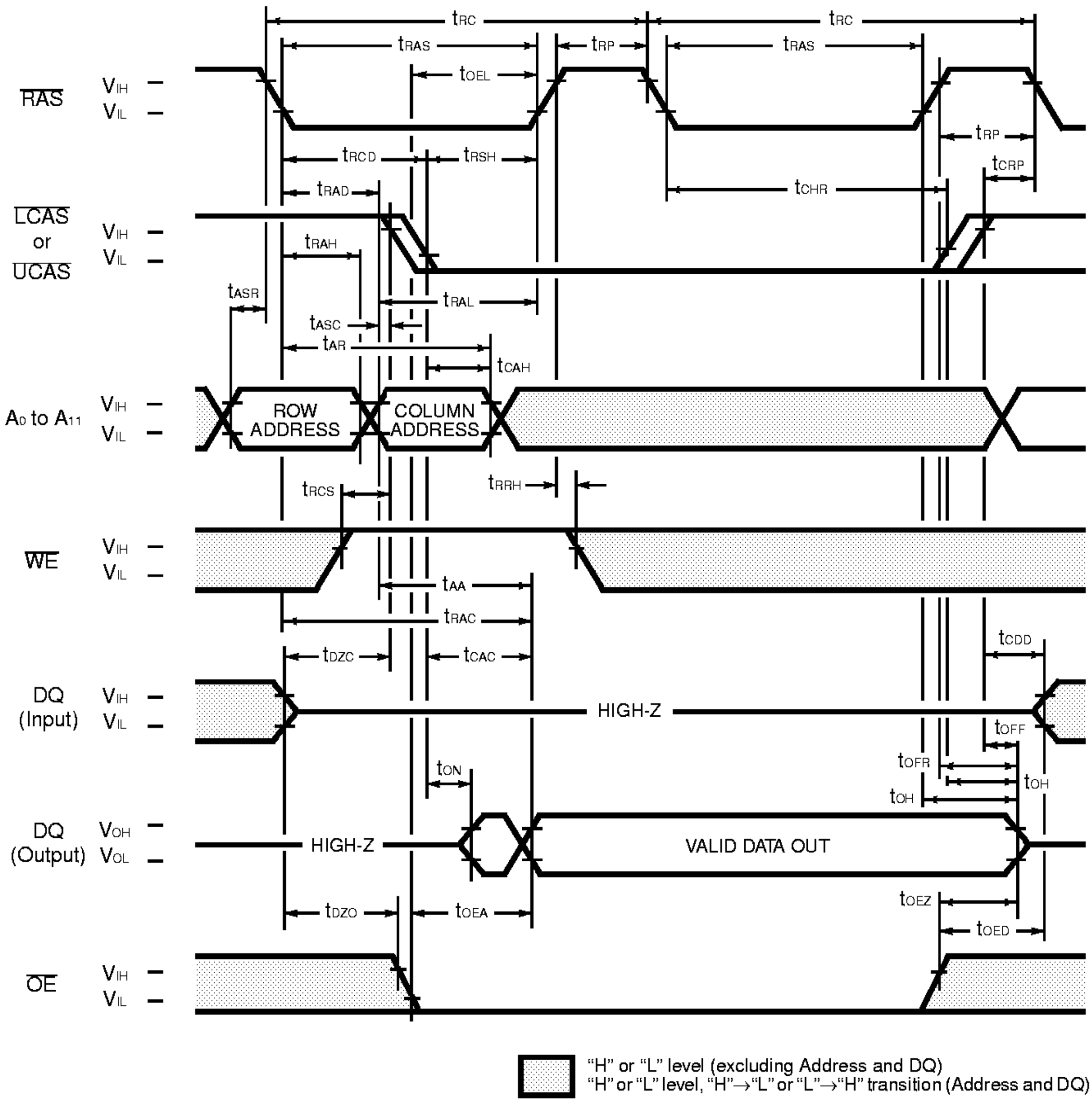
Fig. 17 – CAS-BEFORE-RAS REFRESH (ADDRESSES = WE = OE = “H” or “L”)



DESCRIPTION

CAS-before-RAS refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If LCAS or UCAS is held Low for the specified setup time (t_{CSR}) before RAS goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next CAS-before-RAS refresh operation.

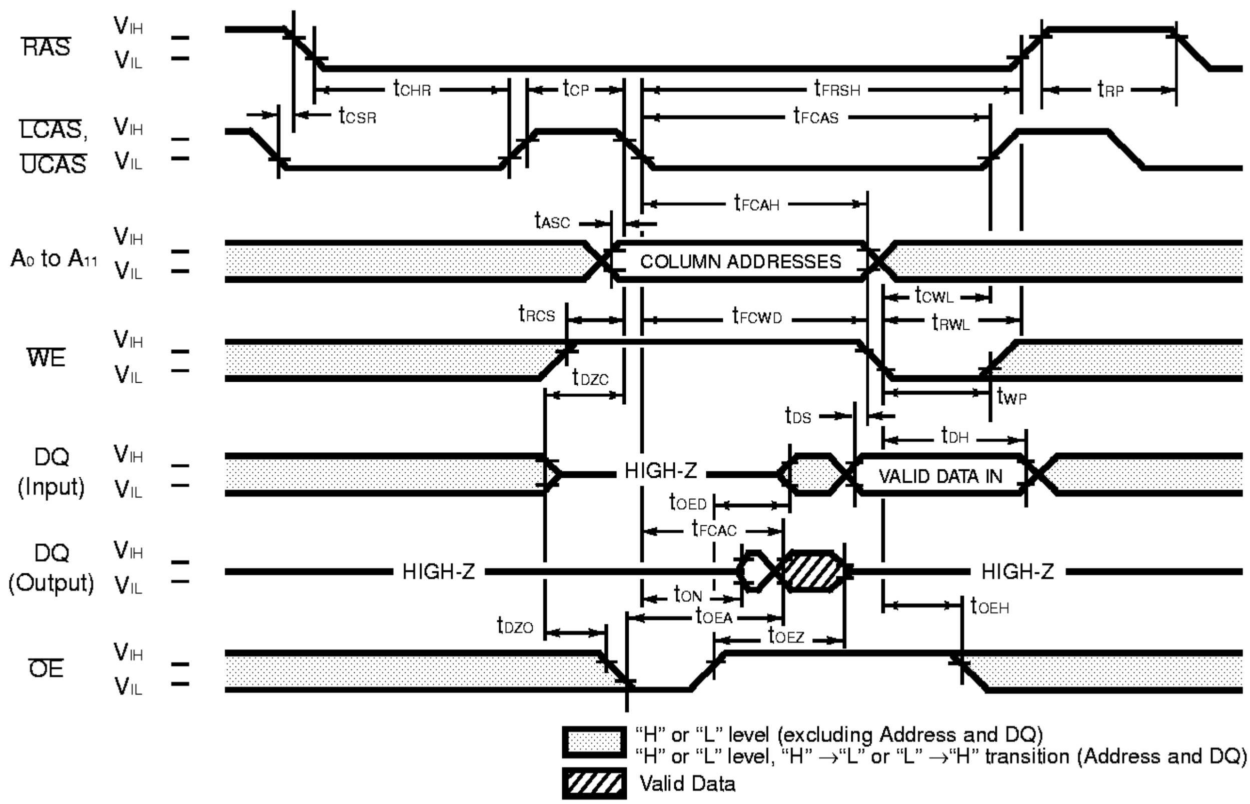
Fig. 18 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{LCAS}$ or $\overline{UCAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 19 – $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the function of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh circuitry. If a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Addresses: Bits A_0 through A_{11} are defined by the on-chip refresh counter.
Column Addresses: Bits A_0 through A_7 are defined by latching levels on A_0 to A_7 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test procedure is as follows;

1) Initialize the internal refresh address counter by using 8 $\overline{\text{RAS}}$-only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 4,096 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test (read-modify-write cycles). Repeat this procedure 4,096 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 4,096 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB8116165B-50		MB8116165B-60		Unit
			Min.	Max.	Min.	Max.	
69	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	45	—	50	ns
70	Column Address Hold Time	t_{FCAH}	35	—	35	—	ns
71	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{FCWD}	63	—	70	—	ns
72	$\overline{\text{CAS}}$ Pulse Width	t_{FCAS}	45	—	50	—	ns
73	$\overline{\text{RAS}}$ Hold Time	t_{FRSH}	45	—	50	—	ns

Note: Assumes that $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle only.

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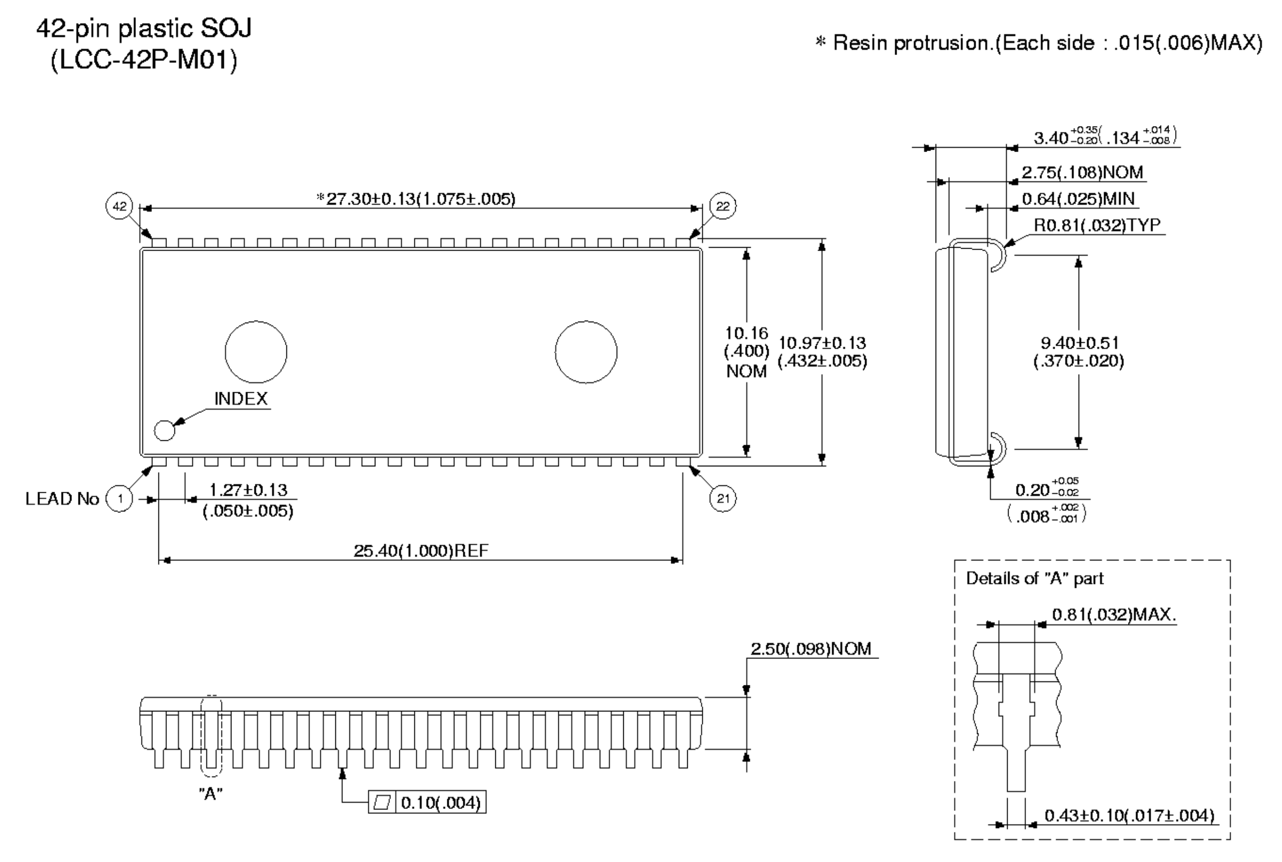
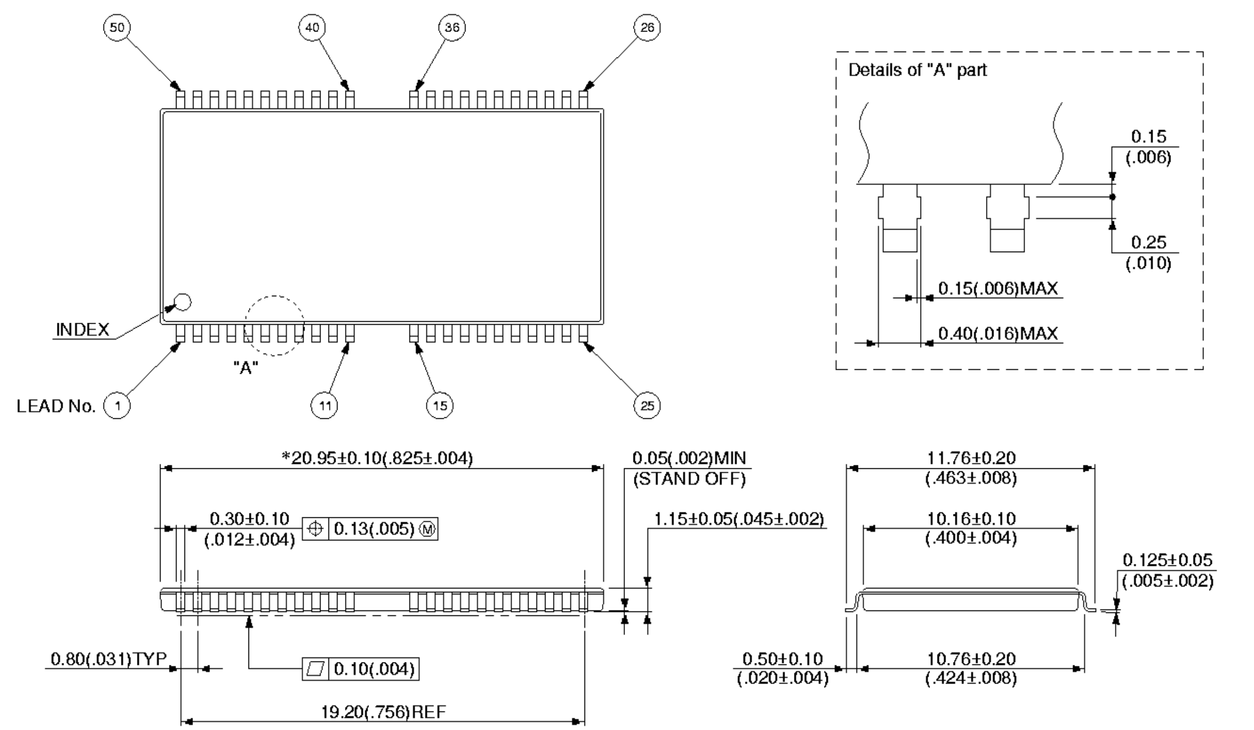
■ PACKAGE DIMENSIONS



Dimensions in mm (inches)

(Continued)

50-pin plastic TSOP (II)
(FPT-50P-M06)



Dimensions in mm (inches)

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