

February 1998

Fast CMOS 16-Bit Registers (Three-State)

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16374T**
 - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
 - **Power Off Disable Outputs Permit "Live Insertion"**
 - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162374T**
 - **Balanced Output Drivers: ±24mA**
 - **Reduced System Switching Noise**
 - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162H374T**
 - **Bus Hold Retains Last Active Bus State During Three-State**
 - **Eliminates the Need for External Pull-up Resistors**

Description

These Devices are 16-bit octal registers designed with 16 D-type flip-flops with a buffered common clock and three-state outputs. The Output Enable (\overline{xOE}) and clock ($xCLK$) controls are organized to operate as two 8-bit registers or one 16-bit register. When \overline{OE} is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The CD74FCT16374T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162374T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The CD74FCT162H374T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Ordering Information

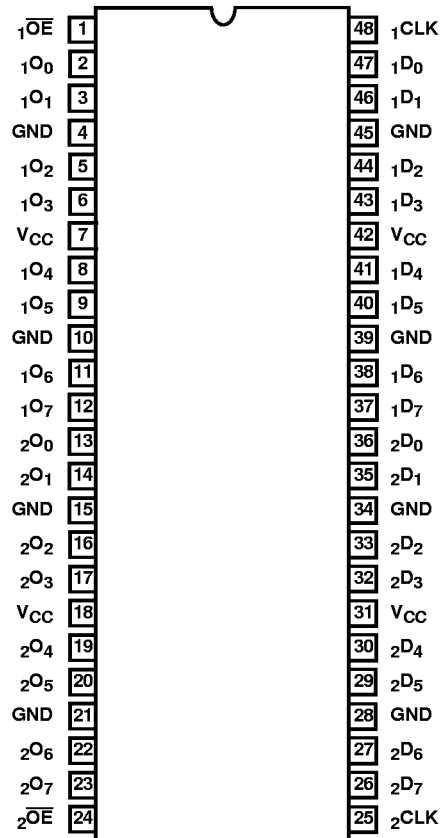
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|--------------------|------------------|-------------|-----------|
| CD74FCT16374ATMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT16374ATSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT16374CTMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT16374CTSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT16374DTMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT16374DTSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT16374ETMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT16374ETSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT16374TMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT16374TSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT162374ATMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT162374ATSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT162374CTMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT162374CTSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT162374DTMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT162374DTSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT162374ETMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT162374ETSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT162374TMT | -40 to 85 | 48 Ld TSSOP | M48.240-P |
| CD74FCT162374TSM | -40 to 85 | 48 Ld SSOP | M48.300-P |
| CD74FCT162H374ATMT | -40 to 85 | 48 Ld TSSOP | M56.240-P |
| CD74FCT162H374ATSM | -40 to 85 | 48 Ld SSOP | M56.300-P |
| CD74FCT162H374CTMT | -40 to 85 | 48 Ld TSSOP | M56.240-P |
| CD74FCT162H374CTSM | -40 to 85 | 48 Ld SSOP | M56.300-P |
| CD74FCT162H374DTMT | -40 to 85 | 48 Ld TSSOP | M56.240-P |
| CD74FCT162H374DTSM | -40 to 85 | 48 Ld SSOP | M56.300-P |
| CD74FCT162H374ETMT | -40 to 85 | 48 Ld TSSOP | M56.240-P |
| CD74FCT162H374ETSM | -40 to 85 | 48 Ld SSOP | M56.300-P |
| CD74FCT162H374TMT | -40 to 85 | 48 Ld TSSOP | M56.240-P |
| CD74FCT162H374TSM | -40 to 85 | 48 Ld SSOP | M56.300-P |

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

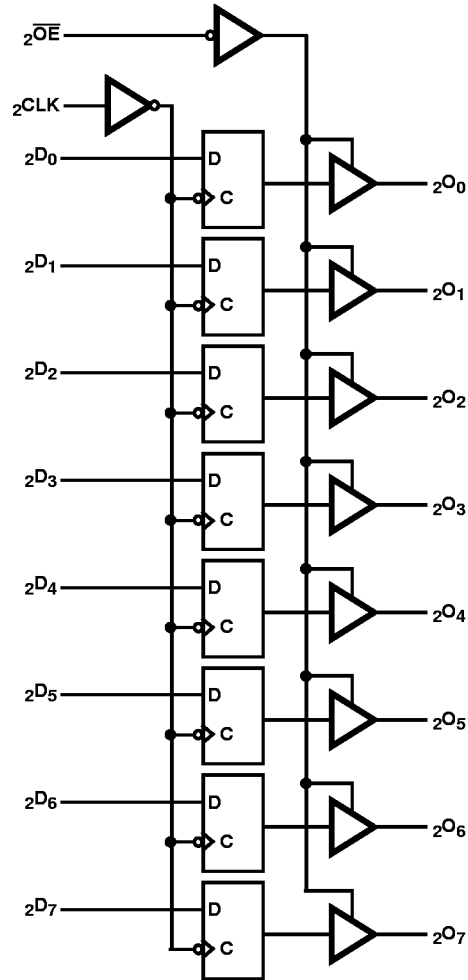
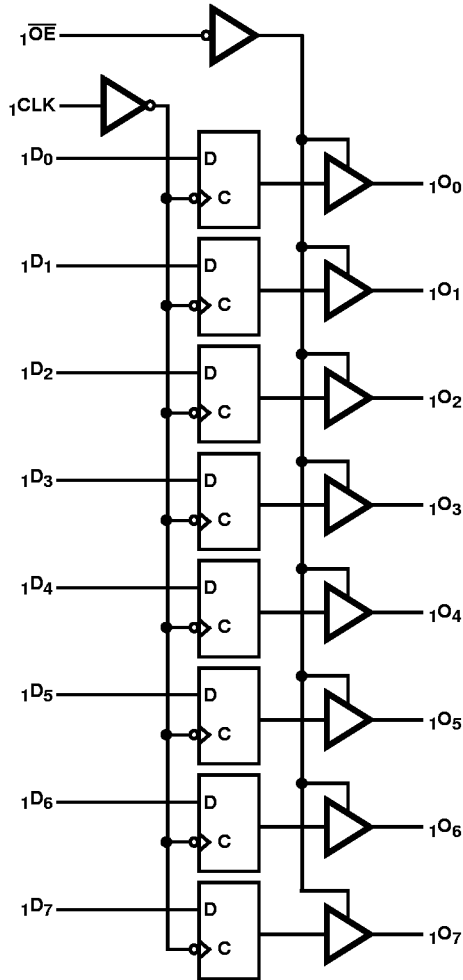
CD74FCT16374T, CD74FCT162374T, CD74FCT162H374T

Pinout

CD74FCT16374T, CD74FCT162374T, CD74FCT162H374T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

| FUNCTION | INPUTS | | | OUTPUTS |
|---------------|-------------------|-------------------|------------------|---------|
| | $x\overline{D}_x$ | $x\overline{CLK}$ | $x\overline{OE}$ | xO_x |
| High-Z | X | L | H | Z |
| | X | H | H | Z |
| Load Register | L | ↑ | L | L |
| | H | ↑ | L | H |
| | L | ↑ | H | Z |
| | H | ↑ | H | Z |

NOTE:

- 20. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance
- ↑ = LOW-to-HIGH Transition

Pin Descriptions

| PIN NAME | DESCRIPTION |
|-------------------|---|
| $x\overline{OE}$ | Three-State Output Enable Inputs (Active LOW) |
| $x\overline{CLK}$ | Clock Inputs |
| $x\overline{D}_x$ | Inputs (Note 2) |
| xO_x | Three-State Outputs |
| GND | Ground |
| V _{CC} | Power |

NOTE:

- 21. For the CD74FCT162H374T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

CD74FCT16374T, CD74FCT162374T, CD74FCT162H374T

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
 TSSOP Package 94
 SSOP Package 76
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

22. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

| PARAMETER | SYMBOL | (NOTE 4) TEST CONDITIONS | MIN | (NOTE 5) TYP | MAX | UNITS | |
|---|------------------|---|---------------------------|-----------------|------|-------|----|
| DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 5.0V ±10% | | | | | | | |
| Input HIGH Voltage | V _{IH} | Guaranteed Logic HIGH Level | 2.0 | - | - | V | |
| Input LOW Voltage | V _{IL} | Guaranteed Logic LOW Level | - | - | 0.8 | V | |
| Input HIGH Current | I _{IH} | Standard Input (Note 7) V _{CC} = Max | | | 1 | μA | |
| | | V _{IN} = V _{CC} | - | - | | | |
| Input HIGH Current | I _{IH} | Standard I/O (Note 7) V _{CC} = Max | | | 1 | μA | |
| | | V _{IN} = V _{CC} | - | - | | | |
| Input HIGH Current | I _{IH} | Bus Hold Input (Note 8) V _{CC} = Max | | | ±100 | μA | |
| | | V _{IN} = V _{CC} | - | - | | | |
| Input HIGH Current | I _{IH} | Bus Hold I/O (Note 8) V _{CC} = Max | | | ±100 | μA | |
| | | V _{IN} = V _{CC} | - | - | | | |
| Input LOW Current | I _{IL} | Standard Input (Note 7) V _{CC} = Min | | | -1 | μA | |
| | | V _{IN} = GND | - | - | | | |
| Input LOW Current | I _{IL} | Standard I/O (Note 7) V _{CC} = Min | | | -1 | μA | |
| | | V _{IN} = GND | - | - | | | |
| Input LOW Current | I _{IL} | Bus Hold Input (Note 8) V _{CC} = Min | | | ±100 | μA | |
| | | V _{IN} = GND | - | - | | | |
| Input LOW Current | I _{IL} | Bus Hold I/O (Note 8) V _{CC} = Min | | | ±100 | μA | |
| | | V _{IN} = GND | - | - | | | |
| Bus Hold Sustain Current | I _{BHH} | Bus Hold Input (Note 8) V _{CC} = Min | V _{IN} = 2.0V | -50 | - | - | μA |
| | I _{BHL} | | V _{IN} = 0.8V | 50 | - | - | μA |
| High Impedance Output Current (Three-State) (Note 9) | I _{OZH} | V _{CC} = Max | V _{OUT} = 2.7V | - | - | 1 | μA |
| | I _{OZL} | | V _{OUT} = 0.5V | - | - | -1 | μA |
| Clamp Diode Voltage | V _{IK} | V _{CC} = Min, I _{IN} = -18mA | - | -0.7 | -1.2 | V | |
| Short Circuit Current | I _{OS} | V _{CC} = Max (Note 6), V _{OUT} = GND | -80 | -140 | -200 | mA | |
| Output Drive Current | I _O | V _{CC} = Max (Note 6), V _{OUT} = 2.5V | -50 | - | -180 | mA | |
| Input Hysteresis | V _H | | - | 100 | - | mV | |
| CD74FCT16374T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range | | | | | | | |
| Output HIGH Voltage | V _{OH} | V _{CC} = Min, V _{IN} = V _{IH} or V _{IL} | I _{OH} = -3.0mA | 2.5 | 3.5 | - | V |
| | | | I _{OH} = -15.0mA | 2.4 | 3.5 | - | V |
| | | | I _{OH} = -32.0mA | 2.0 | 3.0 | - | V |

CD74FCT16374T, CD74FCT162374T, CD74FCT162H374T

Electrical Specifications (Continued)

| PARAMETER | SYMBOL | (NOTE 4) TEST CONDITIONS | | MIN | (NOTE 5) TYP | MAX | UNITS |
|--|------------------|--|--|-----|-----------------|-------------------|--------|
| | | | | | | | |
| Output LOW Voltage | V _{OL} | V _{CC} = Min, V _{IN} = V _{IH} or V _{IL} | I _{OL} = 64mA | - | 0.2 | 0.55 | V |
| Power Down Disable | I _{OFF} | V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V | | - | - | ±100 | μA |
| CD74FCT162374T, CD74FCT162H374T, OUTPUT DRIVE SPECIFICATIONS Over the Operating Range | | | | | | | |
| Output HIGH Voltage | V _{OH} | V _{CC} = Min, V _{IN} = V _{IH} or V _{IL} | I _{OH} = -24.0mA | 2.4 | 3.3 | - | V |
| Output LOW Voltage | V _{OL} | V _{CC} = Min, V _{IN} = V _{IH} or V _{IL} | I _{OL} = 24mA | - | 0.3 | 0.55 | V |
| Output LOW Current | I _{ODL} | V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 6) | | 60 | 115 | 150 | mA |
| Output HIGH Current | I _{ODH} | V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V (Note 6) | | -60 | -115 | -150 | mA |
| CAPACITANCE T _A = 25°C, f = 1MHz | | | | | | | |
| Input Capacitance (Note 10) | C _{IN} | V _{IN} = 0V | | - | 4.5 | 6 | pF |
| Output Capacitance (Note 10) | C _{OUT} | V _{OUT} = 0V | | - | 5.5 | 8 | pF |
| POWER SUPPLY SPECIFICATIONS | | | | | | | |
| Quiescent Power Supply Current | I _{CC} | V _{CC} = Max | V _{IN} = GND or V _{CC} | - | 0.1 | 500 | μA |
| Supply Current per Input at TTL HIGH | ΔI _{CC} | V _{CC} = Max | V _{IN} = 3.4V (Note 12) | - | 0.5 | 1.5 | mA |
| Supply Current per Input per MHz (Note 12) | I _{CCD} | V _{CC} = Max, Outputs Open xOE = GND One Bit Toggling 50% Duty Cycle | V _{IN} = V _{CC} V _{IN} = GND | - | 60 | 100 | μA/MHz |
| Total Power Supply Current (Note 14) | I _C | V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle xOE = GND f _I = 5MHz, 50% Duty Cycle One Bit Toggling | V _{IN} = V _{CC} V _{IN} = GND | - | 0.6 | 1.5 (Note 13) | mA |
| | | | V _{IN} = 3.4V V _{IN} = GND | - | 1.1 | 3.0 (Note 13) | mA |
| | | V _{CC} = Max, Outputs Open f _{CP} = 10MHz, 50% Duty Cycle xOE = GND 16 Bits Toggling f _I = 2.5MHz, 50% Duty Cycle | V _{IN} = V _{CC} V _{IN} = GND | - | 3.0 | 5.5 (Note 13) | mA |
| | | | V _{IN} = 3.4V V _{IN} = GND | - | 7.5 | 19.0 (Note 13) | mA |

Switching Specifications Over Operating Range

| PARAMETER | SYMBOL | (NOTE 15) TEST CONDITIONS | T | | AT | | CT | | DT | | ET | | UNITS |
|--|--|--|------------------|------|------------------|-----|------------------|-----|------------------|-----|------------------|-----|-------|
| | | | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | |
| | | | | | | | | | | | | | |
| CD74FCT16374T, CD74FCT162374T, CD74FCT162H374T | | | | | | | | | | | | | |
| Propagation Delay xCLK _X to xO _X | t _{PLH} , t _{PHL} | C _L = 50pF R _L = 500Ω | 2.0 | 10.0 | 2.0 | 6.5 | 2.0 | 5.2 | 2.0 | 4.2 | 1.5 | 3.7 | ns |
| Output Enable Time xOE to xO _X | t _{PZH} , t _{PZL} | | 1.5 | 12.5 | 1.5 | 6.5 | 1.5 | 5.5 | 1.5 | 4.8 | 1.5 | 4.4 | ns |
| Output Disable Time (Note 17) xOE to xO _X | t _{PHZ} , t _{PLZ} | FCT16374T, FCT162374T | 1.5 | 8.0 | 1.5 | 5.5 | 1.5 | 5.0 | 1.5 | 4.0 | 1.5 | 3.6 | ns |
| | | FCT162H374T | 1.5 | 8.0 | 1.5 | 5.5 | 1.5 | 5.0 | 1.5 | 4.0 | 1.5 | 4.0 | ns |
| Setup Time HIGH or LOW, xD _X to xCLK | t _{SU} | | 2.0 | - | 2.0 | - | 2.0 | - | 2.0 | - | 1.5 | - | ns |

CD74FCT16374T, CD74FCT162374T, CD74FCT162H374T

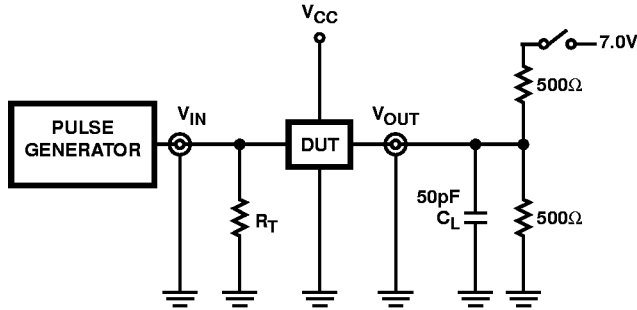
Switching Specifications Over Operating Range (Continued)

| PARAMETER | SYMBOL | (NOTE 15) TEST CONDITIONS | T | | AT | | CT | | DT | | ET | | UNITS |
|--|-------------|--|------------------|-----|------------------|-----|------------------|-----|------------------|-----|------------------|-----|-------|
| | | | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | (NOTE 16) MIN | MAX | |
| Hold Time HIGH or LOW, χ D χ to χ CLK | t_H | $C_L = 50\text{pF}$ $R_L = 500\Omega$ | 1.5 | - | 1.5 | - | 1.5 | - | 1.0 | - | 0.0 | - | ns |
| χ CLK Pulse Width HIGH or LOW (Note 17) | t_W | | 7.0 | - | 5.0 | - | 5.0 | - | 3.0 | - | 3.0 | - | ns |
| Output Skew (Note 18) | $t_{SK(O)}$ | | - | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | ns |

NOTES:

23. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
24. Typical values are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading, except as noted.
25. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
26. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
27. Pins with Bus Hold are identified in the pin description.
28. This specification does not apply to bidirectional functionalities with Bus Hold.
29. This parameter is determined by device characterization but is not production tested.
30. Per TTL driven input ($V_{IN} = 3.4\text{V}$); all other inputs at V_{CC} or GND.
31. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
32. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
33. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
34. See test circuit and wave forms.
35. Minimum limits are guaranteed but not tested on Propagation Delays.
36. This parameter is guaranteed but not production tested.
37. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



| SWITCH POSITION | |
|--------------------------------------|--------|
| TEST | SWITCH |
| t_{PLZ}, t_{PZL} | Closed |
| $t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$ | Open |

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

38. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 6. TEST CIRCUIT

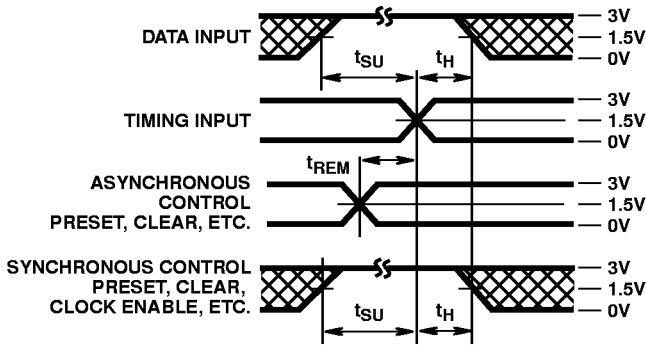


FIGURE 7. SETUP, HOLD, AND RELEASE TIMING

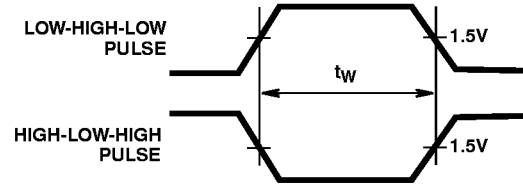


FIGURE 8. PULSE WIDTH

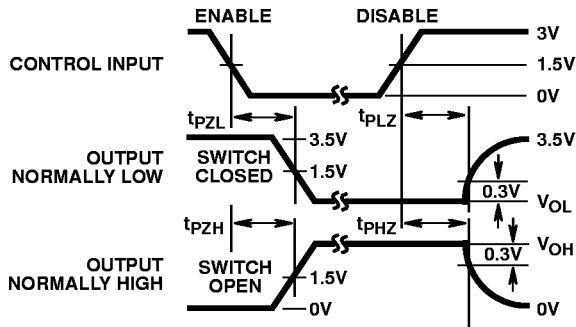


FIGURE 9. ENABLE AND DISABLE TIMING

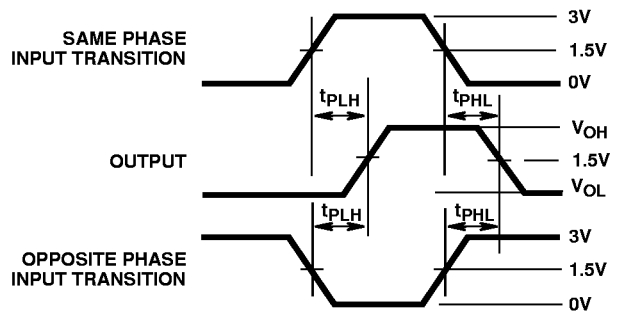


FIGURE 10. PROPAGATION DELAY