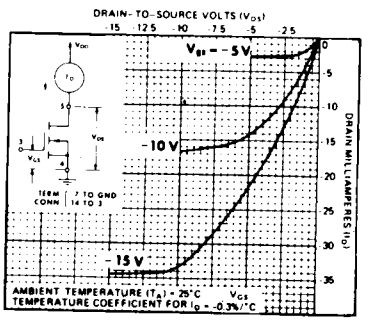
CMOS DUAL COMPLEMENTARY PAIR PLUS INVERTER

FEATURES

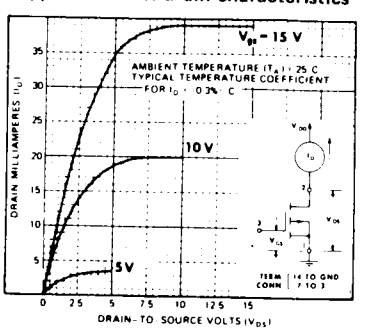
- Low Output Impedance
- Extremely High Input Impedance
- Single Supply Operation - Positive or Negative
- All Inputs Diode-Protected

DESCRIPTION

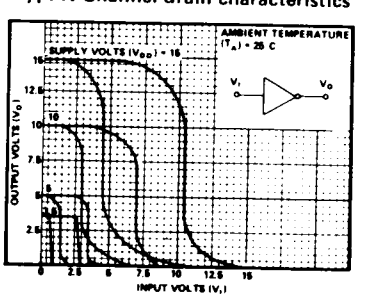
4007UB contains three N-Channel and three P-Channel enhancement-type MOS transistors on a single monolithic silicon chip. The transistor elements are accessible through the package terminals to provide means for constructing various logic, transmission gating, and linear circuits.



Typ. P-Channel drain characteristics

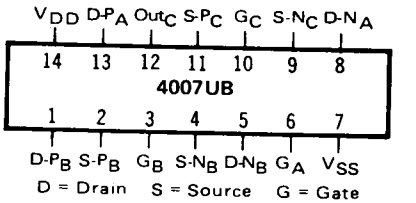


Typ. N-Channel drain characteristics



Min. and max. voltage transfer characteristics for inverter

CONNECTION DIAGRAM
(all packages)



D = Drain S = Source G = Gate

Add suffix for package:

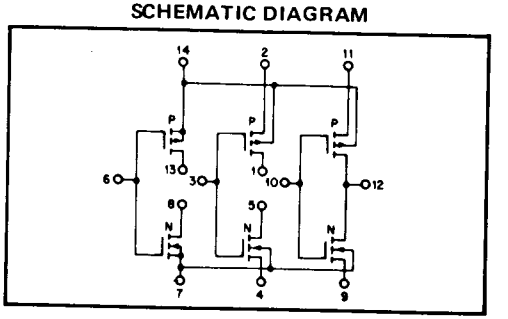
C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

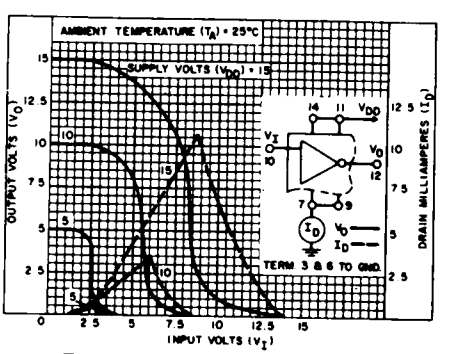
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM





Typ. current and voltage transfer characteristics for inverter

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

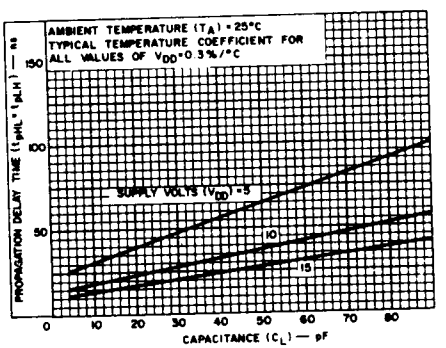
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

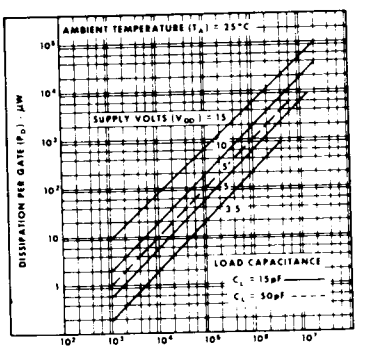
DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25 C) [1]

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5		55	110	ns
		10		30	60	
		15		25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5		100	200	ns
		10		50	100	
		15		40	80	

[1] Connected as inverter



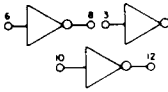
Typ. propagation delay time vs. C_L



Typ. dissipation characteristics

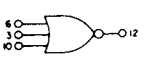
APPLICATIONS INFORMATION

Triple Inverters



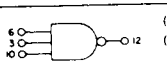
(14,2,11); (8,13); (1,5); (7,4,9)

3-Input NOR Gate



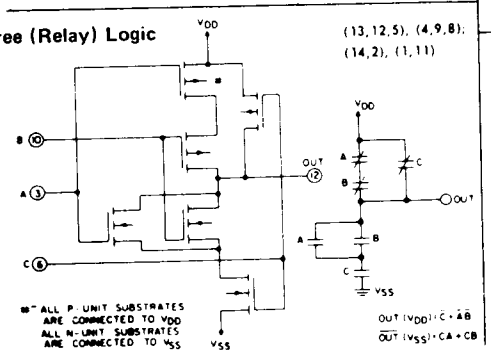
(13,2); (1,11); (12,5,8); (7,4,9)

3-Input NAND Gate



(1,12,13); (2,14,11); (4,8); (5,9)

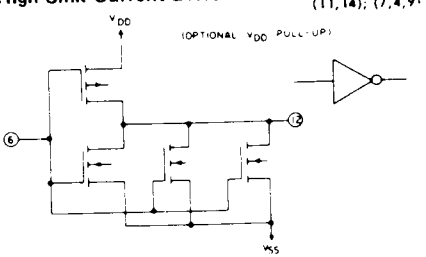
Tree (Relay) Logic



(13,12,5), (4,9,8); (14,2), (1,11)

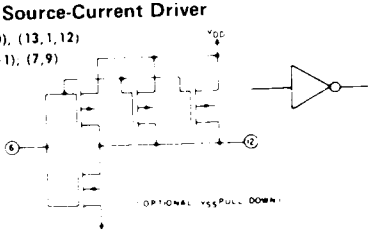
High Sink-Current Driver

(6,3,10); (8,5,12); (11,14); (7,4,9)



High Source-Current Driver

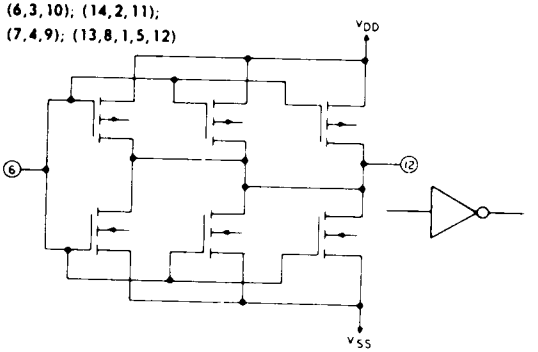
(6,3,10), (13,1,12) (14,2,11), (7,9)



APPLICATIONS INFORMATION (Continued)

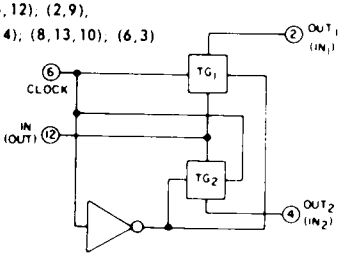
High Sink- and Source-Current Driver

(6,3,10); (14,2,11);
(7,4,9); (13,8,1,5,12)

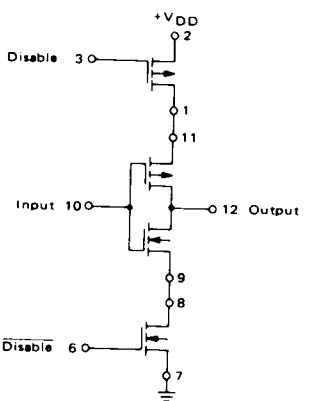


Dual Bi-Directional Transmission Gating

(1,5,12), (2,9),
(11,4); (8,13,10), (6,3)



3-State Buffer



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care