Product Brief

DSP56362

24-BIT AUDIO DIGITAL SIGNAL PROCESSOR

The DSP56362 is a high performance DSP optimized for cost-sensative consumer audio applications. A general purpose DSP56362 is available as well as a multimode, multichannel audio decoder for consumer applications such as Audio/Video (A/V) receivers, surround sound decoders, Digital Versatile Disk (DVD) players, digital TV, and other audio applications. The DSP56362 supports all of the popular multichannel audio decoding formats, including Dolby Digital Surround, Moving Picture Experts Group Standard 2 (MPEG2), and Digital Theater Systems (DTS), in a single device with sufficient MIPS resources for customer defined post-processing features such as bass management, 3D virtual surround, Lucasfilm THX5.1, soundfield processing, and advanced equalization.

The DSP56362, **Figure 1**,is member of the 56300 Motorola Symphony™ DSP Family. The DSP56362 utilizes the single-instruction-per-clock-cycle DSP56300 core, while retaining code compatibility with the DSP56000 core family. The DSP56362 contains audio-specific peripherals and an on-board software architecture as shown in **Figure 2** and is offered in a 100/120 MHz/MIPS version at a nominal 3.3 V.

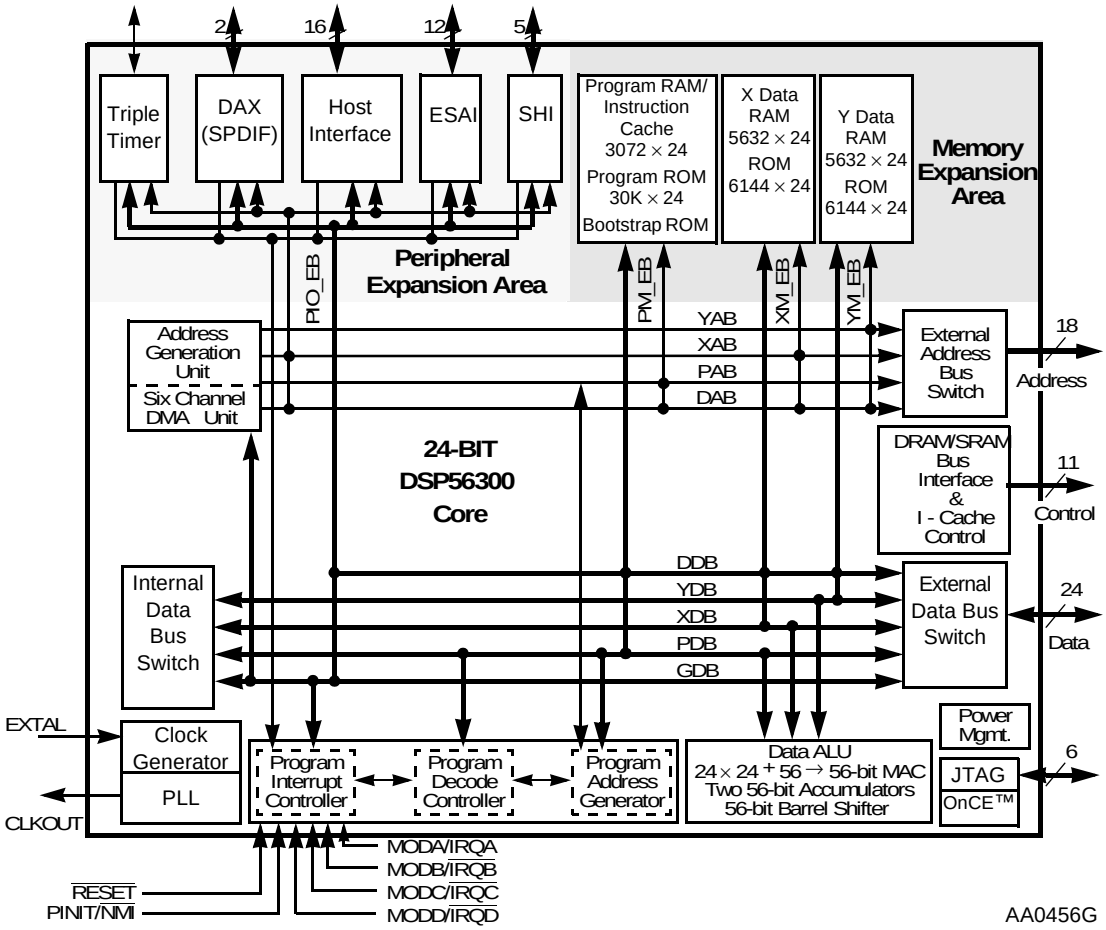

Figure 1 DSP56362 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

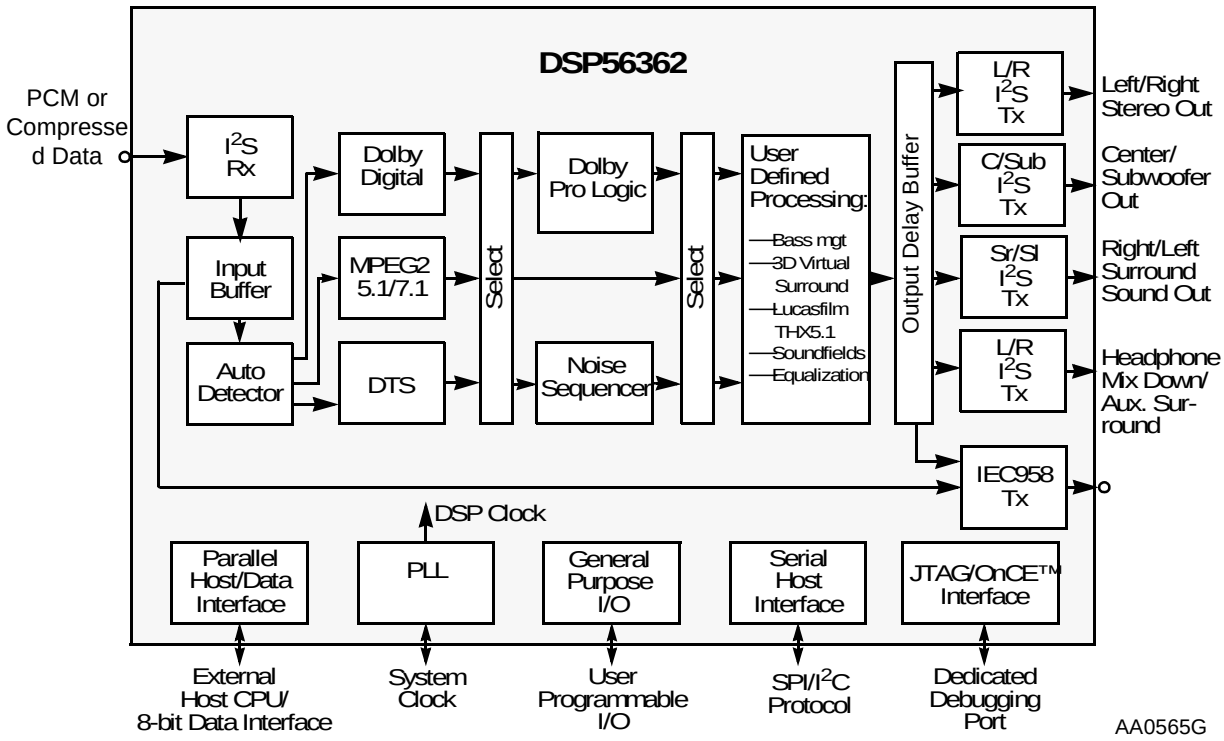

Figure 2 DSP56362 Surround Decoder Functionality

Features

- Multimode, multichannel decoder software functionality
  - Dolby Digital and Pro Logic
  - MPEG2 5.1
  - DTS
- Digital audio post-processing capabilities
  - Bass management
  - 3D Virtual surround sound
  - Lucasfilm THX5.1
  - Soundfield processing
  - Equalization
- Digital Signal Processing Core
  - 100/120 Million Instructions Per Second (MIPS) with an 100/120 MHz clock at a nominal 3.3 V
  - Object code compatible with the DSP56000 core with highly parallel instruction set
  - Data Arithmetic Logic Unit (Data ALU)
  - Program Control Unit (PCU)
  - Direct Memory Access (DMA)
  - Software programmable PLL-based frequency synthesizer for the core clock

  - Hardware debugging support: On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP), and Address Trace mode
- On-Chip Memories
  - Modified Harvard architecture allows simultaneous access to program and data memories
  - Program ROMs that may be factory programmed with data/program provided by the application developer
  - 3K x 24 Bit Program RAM
  - 30K x 24 Bit Program ROM
  - 5.5K x 24 Bit X-dataRAM
  - 6K x 24 Bit X-data ROM
  - 5.5K x 24 Bit Y-data RAM
  - 6K x 24 Bit Y-data ROM
  - 192 x 24-bit bootstrap ROM
- Off-Chip Memory Expansion
  - Memory expansion up to 4-256K x 24-bit word memory for P, X, and Y memory when using SRAM
  - Memory expansion up to 4-16M x 24-bit word memory for P, X, and Y memory when using DRAM
  - Twenty-four data pin external memory expansion port (for high speed external memory access allowing for a large number of external accesses per sample)
  - Chip Select Logic for glueless interface to SRAMs
  - On-chip DRAM Controller for glueless interface to DRAMs
- Peripheral and Support Circuits
  - Enhanced Serial Audio Interface (ESAI) includes:
    - 6 serial data lines, 4 selectable as receive or transmitt and 2 transmitt only.
    - Master or slave capability
    - I^2S, Sony, AC97, and other audio protocol implementations
    - Asynchronous and synchronous operation
  - Serial Host Interface (SHI) features:
    - SPI and I^2C protocols
    - Ten-word receive FIFO
    - Support for 8-, 16-, and 24-bit words.
  - Byte-wide parallel Host Interface (HDI08) with DMA support
  - DAX features one serial transmitter capable of supporting S/PDIF, IEC958, IEC1937, CP-340, and AES/EBU digital audio formats
  - Triple Timer module
  - On-chip peripheral registers memory mapped in data memory space
- Reduced Power Dissipation
  - Very low power (3.3 V) CMOS design
  - Wait and Stop low-power standby modes
  - Fully-static logic, operation frequency down to 0 Hz (DC)
  - Optimized power management circuitry

PACKAGE

  - 144-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package

DOCUMENTATION

Table 1 lists the documents that provide a complete description of the DSP56362 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or (for the latest information) through the Motorola DSP home page on the Internet. (See address below).

Table 1 DSP56362 Chip Documentation

Topic	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56800 family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56362 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56362UM/AD
DSP56362 Technical Data Sheet	Electrical and timing specifications and pin and package descriptions	DSP56362/D

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