

# SYNCBURST SRAM

MT58LC256K18E1, MT58LC128K32E1,  
MT58LC128K36E1

**3.3V Supply, 2.5V I/O, Flow-Through and  
Burst Counter**

## FEATURES

- Fast access times: 6.8ns, 7.5ns, 8.5ns and 9ns
- Fast OE# access time: 3.8ns, 4.2ns and 5ns
- +3.3V +0.3V/-0.165V power supply (V<sub>DD</sub>)
- Separate +2.5V +0.4V/-0.125V power supply (V<sub>DDQ</sub>)
- SNOOZE MODE for reduced power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

## OPTIONS

- Timing (Access/Cycle)

|             |      |
|-------------|------|
| 6.8ns/8ns   | -6.8 |
| 7.5ns/8.8ns | -7.5 |
| 8.5ns/10ns  | -8.5 |
| 9ns/10.5ns  | -9   |

- Configurations

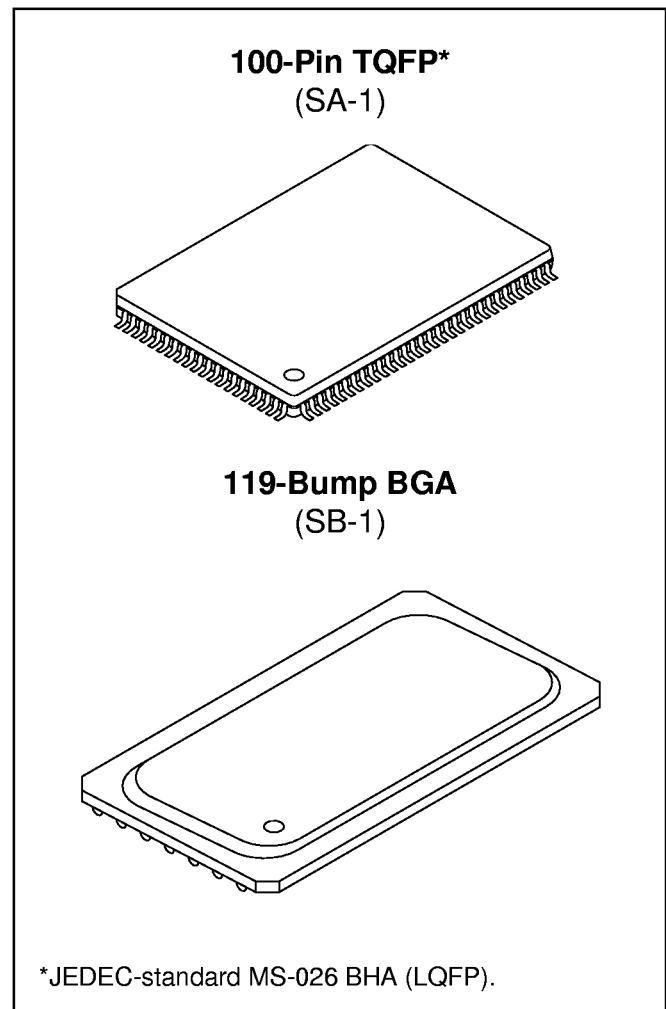
|           |                |
|-----------|----------------|
| 256K x 18 | MT58LC256K18E1 |
| 128K x 32 | MT58LC128K32E1 |
| 128K x 36 | MT58LC128K36E1 |

- Packages

|                           |    |
|---------------------------|----|
| 100-pin TQFP              | LG |
| 119-bump, 14mm x 22mm BGA | BG |

- Part Number Example: MT58LC256K18E1LG-9

## MARKING



\*JEDEC-standard MS-026 BHA (LQFP).

## GENERAL DESCRIPTION

The Micron SyncBurst SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

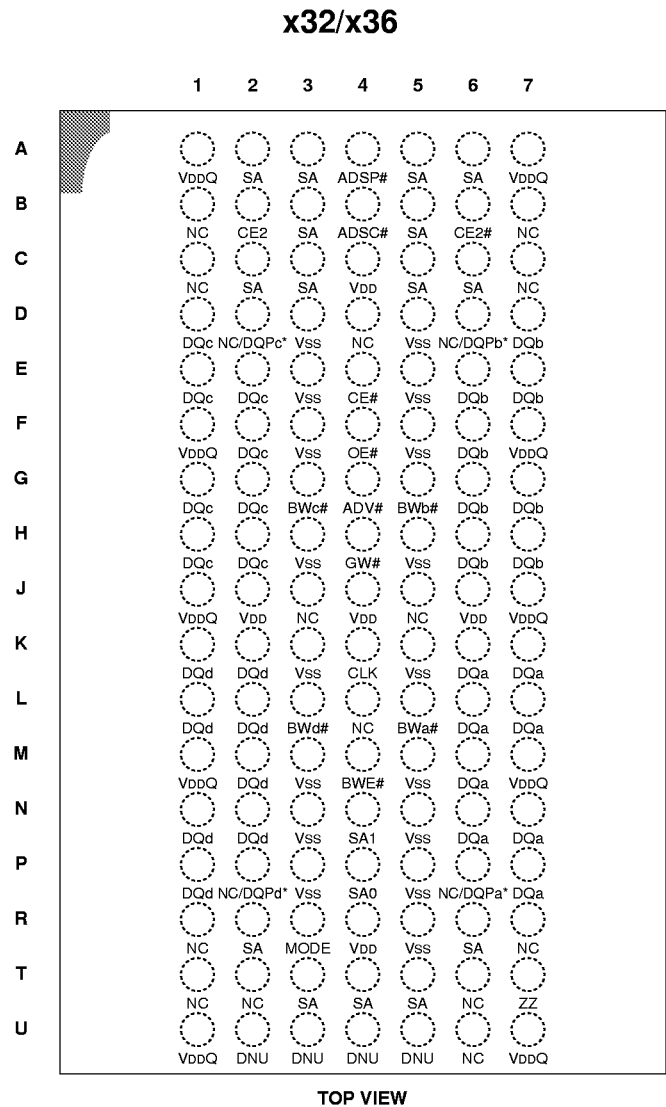
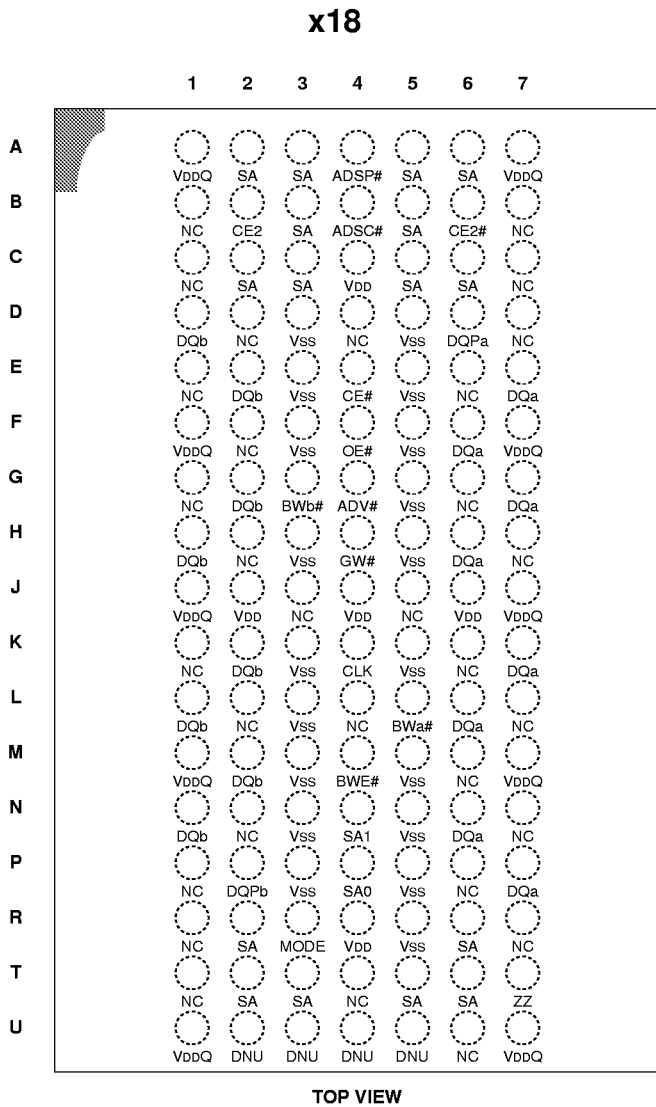
The MT58LC256K18E1 and MT58LC128K32/36E1 SRAMs integrate a 256K x 18, 128K x 32 or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock

input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2#, CE2), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between linear and interleaved burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36) as controlled by the write control inputs.



**PIN ASSIGNMENT (Top View)**  
**119-Bump BGA**



\* No Connect (NC) is used in the x32 version. Parity (DQPx) is used in the x36 version.

## 256K x 18, 128K x 32/36 2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

### GENERAL DESCRIPTION (continued)

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWA# controls DQa pins and DQPb; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWA# controls DQa pins and DQPb; BWb# controls DQb pins and DQPb; BWC# controls DQc pins and DQPc; BWD# controls DQd pins and DQPd. GW# LOW causes all bytes

to be written. Parity is only available on the x18 and x36 versions.

The MT58LC256K18E1 and MT58LC128K32/36E1 operate from a +3.3V power supply, and all inputs and outputs can communicate with 2.5V I/O. All inputs except the data I/Os are 3.3V-tolerant and can be used in mixed 3.3V and 2.5V systems. The device is ideally suited for systems that benefit from a wide synchronous data bus and 2.5V I/O. These devices are also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit-wide applications.

Please refer to the Micron Web site ([www.micron.com./mti/msp/html/sramprod.html](http://www.micron.com./mti/msp/html/sramprod.html)) for the latest data sheet revisions.

### TQFP PIN ASSIGNMENT TABLE

| PIN # | x18  | x32/x36  |
|-------|------|----------|
| 1     | NC   | NC/DQPa* |
| 2     | NC   | DQc      |
| 3     | NC   | DQc      |
| 4     | VDDQ |          |
| 5     | VSS  |          |
| 6     | NC   | DQc      |
| 7     | NC   | DQc      |
| 8     | DQb  | DQc      |
| 9     | DQb  | DQc      |
| 10    | VSS  |          |
| 11    | VDDQ |          |
| 12    | DQb  | DQc      |
| 13    | DQb  | DQc      |
| 14    | VSS  |          |
| 15    | VDD  |          |
| 16    | NC   |          |
| 17    | VSS  |          |
| 18    | DQb  | DQd      |
| 19    | DQb  | DQd      |
| 20    | VDDQ |          |
| 21    | VSS  |          |
| 22    | DQb  | DQd      |
| 23    | DQb  | DQd      |
| 24    | DQPb | DQd      |
| 25    | NC   | DQd      |

| PIN # | x18  | x32/x36  |
|-------|------|----------|
| 26    | VSS  |          |
| 27    | VDDQ |          |
| 28    | NC   | DQd      |
| 29    | NC   | DQd      |
| 30    | NC   | NC/DQPd* |
| 31    | MODE |          |
| 32    | SA   |          |
| 33    | SA   |          |
| 34    | SA   |          |
| 35    | SA   |          |
| 36    | SA1  |          |
| 37    | SA0  |          |
| 38    | DNU  |          |
| 39    | DNU  |          |
| 40    | VSS  |          |
| 41    | VDD  |          |
| 42    | DNU  |          |
| 43    | DNU  |          |
| 44    | SA   |          |
| 45    | SA   |          |
| 46    | SA   |          |
| 47    | SA   |          |
| 48    | SA   |          |
| 49    | SA   |          |
| 50    | SA   |          |

| PIN # | x18  | x32/x36  |
|-------|------|----------|
| 51    | NC   | NC/DQPa* |
| 52    | NC   | DQa      |
| 53    | NC   | DQa      |
| 54    | VDDQ |          |
| 55    | VSS  |          |
| 56    | NC   | DQa      |
| 57    | NC   | DQa      |
| 58    | DQa  |          |
| 59    | DQa  |          |
| 60    | VSS  |          |
| 61    | VDDQ |          |
| 62    | DQa  |          |
| 63    | DQa  |          |
| 64    | ZZ   |          |
| 65    | VDD  |          |
| 66    | NC   |          |
| 67    | VSS  |          |
| 68    | DQa  | DQb      |
| 69    | DQa  | DQb      |
| 70    | VDDQ |          |
| 71    | VSS  |          |
| 72    | DQa  | DQb      |
| 73    | DQa  | DQb      |
| 74    | DQPa | DQb      |
| 75    | NC   | DQb      |

| PIN # | x18   | x32/x36  |
|-------|-------|----------|
| 76    | VSS   |          |
| 77    | VDDQ  |          |
| 78    | NC    | DQb      |
| 79    | NC    | DQb      |
| 80    | SA    | NC/DQPb* |
| 81    | SA    |          |
| 82    | SA    |          |
| 83    | ADV#  |          |
| 84    | ADSP# |          |
| 85    | ADSC# |          |
| 86    | OE#   |          |
| 87    | BWE#  |          |
| 88    | GW#   |          |
| 89    | CLK   |          |
| 90    | VSS   |          |
| 91    | VDD   |          |
| 92    | CE2#  |          |
| 93    | BWA#  |          |
| 94    | BWB#  |          |
| 95    | NC    | BWc#     |
| 96    | NC    | BWd#     |
| 97    | CE2   |          |
| 98    | CE#   |          |
| 99    | SA    |          |
| 100   | SA    |          |

\* No Connect (NC) is used in the x32 version. Parity (DQPx) is used in the x36 version.

**x18 BGA BUMP LAYOUT  
 (Top View)**

|          | 1                | 2                | 3               | 4               | 5                 | 6                | 7                |
|----------|------------------|------------------|-----------------|-----------------|-------------------|------------------|------------------|
| <b>A</b> | V <sub>DDQ</sub> | SA               | SA              | ADSP#           | SA                | SA               | V <sub>DDQ</sub> |
| <b>B</b> | NC               | CE2              | SA              | ADSC#           | SA                | CE2#             | NC               |
| <b>C</b> | NC               | SA               | SA              | V <sub>DD</sub> | SA                | SA               | NC               |
| <b>D</b> | DQb              | NC               | V <sub>SS</sub> | NC              | V <sub>SS</sub>   | DQP <sub>a</sub> | NC               |
| <b>E</b> | NC               | DQb              | V <sub>SS</sub> | CE#             | V <sub>SS</sub>   | NC               | DQ <sub>a</sub>  |
| <b>F</b> | V <sub>DDQ</sub> | NC               | V <sub>SS</sub> | OE#             | V <sub>SS</sub>   | DQ <sub>a</sub>  | V <sub>DDQ</sub> |
| <b>G</b> | NC               | DQb              | BWb#            | ADV#            | V <sub>SS</sub>   | NC               | DQ <sub>a</sub>  |
| <b>H</b> | DQb              | NC               | V <sub>SS</sub> | GW#             | V <sub>SS</sub>   | DQ <sub>a</sub>  | NC               |
| <b>J</b> | V <sub>DDQ</sub> | V <sub>DD</sub>  | NC              | V <sub>DD</sub> | NC                | V <sub>DD</sub>  | V <sub>DDQ</sub> |
| <b>K</b> | NC               | DQb              | V <sub>SS</sub> | CLK             | V <sub>SS</sub>   | NC               | DQ <sub>a</sub>  |
| <b>L</b> | DQb              | NC               | V <sub>SS</sub> | NC              | BW <sub>a</sub> # | DQ <sub>a</sub>  | NC               |
| <b>M</b> | V <sub>DDQ</sub> | DQb              | V <sub>SS</sub> | BWE#            | V <sub>SS</sub>   | NC               | V <sub>DDQ</sub> |
| <b>N</b> | DQb              | NC               | V <sub>SS</sub> | SA1             | V <sub>SS</sub>   | DQ <sub>a</sub>  | NC               |
| <b>P</b> | NC               | DQP <sub>b</sub> | V <sub>SS</sub> | SA0             | V <sub>SS</sub>   | NC               | DQ <sub>a</sub>  |
| <b>R</b> | NC               | SA               | MODE            | V <sub>DD</sub> | V <sub>SS</sub>   | SA               | NC               |
| <b>T</b> | NC               | SA               | SA              | NC              | SA                | SA               | ZZ               |
| <b>U</b> | V <sub>DDQ</sub> | DNU              | DNU             | DNU             | DNU               | NC               | V <sub>DDQ</sub> |

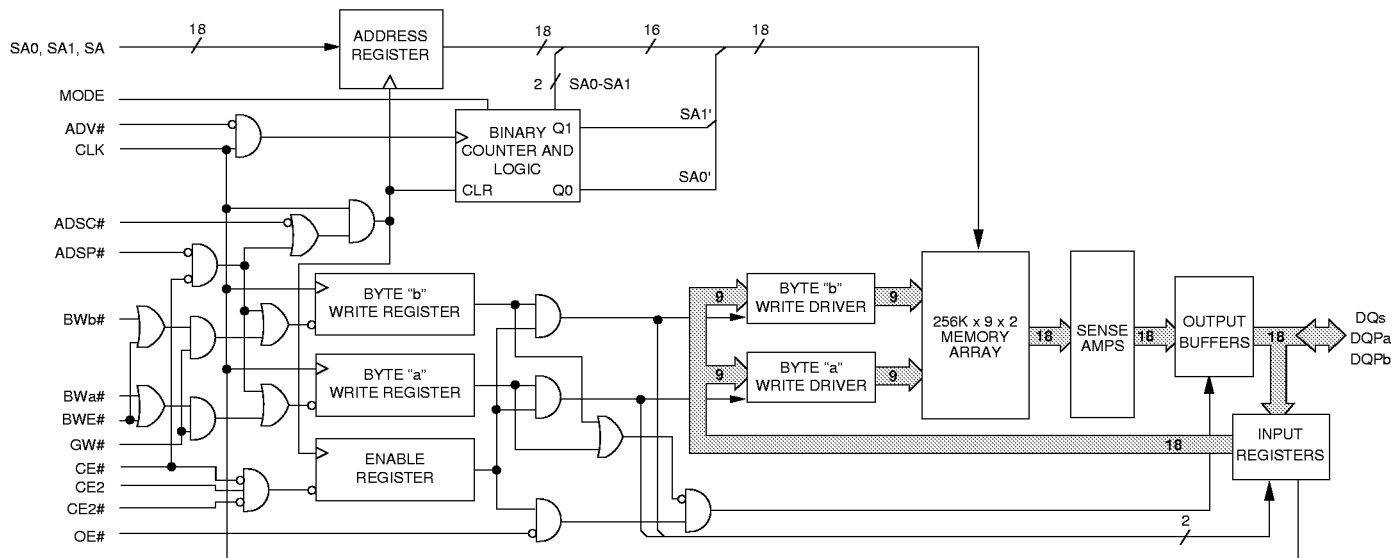
**x32/x36 BGA BUMP LAYOUT  
 (Top View)**

|          | 1                | 2                     | 3                 | 4               | 5                 | 6                     | 7                |
|----------|------------------|-----------------------|-------------------|-----------------|-------------------|-----------------------|------------------|
| <b>A</b> | V <sub>DDQ</sub> | SA                    | SA                | ADSP#           | SA                | SA                    | V <sub>DDQ</sub> |
| <b>B</b> | NC               | CE2                   | SA                | ADSC#           | SA                | CE2#                  | NC               |
| <b>C</b> | NC               | SA                    | SA                | V <sub>DD</sub> | SA                | SA                    | NC               |
| <b>D</b> | DQ <sub>c</sub>  | NC/DQP <sub>c</sub> * | V <sub>SS</sub>   | NC              | V <sub>SS</sub>   | NC/DQP <sub>b</sub> * | DQ <sub>b</sub>  |
| <b>E</b> | DQ <sub>c</sub>  | DQ <sub>c</sub>       | V <sub>SS</sub>   | CE#             | V <sub>SS</sub>   | DQ <sub>b</sub>       | DQ <sub>b</sub>  |
| <b>F</b> | V <sub>DDQ</sub> | DQ <sub>c</sub>       | V <sub>SS</sub>   | OE#             | V <sub>SS</sub>   | DQ <sub>b</sub>       | V <sub>DDQ</sub> |
| <b>G</b> | DQ <sub>c</sub>  | DQ <sub>c</sub>       | BW <sub>c</sub> # | ADV#            | BW <sub>b</sub> # | DQ <sub>b</sub>       | DQ <sub>b</sub>  |
| <b>H</b> | DQ <sub>c</sub>  | DQ <sub>c</sub>       | V <sub>SS</sub>   | GW#             | V <sub>SS</sub>   | DQ <sub>b</sub>       | DQ <sub>b</sub>  |
| <b>J</b> | V <sub>DDQ</sub> | V <sub>DD</sub>       | NC                | V <sub>DD</sub> | NC                | V <sub>DD</sub>       | V <sub>DDQ</sub> |
| <b>K</b> | DQ <sub>d</sub>  | DQ <sub>d</sub>       | V <sub>SS</sub>   | CLK             | V <sub>SS</sub>   | DQ <sub>a</sub>       | DQ <sub>a</sub>  |
| <b>L</b> | DQ <sub>d</sub>  | DQ <sub>d</sub>       | BW <sub>d</sub> # | NC              | BW <sub>a</sub> # | DQ <sub>a</sub>       | DQ <sub>a</sub>  |
| <b>M</b> | V <sub>DDQ</sub> | DQ <sub>d</sub>       | V <sub>SS</sub>   | BWE#            | V <sub>SS</sub>   | DQ <sub>a</sub>       | V <sub>DDQ</sub> |
| <b>N</b> | DQ <sub>d</sub>  | DQ <sub>d</sub>       | V <sub>SS</sub>   | SA1             | V <sub>SS</sub>   | DQ <sub>a</sub>       | DQ <sub>a</sub>  |
| <b>P</b> | DQ <sub>d</sub>  | NC/DQP <sub>d</sub> * | V <sub>SS</sub>   | SA0             | V <sub>SS</sub>   | NC/DQP <sub>a</sub> * | DQ <sub>a</sub>  |
| <b>R</b> | NC               | SA                    | MODE              | V <sub>DD</sub> | V <sub>SS</sub>   | SA                    | NC               |
| <b>T</b> | NC               | NC                    | SA                | SA              | SA                | NC                    | ZZ               |
| <b>U</b> | V <sub>DDQ</sub> | DNU                   | DNU               | DNU             | DNU               | NC                    | V <sub>DDQ</sub> |

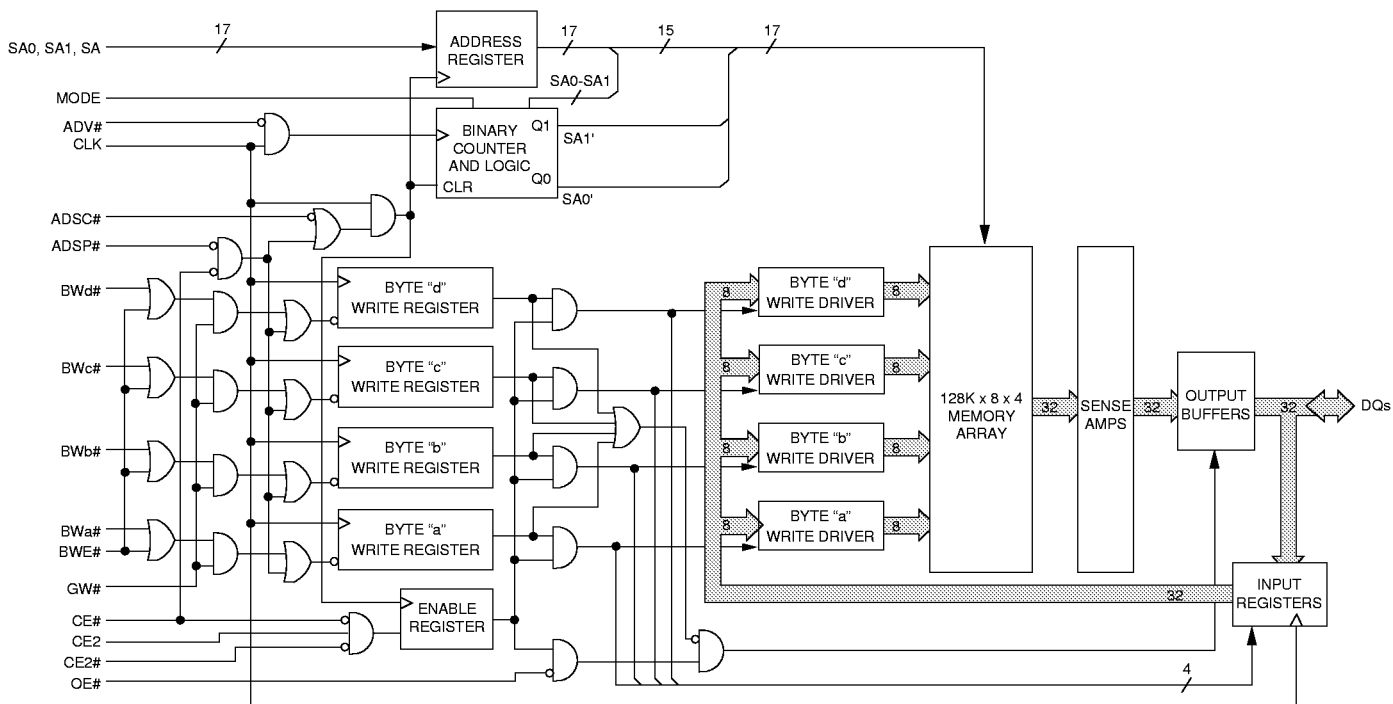
\* No Connect (NC) is used in the x32 version. Parity (DQP<sub>x</sub>) is used in the x36 version.

256K x 18, 128K x 32/36  
2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

FUNCTIONAL BLOCK DIAGRAM  
256K x 18

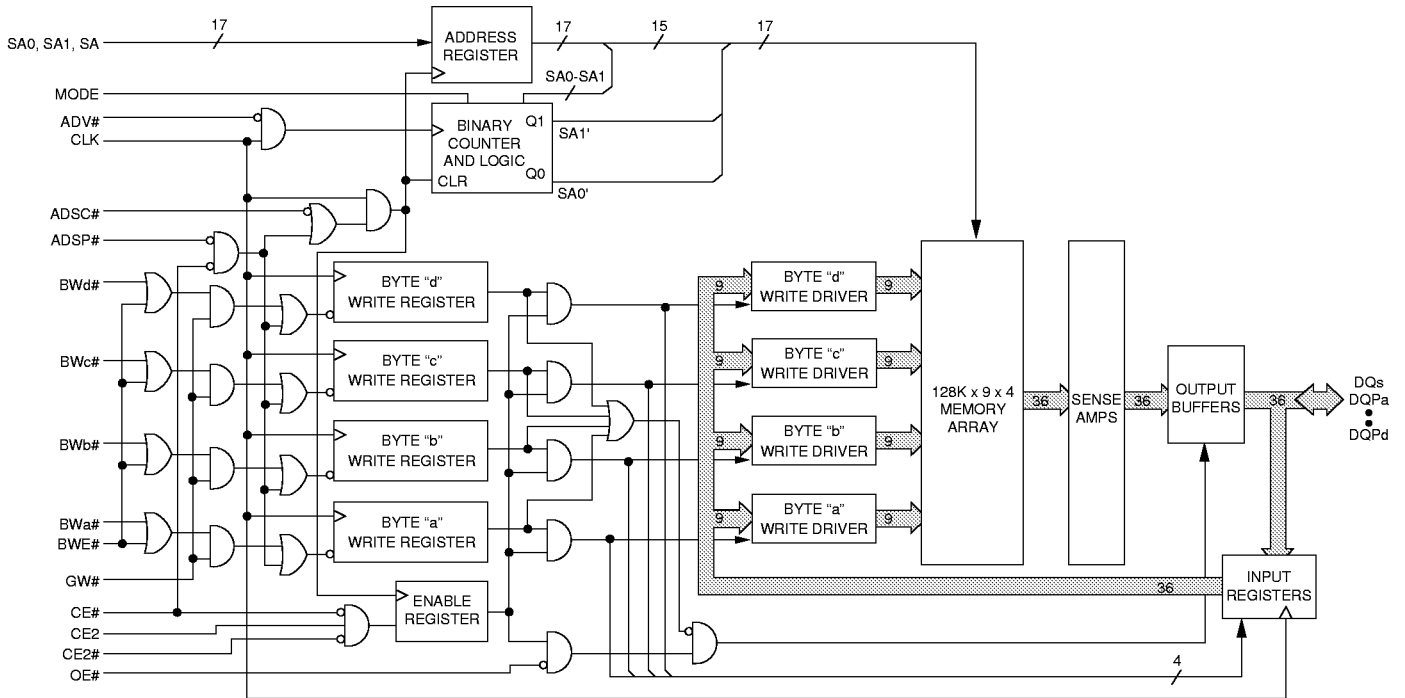


FUNCTIONAL BLOCK DIAGRAM  
128K x 32



**NOTE:** Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

**FUNCTIONAL BLOCK DIAGRAM**  
**128K x 36**



**NOTE:** Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

**ADVANCE**  
**256K x 18, 128K x 32/36**  
**2.5V I/O, FLOW-THROUGH SYNCBURST SRAM**

**PIN DESCRIPTIONS**

| TQFP (x18)                                    | TQFP (x32/x36)                                  | SYMBOL                       | TYPE  | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------------|-------------------------------------------------|------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 37<br>36<br>32-35, 44-50<br>80-82, 99,<br>100 | 37<br>36<br>32-35, 44-50,<br>81, 82, 99,<br>100 | SA0<br>SA1<br>SA             | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 93<br>94<br>–<br>–                            | 93<br>94<br>95<br>96                            | BWa#<br>BWb#<br>BWc#<br>BWd# | Input | Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQP <sub>a</sub> ; BWb# controls DQb pins and DQP <sub>b</sub> . For the x32 and x36 versions, BWa# controls DQa pins and DQP <sub>a</sub> ; BWb# controls DQb pins and DQP <sub>b</sub> ; BWc# controls DQc pins and DQP <sub>c</sub> ; BWd# controls DQd pins and DQP <sub>d</sub> . Parity is only available on the x18 and x36 versions. |
| 87                                            | 87                                              | BWE#                         | Input | Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 88                                            | 88                                              | GW#                          | Input | Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 89                                            | 89                                              | CLK                          | Input | Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 98                                            | 98                                              | CE#                          | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 92                                            | 92                                              | CE2#                         | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 97                                            | 97                                              | CE2                          | Input | Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 86                                            | 86                                              | OE#                          | Input | Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 83                                            | 83                                              | ADV#                         | Input | Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.                                                                                                                                                                                                                              |



**PIN DESCRIPTIONS (continued)**

| TQFP (x18)                                                                         | TQFP (x32/x36)                                                                                                           | SYMBOL                                   | TYPE             | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                              |
|------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|------------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 84                                                                                 | 84                                                                                                                       | ADSP#                                    | Input            | Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH. |
| 85                                                                                 | 85                                                                                                                       | ADSC#                                    | Input            | Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.                                                                               |
| 31                                                                                 | 31                                                                                                                       | MODE                                     | Input            | Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.                                                                                                                                                                           |
| 64                                                                                 | 64                                                                                                                       | ZZ                                       | Input            | Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.                                                                                                                                                              |
| (a) 58, 59,<br>62, 63, 68, 69,<br>72, 73<br>(b) 8, 9, 12,<br>13, 18, 19,<br>22, 23 | (a) 52, 53,<br>56-59, 62, 63<br>(b) 68, 69,<br>72-75, 78, 79<br>(c) 2, 3, 6-9,<br>12, 13<br>(d) 18, 19,<br>22-25, 28, 29 | DQa<br><br>DQb<br><br>DQc<br><br>DQd     | Input/<br>Output | SRAM Data I/Os: For the x18 version, Byte "a" is DQa pins; Byte "b" is DQb pins. For the x32 and x36 versions, Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.                                                                                          |
| 74<br>24<br>–<br>–                                                                 | 51<br>80<br>1<br>30                                                                                                      | NC/DQPa<br>NC/DQPb<br>NC/DQPC<br>NC/DQPD | NC/<br>I/O       | No Connect/Parity Data I/Os: On the x32 version, these pins are No Connect (NC). On the x18 version, Byte "a" Parity is DQPa; Byte "b" Parity is DQPb. On the x36 version, Byte "a" Parity is DQPa; Byte "b" Parity is DQPb; Byte "c" Parity is DQPC; Byte "d" Parity is DQPD.                                                                                           |
| 15, 41, 65, 91                                                                     | 15, 41, 65, 91                                                                                                           | V <sub>DD</sub>                          | Supply           | Power Supply: See DC Electrical Characteristics and Operating Conditions for range.                                                                                                                                                                                                                                                                                      |
| 4, 11, 20, 27,<br>54, 61, 70, 77                                                   | 4, 11, 20, 27,<br>54, 61, 70, 77                                                                                         | V <sub>DDQ</sub>                         | Supply           | Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.                                                                                                                                                                                                                                                                     |
| 5, 10, 14,<br>17, 21, 26, 40,<br>55, 60, 67,<br>71, 76, 90                         | 5, 10, 14,<br>17, 21, 26, 40,<br>55, 60, 67,<br>71, 76, 90                                                               | V <sub>SS</sub>                          | Supply           | Ground: GND.                                                                                                                                                                                                                                                                                                                                                             |
| 38, 39, 42, 43                                                                     | 38, 39, 42, 43                                                                                                           | DNU                                      | –                | Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.                                                                                                                                                                                                                                                                 |
| 1-3, 6, 7, 16,<br>25, 28-30,<br>51-53, 56, 57,<br>66, 75, 78, 79,<br>95, 96        | 16, 66                                                                                                                   | NC                                       | –                | No Connect: These signals are not internally connected. However, to improve package heat dissipation, these signals may be connected to ground.                                                                                                                                                                                                                          |

## 256K x 18, 128K x 32/36 2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

### PIN DESCRIPTIONS

| BGA (x18)                                                                              | BGA (x32/x36)                                                                      | SYMBOL                       | TYPE  | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4P<br>4N<br>2A, 3A, 5A,<br>6A, 3B, 5B,<br>2C, 3C, 5C,<br>6C, 2R, 6R,<br>2T, 3T, 5T, 6T | 4P<br>4N<br>2A, 2C, 2R,<br>3A, 3B, 3C,<br>3T, 4T, 5A,<br>5B, 5C, 5T,<br>6A, 6C, 6R | SA0<br>SA1<br>SA             | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5L<br>3G<br>–<br>–                                                                     | 5L<br>5G<br>3G<br>3L                                                               | BWa#<br>BWb#<br>BWc#<br>BWd# | Input | Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQP <sub>a</sub> ; BWb# controls DQb pins and DQP <sub>b</sub> . For the x32 and x36 versions, BWa# controls DQa pins and DQP <sub>a</sub> ; BWb# controls DQb pins and DQP <sub>b</sub> ; BWc# controls DQc pins and DQP <sub>c</sub> ; BWd# controls DQd pins and DQP <sub>d</sub> . Parity is only available on the x18 and x36 versions. |
| 4M                                                                                     | 4M                                                                                 | BWE#                         | Input | Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 4H                                                                                     | 4H                                                                                 | GW#                          | Input | Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4K                                                                                     | 4K                                                                                 | CLK                          | Input | Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 4E                                                                                     | 4E                                                                                 | CE#                          | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 6B                                                                                     | 6B                                                                                 | CE2#                         | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7T                                                                                     | 7T                                                                                 | ZZ                           | Input | Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2B                                                                                     | 2B                                                                                 | CE2                          | Input | Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 4F                                                                                     | 4F                                                                                 | OE#                          | Input | Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 4G                                                                                     | 4G                                                                                 | ADV#                         | Input | Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.                                                                                                                                                                                                                              |

**PIN DESCRIPTIONS (continued)**

| BGA (x18)                                                                                    | BGA (x32/x36)                                                                                                                                                                | SYMBOL                                   | TYPE             | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                              |
|----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4A                                                                                           | 4A                                                                                                                                                                           | ADSP#                                    | Input            | Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH. |
| 4B                                                                                           | 4B                                                                                                                                                                           | ADSC#                                    | Input            | Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.                                                                               |
| 3R                                                                                           | 3R                                                                                                                                                                           | MODE                                     | Input            | Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.                                                                                                                                                                           |
| (a) 6F, 6H, 6L,<br>6N, 7E, 7G,<br>7K, 7P<br>(b) 1D, 1H,<br>1L, 1N, 2E,<br>2G, 2K, 2M         | (a) 6K, 6L,<br>6M, 6N, 7K,<br>7L, 7N, 7P<br>(b) 6E, 6F,<br>6G, 6H, 7D,<br>7E, 7G, 7H<br>(c) 1D, 1E,<br>1G, 1H, 2E,<br>2F, 2G, 2H<br>(d) 1K, 1L,<br>1N, 1P, 2K,<br>2L, 2M, 2N | DQa<br><br>DQb<br><br>DQc<br><br>DQd     | Input/<br>Output | SRAM Data I/Os: For the x18 version, Byte "a" is DQa pins; Byte "b" is DQb pins. For the x32 and x36 versions, Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.                                                                                          |
| 6D<br>2P<br>–<br>–                                                                           | 6P<br>6D<br>2D<br>2P                                                                                                                                                         | NC/DQPa<br>NC/DQPb<br>NC/DQPc<br>NC/DQPd | NC/<br>I/O       | No Connect/Parity Data I/Os: On the x32 version, these pins are No Connect (NC). On the x18 version, Byte "a" Parity is DQPa; Byte "b" Parity is DQPb. On the x36 version, Byte "a" Parity is DQPa; Byte "b" Parity is DQPb; Byte "c" Parity is DQPc; Byte "d" Parity is DQPd.                                                                                           |
| 2J, 4C, 4J,<br>4R, 6J                                                                        | 2J, 4C, 4J,<br>4R, 6J                                                                                                                                                        | V <sub>DD</sub>                          | Supply           | Power Supply: See DC Electrical Characteristics and Operating Conditions for range.                                                                                                                                                                                                                                                                                      |
| 1A, 1F, 1J,<br>1M, 1U, 7A,<br>7F, 7J, 7M,<br>7U                                              | 1A, 1F, 1J,<br>1M, 1U, 7A,<br>7F, 7J, 7M,<br>7U                                                                                                                              | V <sub>DDQ</sub>                         | Supply           | Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.                                                                                                                                                                                                                                                                     |
| 3D, 3E, 3F,<br>3H, 3K,<br>3L, 3M, 3N,<br>3P, 5D, 5E,<br>5F, 5G, 5H,<br>5K, 5M,<br>5N, 5P, 5R | 3D, 3E, 3F,<br>3H, 3K, 3M,<br>3N, 3P, 5D,<br>5E, 5F, 5H,<br>5K, 5M, 5N,<br>5P, 5R                                                                                            | V <sub>SS</sub>                          | Supply           | Ground: GND.                                                                                                                                                                                                                                                                                                                                                             |
| 2U, 3U, 4U,<br>5U                                                                            | 2U, 3U, 4U,<br>5U                                                                                                                                                            | DNU                                      | –                | Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.                                                                                                                                                                                                                                                                 |

## 256K x 18, 128K x 32/36 2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

### PIN DESCRIPTIONS (continued)

| BGA (x18)                                                                                                                                                | BGA (x32/x36)                                                      | SYMBOL | TYPE | DESCRIPTION                                                                                                                                     |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|--------|------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 1B, 1C, 1E,<br>1G, 1K, 1P,<br>1R, 1T, 2D,<br>2F, 2H, 2L,<br>2N, 3J, 4D,<br>4L, 4T, 5J,<br>6E, 6G, 6K,<br>6M, 6P, 6U,<br>7B, 7C, 7D,<br>7H, 7L, 7N,<br>7R | 1B, 1C, 1R,<br>1T, 2T,<br>3J, 4D, 4L,<br>5J, 6T, 6U,<br>7B, 7C, 7R | NC     | –    | No Connect: These signals are not internally connected. However, to improve package heat dissipation, these signals may be connected to ground. |

**INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)**

| First Address (External) | Second Address (Internal) | Third Address (Internal) | Fourth Address (Internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X...X00                  | X...X01                   | X...X10                  | X...X11                   |
| X...X01                  | X...X00                   | X...X11                  | X...X10                   |
| X...X10                  | X...X11                   | X...X00                  | X...X01                   |
| X...X11                  | X...X10                   | X...X01                  | X...X00                   |

**LINEAR BURST ADDRESS TABLE (MODE = LOW)**

| First Address (External) | Second Address (Internal) | Third Address (Internal) | Fourth Address (Internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X...X00                  | X...X01                   | X...X10                  | X...X11                   |
| X...X01                  | X...X10                   | X...X11                  | X...X00                   |
| X...X10                  | X...X11                   | X...X00                  | X...X01                   |
| X...X11                  | X...X00                   | X...X01                  | X...X10                   |

**PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x18)**

| Function        | GW# | BWE# | BWa# | BWb# |
|-----------------|-----|------|------|------|
| READ            | H   | H    | X    | X    |
| READ            | H   | L    | H    | H    |
| WRITE Byte "a"  | H   | L    | L    | H    |
| WRITE Byte "b"  | H   | L    | H    | L    |
| WRITE All Bytes | H   | L    | L    | L    |
| WRITE All Bytes | L   | X    | X    | X    |

**PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x32/x36)**

| Function        | GW# | BWE# | BWa# | BWb# | BWc# | BWd# |
|-----------------|-----|------|------|------|------|------|
| READ            | H   | H    | X    | X    | X    | X    |
| READ            | H   | L    | H    | H    | H    | H    |
| WRITE Byte "a"  | H   | L    | L    | H    | H    | H    |
| WRITE All Bytes | H   | L    | L    | L    | L    | L    |
| WRITE All Bytes | L   | X    | X    | X    | X    | X    |

**NOTE:** Using BWE# and BWa# through BWd#, any one or more bytes may be written.

**ADVANCE**  
**256K x 18, 128K x 32/36**  
**2.5V I/O, FLOW-THROUGH SYNCBURST SRAM**

**TRUTH TABLE**

| OPERATION                    | ADDRESS USED | CE# | CE2# | CE2 | ZZ | ADSP# | ADSC# | ADV# | WRITE# | OE# | CLK | DQ     |
|------------------------------|--------------|-----|------|-----|----|-------|-------|------|--------|-----|-----|--------|
| Deselected Cycle, Power-Down | None         | H   | X    | X   | L  | X     | L     | X    | X      | X   | L-H | High-Z |
| Deselected Cycle, Power-Down | None         | L   | X    | L   | L  | L     | X     | X    | X      | X   | L-H | High-Z |
| Deselected Cycle, Power-Down | None         | L   | H    | X   | L  | L     | X     | X    | X      | X   | L-H | High-Z |
| Deselected Cycle, Power-Down | None         | L   | X    | L   | L  | H     | L     | X    | X      | X   | L-H | High-Z |
| Deselected Cycle, Power-Down | None         | L   | H    | X   | L  | H     | L     | X    | X      | X   | L-H | High-Z |
| SNOOZE MODE, Power-Down      | None         | X   | X    | X   | H  | X     | X     | X    | X      | X   | X   | High-Z |
| READ Cycle, Begin Burst      | External     | L   | L    | H   | L  | L     | X     | X    | X      | L   | L-H | Q      |
| READ Cycle, Begin Burst      | External     | L   | L    | H   | L  | L     | X     | X    | X      | H   | L-H | High-Z |
| WRITE Cycle, Begin Burst     | External     | L   | L    | H   | L  | H     | L     | X    | L      | X   | L-H | D      |
| READ Cycle, Begin Burst      | External     | L   | L    | H   | L  | H     | L     | X    | H      | L   | L-H | Q      |
| READ Cycle, Begin Burst      | External     | L   | L    | H   | L  | H     | L     | X    | H      | H   | L-H | High-Z |
| READ Cycle, Continue Burst   | Next         | X   | X    | X   | L  | H     | H     | L    | H      | L   | L-H | Q      |
| READ Cycle, Continue Burst   | Next         | X   | X    | X   | L  | H     | H     | L    | H      | H   | L-H | High-Z |
| READ Cycle, Continue Burst   | Next         | H   | X    | X   | L  | X     | H     | L    | H      | L   | L-H | Q      |
| READ Cycle, Continue Burst   | Next         | H   | X    | X   | L  | X     | H     | L    | H      | H   | L-H | High-Z |
| WRITE Cycle, Continue Burst  | Next         | X   | X    | X   | L  | H     | H     | L    | L      | X   | L-H | D      |
| WRITE Cycle, Continue Burst  | Next         | H   | X    | X   | L  | X     | H     | L    | L      | X   | L-H | D      |
| READ Cycle, Suspend Burst    | Current      | X   | X    | X   | L  | H     | H     | H    | H      | L   | L-H | Q      |
| READ Cycle, Suspend Burst    | Current      | X   | X    | X   | L  | H     | H     | H    | H      | H   | L-H | High-Z |
| READ Cycle, Suspend Burst    | Current      | H   | X    | X   | L  | X     | H     | H    | H      | L   | L-H | Q      |
| READ Cycle, Suspend Burst    | Current      | H   | X    | X   | L  | X     | H     | H    | H      | H   | L-H | High-Z |
| WRITE Cycle, Suspend Burst   | Current      | X   | X    | X   | L  | H     | H     | H    | L      | X   | L-H | D      |
| WRITE Cycle, Suspend Burst   | Current      | H   | X    | X   | L  | X     | H     | H    | L      | X   | L-H | D      |

- NOTE:**
1. X means "Don't Care." # means active LOW. H means logic HIGH. L means logic LOW.
  2. For WRITE#, L means any one or more byte write enable signals (BWA#, BWB#, BWC# or BWD#) and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
  3. BWA# enables WRITES to DQa pins, DQPa. BWB# enables WRITES to DQb pins, DQPb. BWC# enables WRITES to DQc pins, DQPc. BWD# enables WRITES to DQd pins, DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
  4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
  5. Wait states are inserted by suspending burst.
  6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
  7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
  8. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.



## 256K x 18, 128K x 32/36 2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

### ABSOLUTE MAXIMUM RATINGS\*

|                                                                     |                                  |
|---------------------------------------------------------------------|----------------------------------|
| Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub> ..... | -0.5V to +4.6V                   |
| Voltage on V <sub>DDQ</sub> Supply Relative to V <sub>SS</sub> .... | -0.5V to +4.6V                   |
| V <sub>IN</sub> (DQx) .....                                         | -0.5V to V <sub>DDQ</sub> + 0.5V |
| V <sub>IN</sub> (inputs) .....                                      | -0.5V to V <sub>DD</sub> + 0.5V  |
| Storage Temperature (plastic) .....                                 | -55°C to +150°C                  |
| Storage Temperature (BGA) .....                                     | -55°C to +125°C                  |
| Junction Temperature** .....                                        | +150°C                           |
| Short Circuit Output Current .....                                  | 100mA                            |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\*Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

### DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub> = +3.3V +0.3V/-0.165V; V<sub>DDQ</sub> = +2.5V +0.4V/-0.125V unless otherwise noted)

| DESCRIPTION                   | CONDITIONS                                                           | SYMBOL           | MIN   | MAX                    | UNITS | NOTES |
|-------------------------------|----------------------------------------------------------------------|------------------|-------|------------------------|-------|-------|
| Input High (Logic 1) Voltage  | Data bus (DQx)                                                       | V <sub>IHQ</sub> | 1.7   | V <sub>DDQ</sub> + 0.3 | V     | 1, 2  |
|                               | Inputs                                                               | V <sub>IH</sub>  | 1.7   | V <sub>DD</sub> + 0.3  | V     | 1, 2  |
| Input Low (Logic 0) Voltage   |                                                                      | V <sub>IL</sub>  | -0.3  | 0.7                    | V     | 1, 2  |
| Input Leakage Current         | 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>                               | I <sub>LI</sub>  | -1    | 1                      | μA    | 3     |
| Output Leakage Current        | Output(s) disabled,<br>0V ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub> (DQx) | I <sub>LO</sub>  | -1    | 1                      | μA    |       |
| Output High Voltage           | I <sub>OH</sub> = -2.0mA                                             | V <sub>OH</sub>  | 1.7   |                        | V     | 1     |
|                               | I <sub>OH</sub> = -1.0mA                                             | V <sub>OH</sub>  | 2.0   |                        | V     | 1     |
| Output Low Voltage            | I <sub>OL</sub> = 2.0mA                                              | V <sub>OL</sub>  |       | 0.7                    | V     | 1     |
|                               | I <sub>OL</sub> = 1.0mA                                              | V <sub>OL</sub>  |       | 0.4                    | V     | 1     |
| Supply Voltage                |                                                                      | V <sub>DD</sub>  | 3.135 | 3.6                    | V     | 1     |
| Isolated Output Buffer Supply |                                                                      | V <sub>DDQ</sub> | 2.375 | 2.9                    | V     | 1     |

### TQFP THERMAL RESISTANCE

| DESCRIPTION                              | CONDITIONS                                                                 | SYMBOL          | TQFP TYP | UNITS | NOTES |
|------------------------------------------|----------------------------------------------------------------------------|-----------------|----------|-------|-------|
| Thermal Resistance (Junction to Ambient) | Still air, soldered on 4.25 x 1.125 inch,<br>4-layer printed circuit board | θ <sub>JA</sub> | 28       | °C/W  | 4     |
| Thermal Resistance (Junction to Case)    |                                                                            | θ <sub>JC</sub> | 4        | °C/W  | 4     |

### BGA THERMAL RESISTANCE

| DESCRIPTION                           | CONDITIONS                                                        | SYMBOL          | TYP | UNITS | NOTES |
|---------------------------------------|-------------------------------------------------------------------|-----------------|-----|-------|-------|
| Junction to Ambient (Airflow of 1m/s) | Soldered on a 4.25 x 1.125-inch,<br>4-layer printed circuit board | θ <sub>JA</sub> | 25  | °C/W  | 4     |
| Junction to Case (Top)                |                                                                   | θ <sub>JC</sub> | 10  | °C/W  | 4     |
| Junction to Bumps (Bottom)            |                                                                   | θ <sub>JB</sub> | 12  | °C/W  | 4     |

- NOTE:**
- All voltages referenced to V<sub>SS</sub> (GND).
  - Overshoot: V<sub>IH</sub> ≤ +4.6V for t ≤ 1<sup>1</sup>KC/2 for I ≤ 20mA  
Undershoot: V<sub>IL</sub> ≥ -0.7V for t ≤ 1<sup>1</sup>KC/2 for I ≤ 20mA  
Power-up: V<sub>IH</sub> ≤ +3.6V and V<sub>DD</sub> ≤ 3.135V for t ≤ 200ms
  - MODE pin has an internal pull-up, and input leakage = ±100μA.
  - This parameter is sampled.

## 256K x 18, 128K x 32/36 2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

### DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub> = +3.3V +0.3V/-0.165V; V<sub>DDQ</sub> = +2.5V +0.4V/-0.125V unless otherwise noted)

| DESCRIPTION                     | CONDITIONS                                                                                                                                                                                                                                                                               | SYM              | TYP | MAX  |      |      |     | UNITS | NOTES   |
|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|------|------|------|-----|-------|---------|
|                                 |                                                                                                                                                                                                                                                                                          |                  |     | -6.8 | -7.5 | -8.5 | -9  |       |         |
| Power Supply Current: Operating | Device selected; All inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ;<br>Cycle time ≥ 1KC MIN;<br>V <sub>DDQ</sub> = MAX; V <sub>DD</sub> = MAX; Outputs open                                                                                                                             | I <sub>DD</sub>  | TBD | 300  | 280  | 250  | 250 | mA    | 1, 2, 3 |
| Power Supply Current: Idle      | Device selected; V <sub>DD</sub> = MAX; V <sub>DDQ</sub> = MAX;<br>ADSC#, ADSP#, ADV#, GW#, BWx# ≥ V <sub>IH</sub> ; Inputs ≤ V <sub>SS</sub> + 0.2 or ≥ V <sub>DD</sub> - 0.2;<br>Data (DQx) ≤ V <sub>SS</sub> + 0.2 or ≥ V <sub>DDQ</sub> - 0.2;<br>Cycle time ≥ 1KC MIN; Outputs open | I <sub>DD1</sub> | TBD | 90   | 85   | 75   | 60  | mA    | 1, 2, 3 |
| CMOS Standby                    | Device deselected; V <sub>DD</sub> = MAX;<br>V <sub>DDQ</sub> = MAX; Inputs ≤ V <sub>SS</sub> + 0.2 or ≥ V <sub>DD</sub> - 0.2; Data (DQx) ≤ V <sub>SS</sub> + 0.2 or ≥ V <sub>DDQ</sub> - 0.2; All inputs static;<br>CLK frequency = 0                                                  | I <sub>SB2</sub> | TBD | 10   | 10   | 10   | 10  | mA    | 2, 3    |
| TTL Standby                     | Device deselected; V <sub>DD</sub> = MAX;<br>V <sub>DDQ</sub> = MAX; All inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ;<br>All inputs static; CLK frequency = 0                                                                                                                         | I <sub>SB3</sub> | TBD | 25   | 25   | 25   | 25  | mA    | 2, 3    |
| Clock Running                   | Device deselected; V <sub>DD</sub> = MAX;<br>V <sub>DDQ</sub> = MAX; Inputs ≤ V <sub>SS</sub> + 0.2 or ≥ V <sub>DD</sub> - 0.2; Data (DQx) ≤ V <sub>SS</sub> + 0.2 or ≥ V <sub>DDQ</sub> - 0.2; Cycle time ≥ 1KC MIN                                                                     | I <sub>SB4</sub> | TBD | 90   | 85   | 75   | 60  | mA    | 2, 3    |

### TQFP CAPACITANCE

| DESCRIPTION                   | CONDITIONS                                                 | SYMBOL          | TYP | MAX | UNITS | NOTES |
|-------------------------------|------------------------------------------------------------|-----------------|-----|-----|-------|-------|
| Control Input Capacitance     | T <sub>A</sub> = 25°C; f = 1 MHz<br>V <sub>DD</sub> = 3.3V | C <sub>I</sub>  | 3   | 4   | pF    | 4     |
| Input/Output Capacitance (DQ) |                                                            | C <sub>O</sub>  | 4   | 5   | pF    | 4     |
| Address Capacitance           |                                                            | C <sub>A</sub>  | 3   | 3.5 | pF    | 4     |
| Clock Capacitance             |                                                            | C <sub>CK</sub> | 2.5 | 3   | pF    | 4     |

### BGA CAPACITANCE

| DESCRIPTION                       | CONDITIONS                       | SYMBOL          | TYP | MAX | UNITS | NOTES |
|-----------------------------------|----------------------------------|-----------------|-----|-----|-------|-------|
| Address/Control Input Capacitance | T <sub>A</sub> = 25°C; f = 1 MHz | C <sub>I</sub>  | 4   | 5   | pF    | 4     |
| Input/Output Capacitance (DQ)     |                                  | C <sub>O</sub>  | 6   | 7   | pF    | 4     |
| Clock Capacitance                 |                                  | C <sub>CK</sub> | 5   | 6   | pF    | 4     |

- NOTE:**
- I<sub>DD</sub> is specified with no output current and increases with faster cycle times. I<sub>DDQ</sub> increases with faster cycle times and greater output loading.
  - “Device deselected” means device is in power-down mode as defined in the truth table. “Device selected” means device is active (not in power-down mode).
  - Typical values are measured at 3.3V, V<sub>DDQ</sub> = 2.5V, 25°C and 9ns cycle time.
  - This parameter is sampled.



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 1) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{DD} = +3.3\text{V} +0.3\text{V}/-0.165\text{V}$ ;  $V_{DDQ} = +2.5\text{V} +0.4\text{V}/-0.125\text{V}$  unless otherwise noted)

| DESCRIPTION                                            | SYMBOL     | -6.8 |     | -7.5 |     | -8.5 |     | -9   |     | UNITS | NOTES      |
|--------------------------------------------------------|------------|------|-----|------|-----|------|-----|------|-----|-------|------------|
|                                                        |            | MIN  | MAX | MIN  | MAX | MIN  | MAX | MIN  | MAX |       |            |
| <b>Clock</b>                                           |            |      |     |      |     |      |     |      |     |       |            |
| Clock cycle time                                       | $t_{KC}$   | 8.0  |     | 8.8  |     | 10.0 |     | 10.5 |     | ns    |            |
| Clock frequency                                        | $f_{KF}$   |      | 125 |      | 113 |      | 100 |      | 94  | MHz   |            |
| Clock HIGH time                                        | $t_{KH}$   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |            |
| Clock LOW time                                         | $t_{KL}$   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |            |
| <b>Output Times</b>                                    |            |      |     |      |     |      |     |      |     |       |            |
| Clock to output valid                                  | $t_{KQ}$   |      | 6.8 |      | 7.5 |      | 8.5 |      | 9.0 | ns    |            |
| Clock to output invalid                                | $t_{KQX}$  | 1.5  |     | 1.5  |     | 3.0  |     | 3.0  |     | ns    | 2          |
| Clock to output in Low-Z                               | $t_{KQLZ}$ | 1.5  |     | 1.5  |     | 4.0  |     | 4.0  |     | ns    | 2, 3, 4, 5 |
| Clock to output in High-Z                              | $t_{KQHZ}$ |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    | 2, 3, 4, 5 |
| OE# to output valid                                    | $t_{OEQ}$  |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    | 6          |
| OE# to output in Low-Z                                 | $t_{OELZ}$ | 0    |     | 0    |     | 0    |     | 0    |     | ns    | 2, 3, 4, 5 |
| OE# to output in High-Z                                | $t_{OEHZ}$ |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    | 2, 3, 4, 5 |
| <b>Setup Times</b>                                     |            |      |     |      |     |      |     |      |     |       |            |
| Address                                                | $t_{AS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    | 7, 8       |
| Address status (ADSC#, ADSP#)                          | $t_{ADSS}$ | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    | 7, 8       |
| Address advance (ADV#)                                 | $t_{AAS}$  | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    | 7, 8       |
| Byte write enables (BWA#, BWB#, BWC#, BWD#, GW#, BWE#) | $t_{WS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    | 7, 8       |
| Data-in                                                | $t_{DS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    | 7, 8       |
| Chip enable (CE#)                                      | $t_{CES}$  | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    | 7, 8       |
| <b>Hold Times</b>                                      |            |      |     |      |     |      |     |      |     |       |            |
| Address                                                | $t_{AH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5  |     | ns    | 7, 8       |
| Address status (ADSC#, ADSP#)                          | $t_{ADSH}$ | 0.5  |     | 0.5  |     | 0.5  |     | 0.5  |     | ns    | 7, 8       |
| Address advance (ADV#)                                 | $t_{AAH}$  | 0.5  |     | 0.5  |     | 0.5  |     | 0.5  |     | ns    | 7, 8       |
| Byte write enables (BWA#, BWB#, BWC#, BWD#, GW#, BWE#) | $t_{WH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5  |     | ns    | 7, 8       |
| Data-in                                                | $t_{DH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5  |     | ns    | 7, 8       |
| Chip enable (CE#)                                      | $t_{CEH}$  | 0.5  |     | 0.5  |     | 0.5  |     | 0.5  |     | ns    | 7, 8       |

- NOTE:**
1. Test conditions as specified with the output loading as shown in Figure 1 unless otherwise noted.
  2. This parameter is measured with output load as shown in Figure 2.
  3. This parameter is sampled.
  4. Transition is measured  $\pm 150\text{mV}$  from steady state voltage.
  5. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
  6. OE# is a "Don't Care" when a byte write enable is sampled LOW.
  7. A READ cycle is defined by byte write enables all HIGH or ADSP# LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times.
  8. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP# or ADSC# is LOW to remain enabled.

256K x 18, 128K x 32/36  
2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

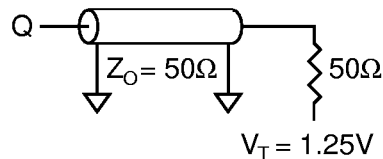
**AC TEST CONDITIONS**

|                                     |                         |
|-------------------------------------|-------------------------|
| Input pulse levels .....            | V <sub>ss</sub> to 2.5V |
| Input rise and fall times .....     | 1ns                     |
| Input timing reference levels ..... | 1.25V                   |
| Output reference levels .....       | 1.25V                   |
| Output load .....                   | See Figures 1 and 2     |

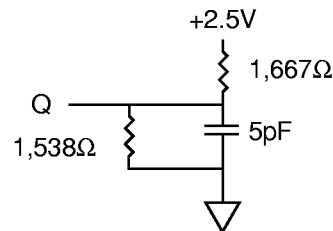
**LOAD DERATING CURVES**

Micron 256K x 18, 128K x 32 and 128K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.



**Figure 1**  
**OUTPUT LOAD EQUIVALENT**



**Figure 2**  
**OUTPUT LOAD EQUIVALENT**

**SNOOZE MODE**

SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to  $I_{SB2Z}$ . The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

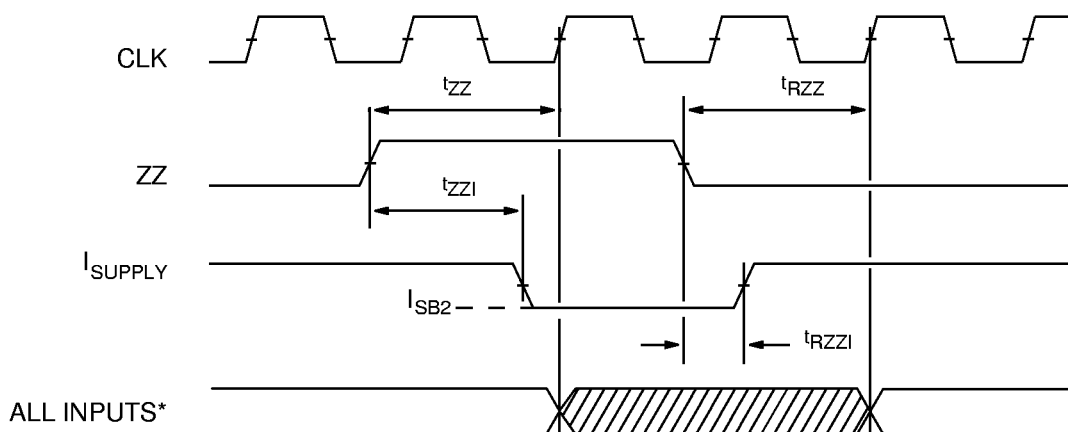
The ZZ pin (pin 64) is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH,  $I_{SB2Z}$  is guaranteed after the setup time  $t_{ZZ}$  is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

**SNOOZE MODE ELECTRICAL CHARACTERISTICS**

| DESCRIPTION                        | CONDITIONS       | SYMBOL     | MIN      | MAX      | UNITS | NOTES |
|------------------------------------|------------------|------------|----------|----------|-------|-------|
| Current during SNOOZE MODE         | $ZZ \geq V_{IH}$ | $I_{SB2Z}$ |          | 10       | mA    |       |
| ZZ active to input ignored         |                  | $t_{ZZ}$   |          | $t_{KC}$ | ns    | 1     |
| ZZ inactive to input sampled       |                  | $t_{RZZ}$  | $t_{KC}$ |          | ns    | 1     |
| ZZ active to snooze current        |                  | $t_{ZZI}$  |          | $t_{KC}$ | ns    | 1     |
| ZZ inactive to exit snooze current |                  | $t_{RZZI}$ | 0        |          | ns    | 1     |

**NOTE:** 1. This parameter is sampled.

**SNOOZE MODE WAVEFORM**

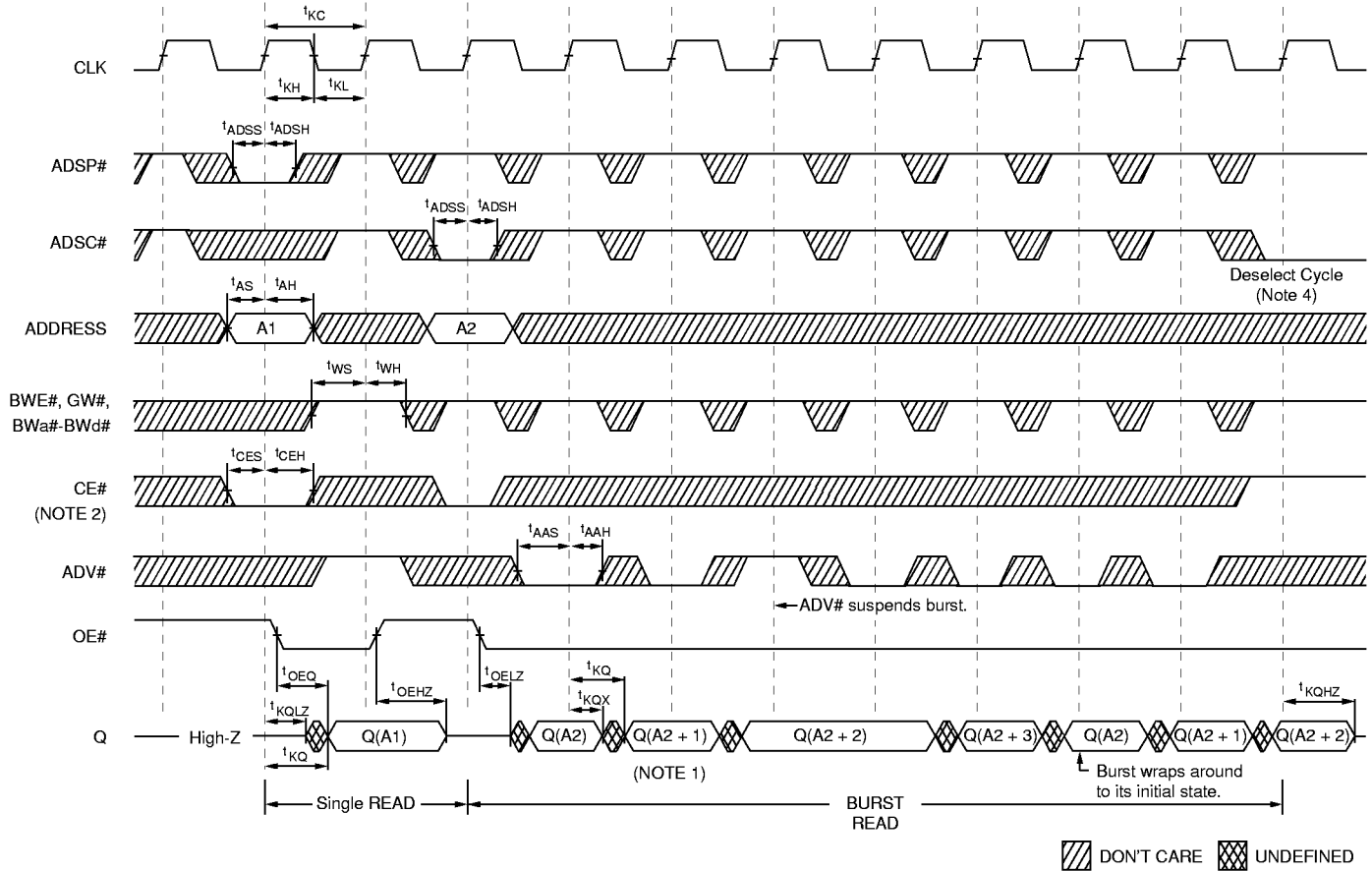


\* Except ZZ

DON'T CARE

**ADVANCE**  
**256K x 18, 128K x 32/36**  
**2.5V I/O, FLOW-THROUGH SYNCBURST SRAM**

**READ TIMING**



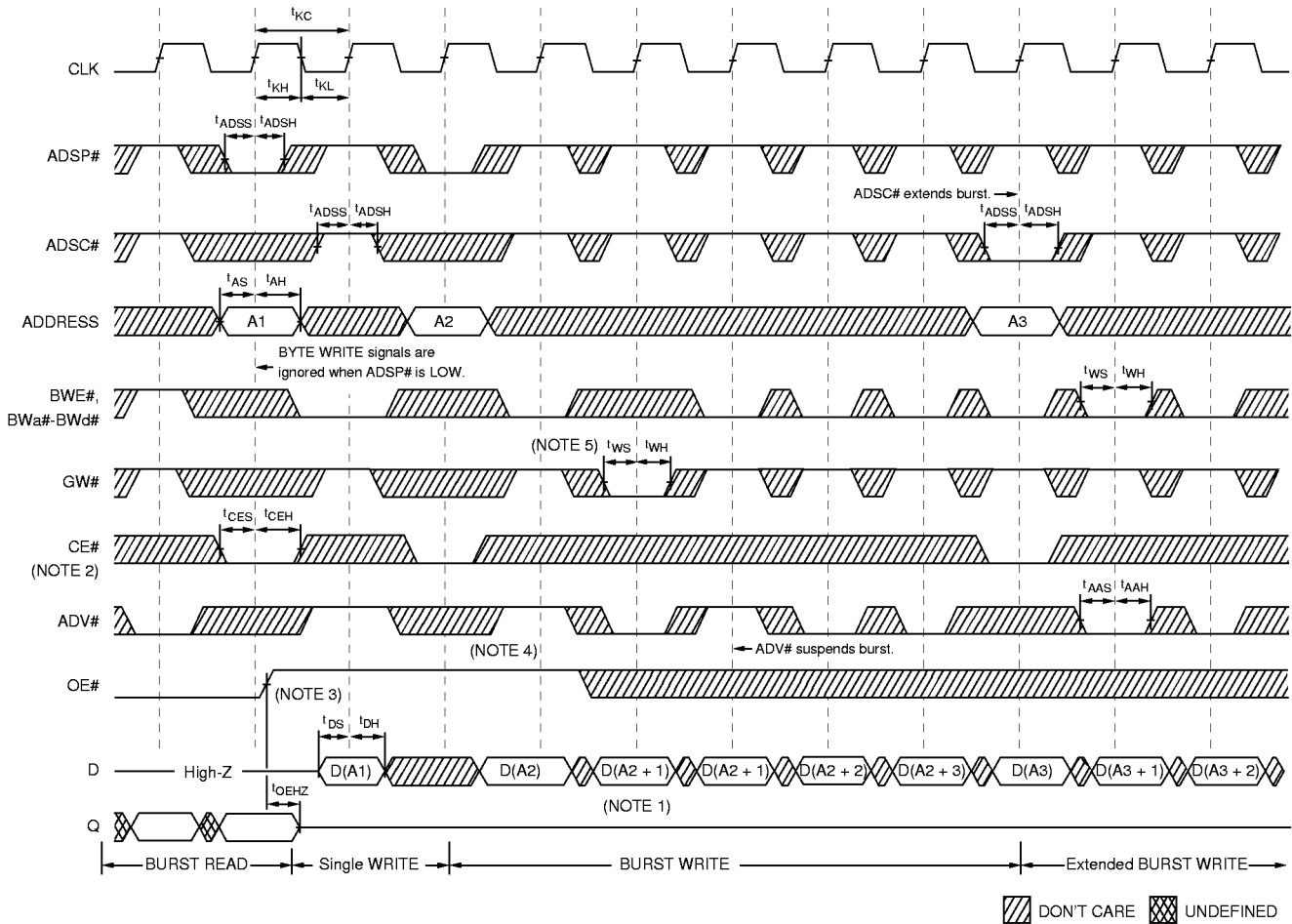
**READ TIMING PARAMETERS**

| SYMBOL     | -6.8 |     | -7.5 |     | -8.5 |     | -9   |     | UNITS |
|------------|------|-----|------|-----|------|-----|------|-----|-------|
|            | MIN  | MAX | MIN  | MAX | MIN  | MAX | MIN  | MAX |       |
| $t_{KC}$   | 8.0  |     | 8.8  |     | 10.0 |     | 10.5 |     | ns    |
| $t_{KF}$   |      | 125 |      | 113 |      | 100 |      | 94  | MHz   |
| $t_{KH}$   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |
| $t_{KL}$   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |
| $t_{KQ}$   |      | 6.8 |      | 7.5 |      | 8.5 |      | 9.0 | ns    |
| $t_{KQX}$  | 1.5  |     | 1.5  |     | 3.0  |     | 3.0  |     | ns    |
| $t_{KQLZ}$ | 1.5  |     | 1.5  |     | 4.0  |     | 4.0  |     | ns    |
| $t_{KQHZ}$ |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    |
| $t_{OEQ}$  |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    |
| $t_{OELZ}$ | 0    |     | 0    |     | 0    |     | 0    |     | ns    |
| $t_{OEHZ}$ |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    |

| SYMBOL     | -6.8 |     | -7.5 |     | -8.5 |     | -9  |     | UNITS |
|------------|------|-----|------|-----|------|-----|-----|-----|-------|
|            | MIN  | MAX | MIN  | MAX | MIN  | MAX | MIN | MAX |       |
| $t_{AS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| $t_{ADSS}$ | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| $t_{AAS}$  | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| $t_{WS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| $t_{CES}$  | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| $t_{AH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{ADSH}$ | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{AAH}$  | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{WH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{CEH}$  | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |

- NOTE:**
1. Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
  2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
  3. Timing is shown assuming that the device was not enabled before entering into this sequence.
  4. Outputs are disabled  $t_{KQHZ}$  after deselect.

**WRITE TIMING**



**WRITE TIMING PARAMETERS**

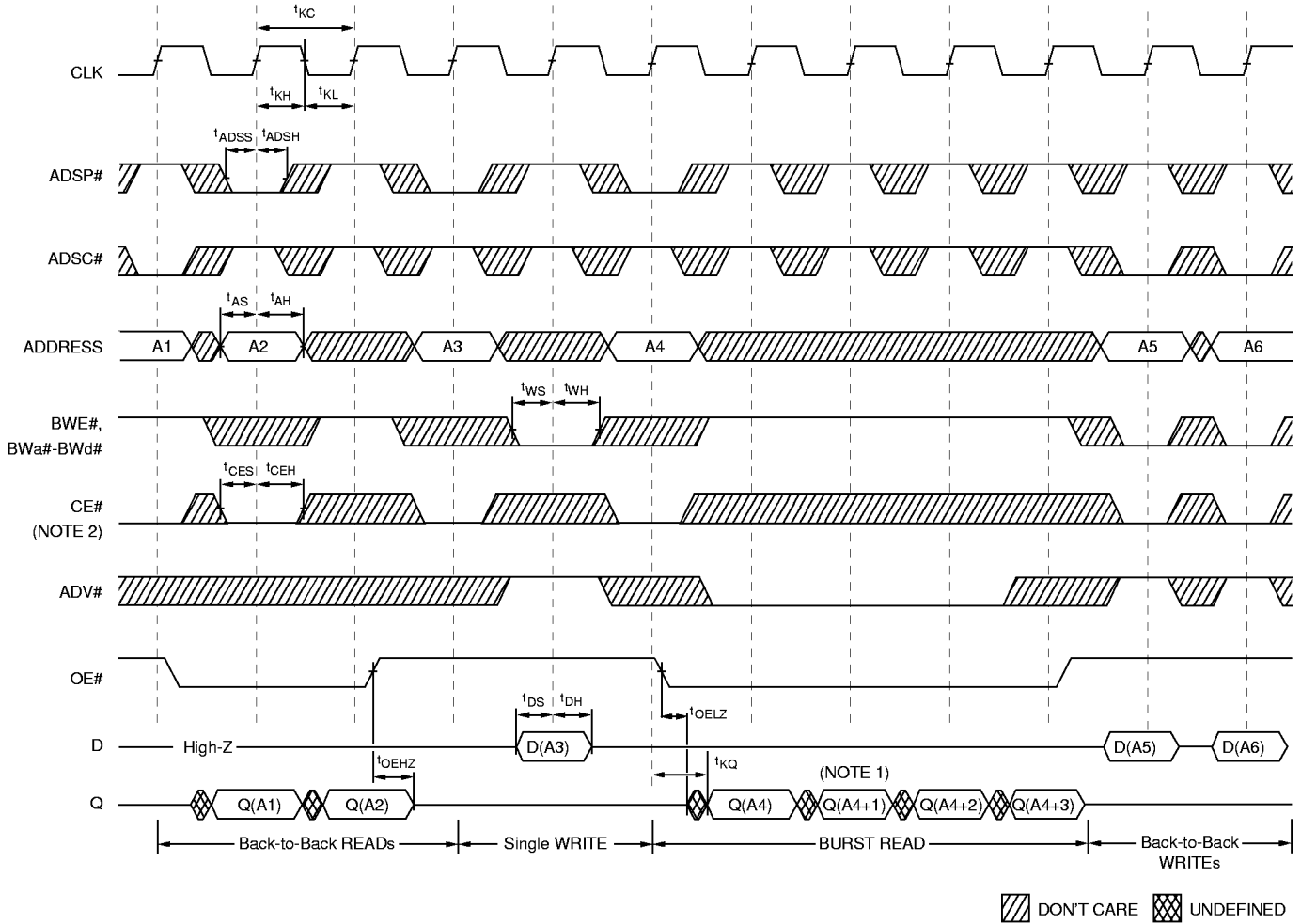
| SYMBOL     | -6.8 |     | -7.5 |     | -8.5 |     | -9   |     | UNITS |
|------------|------|-----|------|-----|------|-----|------|-----|-------|
|            | MIN  | MAX | MIN  | MAX | MIN  | MAX | MIN  | MAX |       |
| $t_{KC}$   | 8.0  |     | 8.8  |     | 10.0 |     | 10.5 |     | ns    |
| $f_{KF}$   |      | 125 |      | 113 |      | 100 |      | 94  | MHz   |
| $t_{KH}$   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |
| $t_{KL}$   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |
| $t_{OEZH}$ |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    |
| $t_{AS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    |
| $t_{ADSS}$ | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    |
| $t_{AAS}$  | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    |
| $t_{WS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    |

| SYMBOL     | -6.8 |     | -7.5 |     | -8.5 |     | -9  |     | UNITS |
|------------|------|-----|------|-----|------|-----|-----|-----|-------|
|            | MIN  | MAX | MIN  | MAX | MIN  | MAX | MIN | MAX |       |
| $t_{DS}$   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| $t_{CES}$  | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| $t_{AH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{ADSH}$ | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{AAH}$  | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{WH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{DH}$   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| $t_{CEH}$  | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |

- NOTE:**
- D(A2) refers to output from address A2. D(A2 + 1) refers to output from the next internal burst address following A2.
  - CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
  - OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
  - ADV# must be HIGH to permit a WRITE to the loaded address.
  - Full-width WRITE can be initiated by GW# LOW; or GW# HIGH and BWE#, BWA# and BWb# LOW for x18 device; or GW# HIGH and BWE#, BWA#-BWd# LOW for x32 and x36 devices.

**ADVANCE**  
**256K x 18, 128K x 32/36**  
**2.5V I/O, FLOW-THROUGH SYNCBURST SRAM**

**READ/WRITE TIMING**



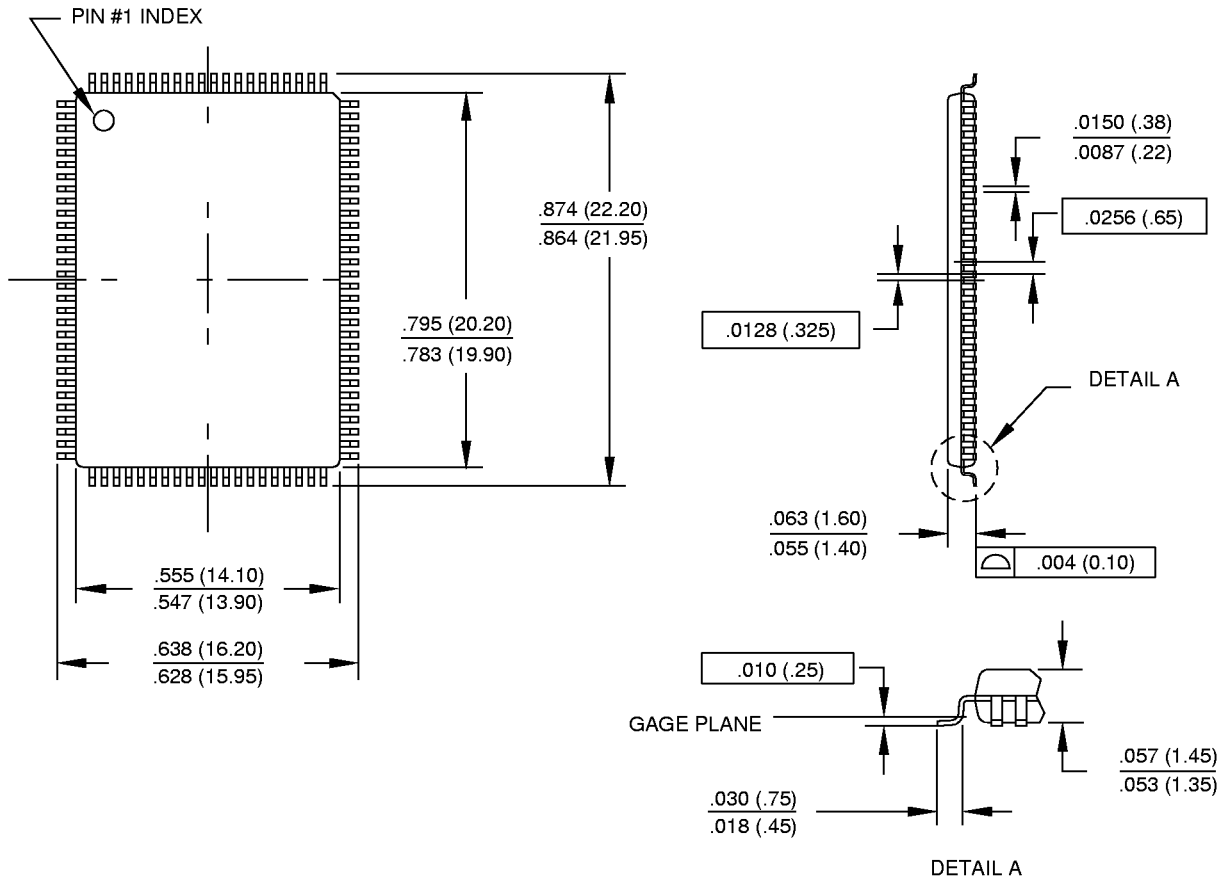
**READ/WRITE TIMING PARAMETERS**

| SYMBOL            | -6.8 |     | -7.5 |     | -8.5 |     | -9   |     | UNITS |
|-------------------|------|-----|------|-----|------|-----|------|-----|-------|
|                   | MIN  | MAX | MIN  | MAX | MIN  | MAX | MIN  | MAX |       |
| t <sub>KC</sub>   | 8.0  |     | 8.8  |     | 10.0 |     | 10.5 |     | ns    |
| t <sub>KF</sub>   |      | 125 |      | 113 |      | 100 |      | 94  | MHz   |
| t <sub>KH</sub>   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |
| t <sub>KL</sub>   | 1.8  |     | 1.9  |     | 1.9  |     | 3.8  |     | ns    |
| t <sub>KQ</sub>   |      | 6.8 |      | 7.5 |      | 8.5 |      | 9.0 | ns    |
| t <sub>OELZ</sub> | 0    |     | 0    |     | 0    |     | 0    |     | ns    |
| t <sub>OEHZ</sub> |      | 3.8 |      | 4.2 |      | 5.0 |      | 5.0 | ns    |
| t <sub>AS</sub>   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    |
| t <sub>ADSS</sub> | 1.8  |     | 2.0  |     | 2.0  |     | 2.5  |     | ns    |

| SYMBOL            | -6.8 |     | -7.5 |     | -8.5 |     | -9  |     | UNITS |
|-------------------|------|-----|------|-----|------|-----|-----|-----|-------|
|                   | MIN  | MAX | MIN  | MAX | MIN  | MAX | MIN | MAX |       |
| t <sub>WS</sub>   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| t <sub>DS</sub>   | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| t <sub>CES</sub>  | 1.8  |     | 2.0  |     | 2.0  |     | 2.5 |     | ns    |
| t <sub>AH</sub>   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| t <sub>ADSH</sub> | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| t <sub>WH</sub>   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| t <sub>DH</sub>   | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |
| t <sub>CEH</sub>  | 0.5  |     | 0.5  |     | 0.5  |     | 0.5 |     | ns    |

- NOTE:**
- Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
  - CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
  - The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC# or ADV# cycle is performed.
  - GW# is HIGH.
  - Back-to-back READs may be controlled by either ADSP# or ADSC#.

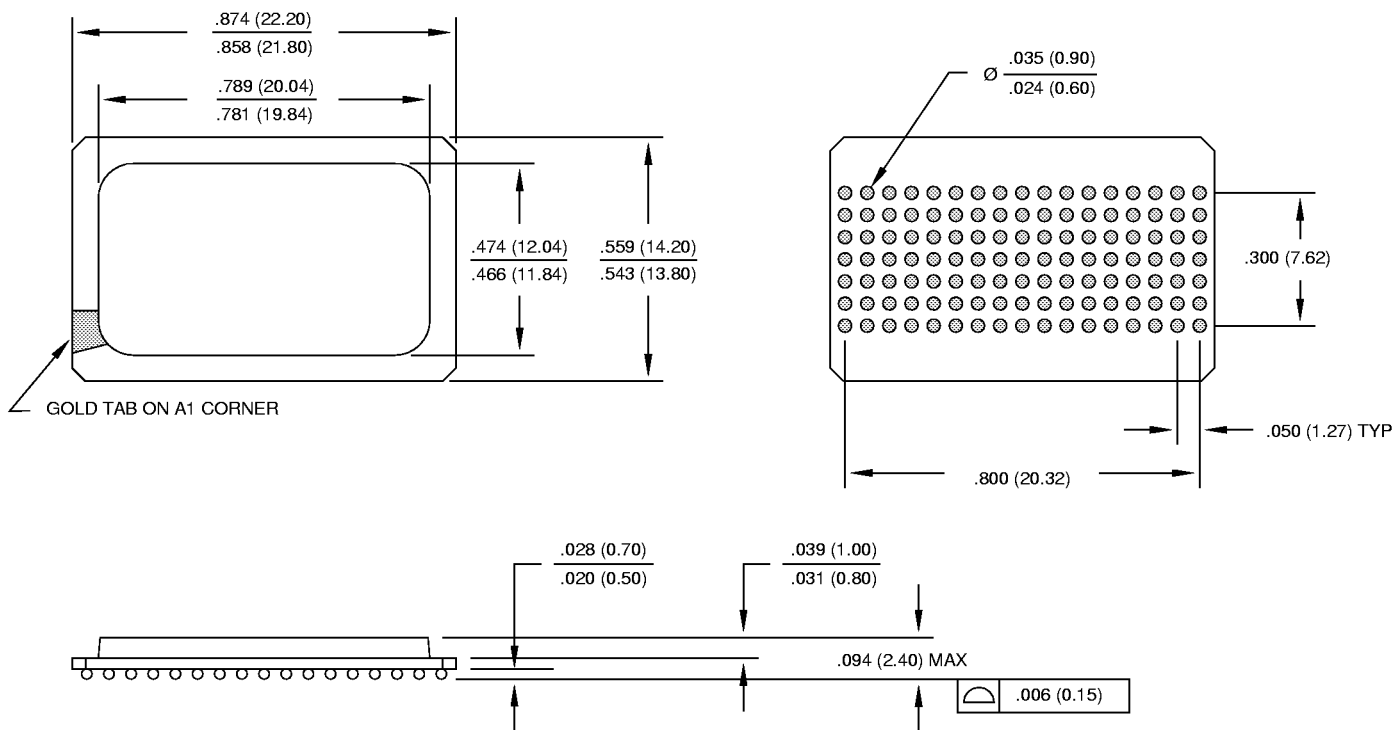
100-PIN TQFP  
SA-1



- NOTE:**
1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

256K x 18, 128K x 32/36  
2.5V I/O, FLOW-THROUGH SYNCBURST SRAM

119-BUMP BGA  
SB-1



- NOTE:**
1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.
  2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.



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