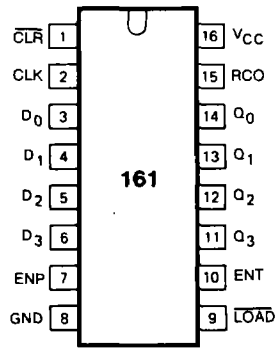
GD54/74HC161, GD54/74HCT161
SYNCHRONOUS BINARY COUNTER WITH ASYNCHRONOUS CLEAR

General Description

These devices are identical in pinout to the 54/74LS161. They contain a 4-bit binary counter consisting of four flip-flops. All flip-flops are clocked simultaneously on the positive edge of the clock input. Counters may be preset using the load input at the rising edge of clock. All the counters may be cleared asynchronously by utilizing the clear input. When the clear is taken low the counter is cleared immediately regardless of the clock. The HC/HCT 161 is similar in function to the HC/HCT 163 which is cleared synchronously. These devices are chararcterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J . Ceramic Dual In Line Package
Suffix-D . Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{CLR}$	CLK	ENP	ENT	$\overline{LOAD}$	D_n	Q_n	RCO
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold	H	X	l	X	h	X	q_n	*
(do nothing)	H	X	X	l	h	X	q_n	L

Note to function table

* The RCO output is HIGH when ENT is HIGH and the counter is at terminal count (HHHH).
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition
X = don't care
↑ = LOW-to-HIGH CLK transition

Logic Diagram

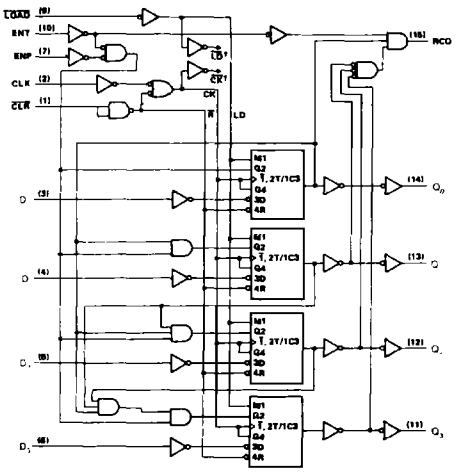


Fig. 1 Logic diagram

Output Sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (HC/HCT 161 is asynchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, zero, one, and two
4. Inhibit

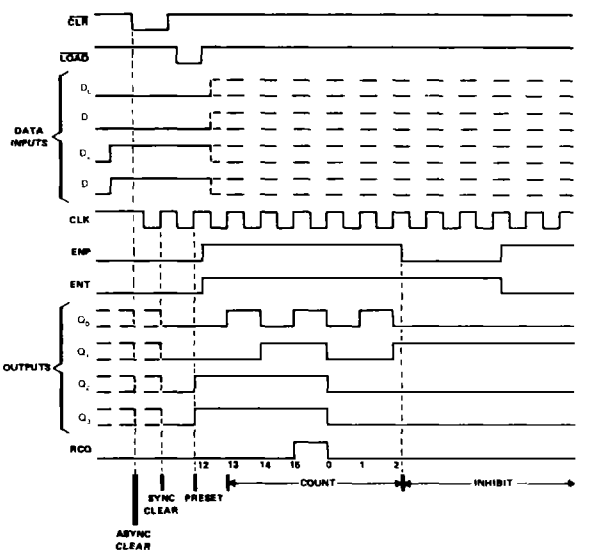


Fig. 2 Output sequence

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX	UNIT
V_{CC}	DC Supply voltage		−0.5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for $V_I<-0.5$ or $V_I>V_{CC}+0.5V$		|20|	mA
I_O	DC output source or sink current	for $-0.5V<V_O<V_{CC}+0.5V$		|25|	mA
I_{CC}	DC V_{CC} or GND current			|50|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC}: GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: GD74 Types	−40	+85	°C
GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f: GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5V		500	

Logic Diagram

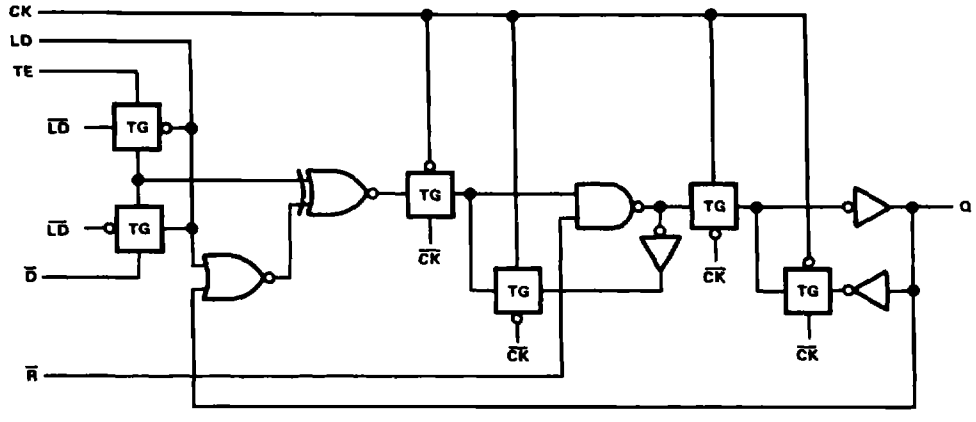


Fig. 3 Each D/T flip-flop

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HC161		GD54HC161		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX	
V_{IH}	HIGH level input Voltage			2.0 4.5 6 0	1.5 3.15 4.2			1.5 3.15 4.2		1 5 3.15 4.2		V
V_{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0 3 0.9 1.2		0 3 0 9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0 4 5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1 9 4.4 5.9		1.9 4.4 5 9		V
			$I_{OH}=-4mA$ $I_{OH}=-5.2mA$	4 5 6 0	3 98 5.48	4.3 5.2		3 84 5 34		3 7 5 2		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2 0 4.5 6 0			0.1 0.1 0 1		0 1 0 1 0.1		0 1 0 1 0 1	V
			$I_{OL}=4mA$ $I_{OL}=5.2mA$	4 5 6.0		0 17 0 15	0 26 0.26		0 33 0 33		0.4 0 4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		6 0			0 1		1.0		1 0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		6 0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HCT161		GD54HCT161		UNIT
					MIN	TYP.	MAX.	MIN	MAX	MIN	MAX	
V_{IH}	HIGH level input Voltage			4.5 to 5.5	2 0			2 0		2 0		V
V_{IL}	LOW level input voltage			4.5 to 5.5			0 8		0.8		0 8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4 4	4 5		4 4		4 4		V
			$I_{OH}=-4mA$	4 5	3 98	4.3		3 84		3 7		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4 5			0 1		0 1		0 1	V
			$I_{OL}=4mA$	4 5		0.17	0 26		0 33		0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$or GND		5 5			0 1		1 0		1 0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		5 5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HC161		GD54HC161		UNIT
				MIN.	TYP.	MAX.	MIN	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{CLR}$ low, CLK	2 0 4.5 6.0	80 16 14	22 8 6		100 20 17		120 24 20		ns
t_{su}	Setup time	D_n to CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 27 20		ns
		$\overline{LOAD}$ to CLK	2 0 4.5 6 0	135 25 22			170 31 29		205 40 35		ns
		ENP, ENT to CLK	2.0 4 5 6 0	135 27 23			250 50 43		300 60 51		ns
t_{rec}	Recovery time	$\overline{CLR}$ to CLK	2.0 4.5 6.0	100 20 17			125 25 21		150 30 26		ns
t_h	Hold time	All sync, input to CLK	2 0 4 5 6.0	0 0 0			0 0 0		0 0 0		ns

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HC161		GD54HC161		UNIT
			MIN	TYP.	MAX.	MIN.	MAX	MIN	MAX	
f_{max}	*Maximum clock pulse frequency*	2 0 4 5 6.0	6 31 36	14 40 44		5 25 29		4.2 21 25		MHz
t_{PLH}/ t_{PHL}	Propagation Delay Time CLK to RCO	2.0 4.5 6.0		60 20 16	200 40 31		250 52 43		305 63 52	ns
t_{PLH}/ t_{PHL}	Propagation Delay Time CLK to Qn	2.0 4.5 6.0		58 19 17	180 34 28		225 43 37		275 53 46	ns
t_{PLH}/ t_{PHL}	Propagation Delay Time ENT to RCO	2.0 4.5 6.0		45 15 13	140 28 25		180 36 32		215 43 38	ns
t_{PLH}/ t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Qn	2.0 4 5 6 0		58 18 16	200 35 30		255 46 42		305 56 51	ns
t_{PLH}/ t_{PHL}	Propagation Delay Time $\overline{CLR}$ to RCO	2.0 4.5 6 0		60 20 18	210 40 34		265 51 45		315 62 55	ns
t_{TLH}/ t_{THL}	Output Transition Time	2 0 4 5 6.0		38 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HCT161		GD54HCT161		UNIT
				MIN	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{CLR}$ low, CLK	4.5	20			24		28		ns
t_{su}	Setup time	D_n to CLK	4 5	20			24		28		ns
		$\overline{LOAD}$ to CLK	4 5	30			38		45		ns
		ENP, ENT to CLK	4 5	30			54		64		ns
t_{rec}	Recovery time	$\overline{CLR}$ to CLK	4 5	24			29		34		ns
t_h	Hold time	All sync, input ıput to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HCT161		GD54HCT161		UNIT
			MIN	TYP.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{max}	Maximum clock pulse frequency	4.5	16	28		13		11		MHz
t_{PLH}/ t_{PHL}	Propagation Delay Time CLK to RCO	4 5		26		56		67		ns
t_{PLH}/ t_{PHL}	Propagation Delay Time CLK to Qn	4.5		24		47		57		ns
t_{PLH}/ t_{PHL}	Propagation Delay Time ENT to RCO	4.5		21		40		47		ns
t_{PLH}/ t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Qn	4.5		24		50		60		ns
t_{PLH}/ t_{PHL}	Propagation Delay Time $\overline{CLR}$ to RCO	4 5		26		55		67		ns
t_{TLH}/ t_{THL}	Output Transition Time	4 5		7		19		22		ns

AC Waveforms

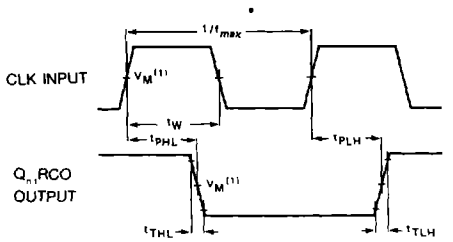


Fig. 4 Waveforms showing the clock (CLK) to outputs (Q_n, RCO) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

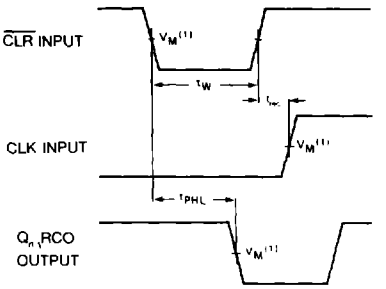


Fig. 5 Waveforms showing the master clear ($\overline{CLR}$) pulse width, the master clear to output (Q_n, RCO) propagation delays and the master clear to clock (CLK) recovery time.

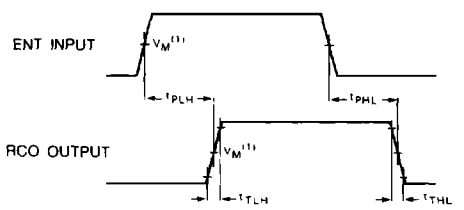


Fig. 6 Waveforms showing the input (ENT) to output (RCO) propagation delays and output transition times.

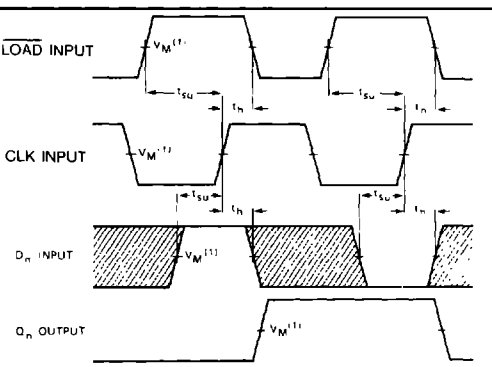


Fig. 7 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input ($\overline{LOAD}$)

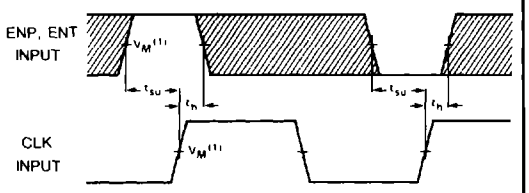


Fig. 8 Waveforms showing the ENP and ENT set-up and hold times.

Note to Figs 7 and 8
The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M=50%, V_I=GND to V_{CC}
HCT V_M=1.3V, V_I=GND to 3V.