

SN54176, SN54177, SN74176, SN74177
35-MHz PRESETTABLE DECADE AND
BINARY COUNTERS/LATCHES
 MAY 1971—REVISED MARCH 1988

SDLS069

- Reduced-Power Versions of SN54196, SN54197, SN74196, and SN74197 50-MHz Counters
- D-C Coupled Counters Designed to Replace Signetics 8280, 8281, 8290, and 8291 Counters in Most Applications
- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Counts at Input Frequencies from 0 to 35 MHz
- Input Clamping Diodes Simplify System Design

description

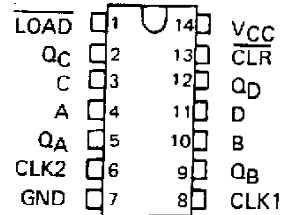
These high-speed monolithic counters consist of four d-c coupled master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54176, SN74176) or a divide-by-two and a divide-by-eight counter (SN54177, SN74177). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

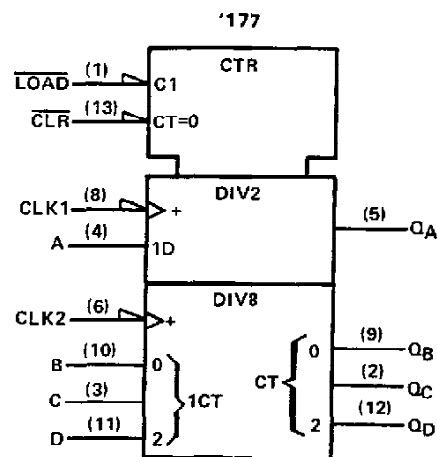
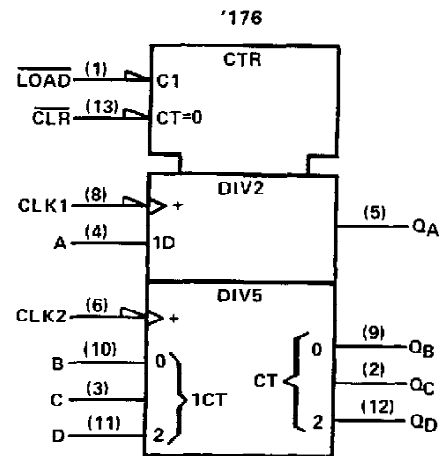
These high-speed counters will accept count frequencies of 0 to 35 megahertz at the clock-1 input and 0 to 17.5 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The circuits are compatible with most TTL logic families. Typical power dissipation is 150 milliwatts. The SN54176 and SN54177 circuits are characterized for operation over the full military temperature range of -55 °C to 125 °C; the SN74176 and SN74177 circuits are characterized for operation from 0 °C to 70 °C.

SN54176, SN54177 . . . J PACKAGE
 SN74176, SN74177 . . . N PACKAGE
 (TOP VIEW)



logic symbols†



† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54176, SN54177, SN74176, SN74177 35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

typical count configurations

SN54176 and SN74176

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

- When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at right.
- If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.
- For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B , Q_C , and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

FUNCTION TABLES
SN54176, SN74176

DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

SN54177 and SN74177

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

- When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A , Q_B , Q_C , and Q_D outputs as shown in the function table at right.
- When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B , Q_C , and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

FUNCTION TABLE
SN54177, SN74177

(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level

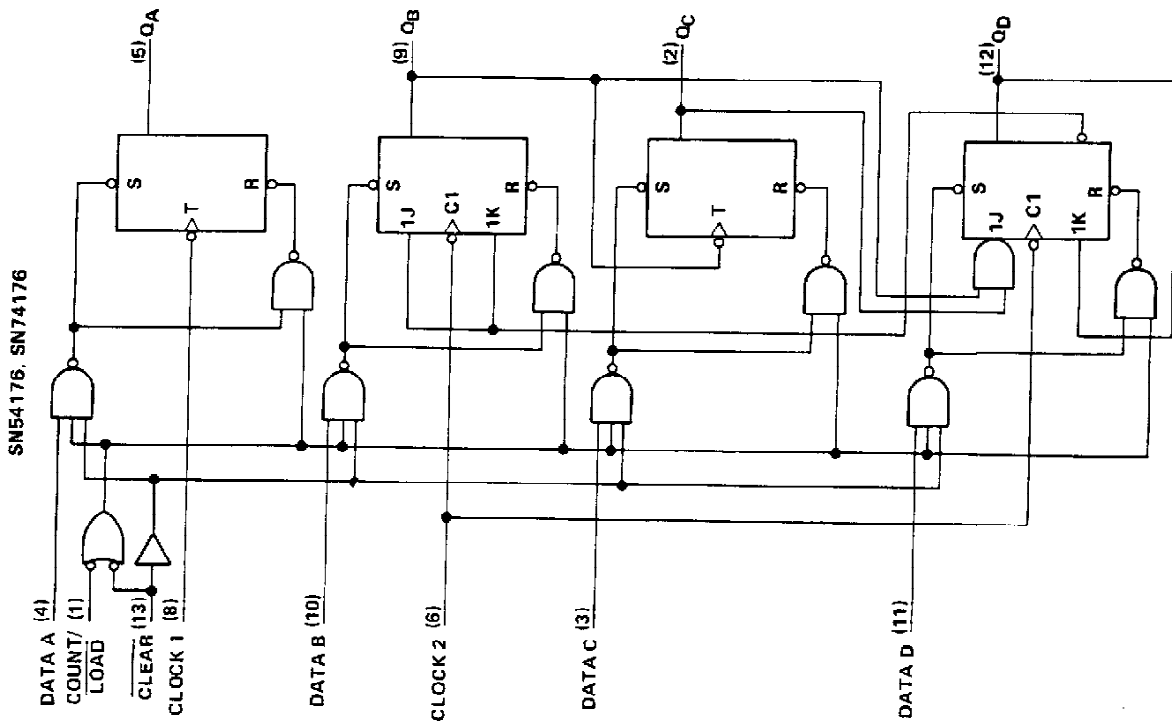
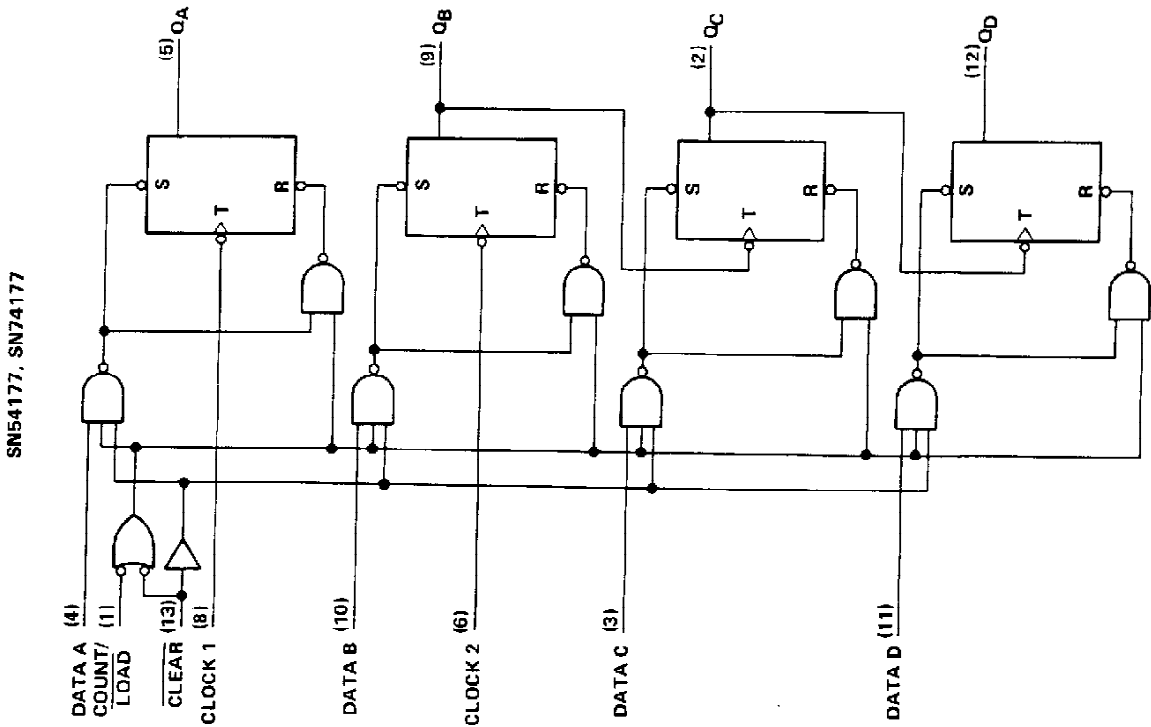
NOTE A: Output Q_A connected to clock-2 input.

TEXAS
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SN54176, SN54177, SN74176, SN74177
 35-MHz PRESETTABLE DECADE AND
 BINARY COUNTERS/LATCHES

logic diagrams (positive logic)

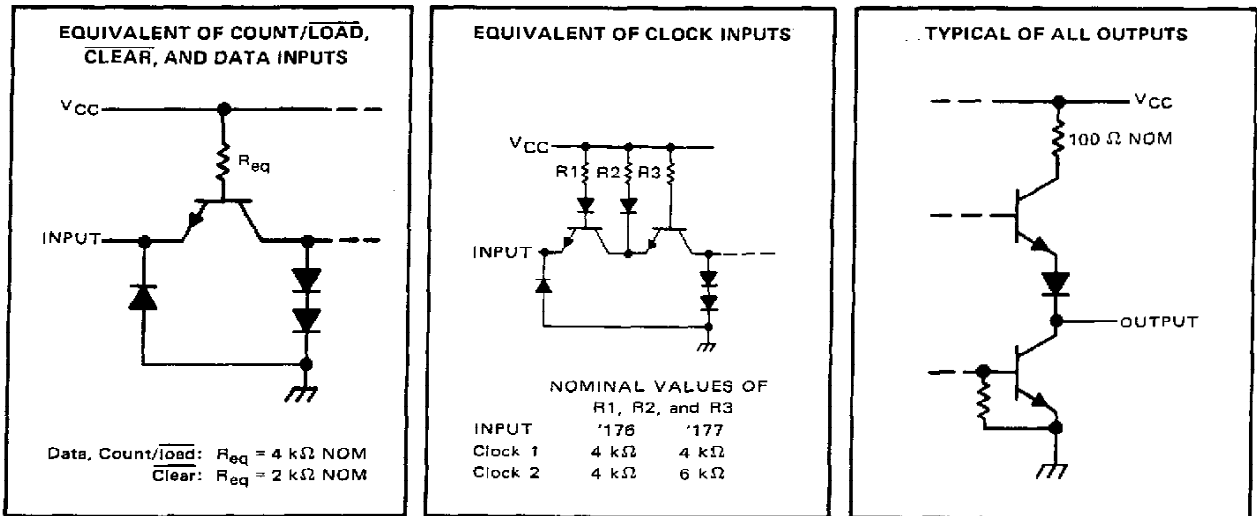


TEXAS
 INSTRUMENTS

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SN54176, SN54177, SN74176, SN74177
35-MHz PRESETTABLE DECADE AND
BINARY COUNTERS/LATCHES

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54176, SN54177 Circuits	-55°C to 125°C
SN74176, SN74177 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
 2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN54'	4.5	5	5.5	V
	SN74'	4.75	5	5.25	
High-level output current, I_{OH}				-800	μA
Low-level output current, I_{OL}				16	mA
Count frequency (see Figure 1)	Clock-1 input	0		35	MHz
	Clock-2 input	0		17.5	
Pulse width, t_w (see Figure 1)	Clock-1 input		14		ns
	Clock-2 input		28		
	Clear		20		
	Load		25		
Input hold time, t_h (see Figure 1)	High-level data		$t_w(\text{load})$		ns
	Low-level data		$t_w(\text{load})$		
Input setup time, t_{SU} (see Figure 1)	High-level data		15		ns
	Low-level data		20		
Count enable time, t_{enable} (see Note 3 and Figure 1)			25		ns
Operating free-air temperature, T_A	SN54'	-55		125	°C
	SN74'	0		70	

NOTE 3: Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.



SN54176, SN54177, SN74176, SN74177
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54176, SN74176			SN54177, SN74177			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage		0.8			0.8			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA	-1.5			-1.5			V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		2.4	3.4	V	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA¶	0.2	0.4		0.2	0.4	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH} High-level input current	Data, count/load	40			40			µA
	Clear, clock 1	80			80			
	Clock 2	120			80			
I _{IL} Low-level input current	Data, count/load	-1.6			-1.6			mA
	Clear	-3.2			-3.2			
	Clock 1	-4.8			-4.8			
	Clock 2	-4.8			-3.2			
I _{OS} Short-circuit output current §	V _{CC} = MAX	SN54'	-20	-57	-20	-57	mA	
		SN74'	-18	-57	-18	-57		
I _{CC} Supply current	V _{CC} = MAX, See Note 4	30	48		30	48	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

¶ Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF, T_A = 25°C, see figure 1

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	SN54176, SN74176			SN54177, SN74177			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	Clock 1	Q _A	35	50		35	50	MHz	
t _{PLH}	Clock 1	Q _A	8	13		8	13	ns	
t _{PHL}			11	17		11	17		
t _{PLH}	Clock 2	Q _B	11	17		11	17	ns	
t _{PHL}			17	26		17	26		
t _{PLH}	Clock 2	Q _C	27	41		27	41	ns	
t _{PHL}			34	51		34	51		
t _{PLH}	Clock 2	Q _D	13	20		44	66	ns	
t _{PHL}			17	26		50	75		
t _{PLH}	A, B, C, D	Q _A , Q _B , Q _C , Q _D	19	29		19	29	ns	
t _{PHL}			31	46		31	46		
t _{PLH}	Load	Any	29	43		29	43	ns	
t _{PHL}			32	48		32	48		
t _{PHL}	Clear	Any	32	48		32	48	ns	

#f_{max} = maximum count frequency.

t_{PLH} = propagation delay time, low-to-high-level output.

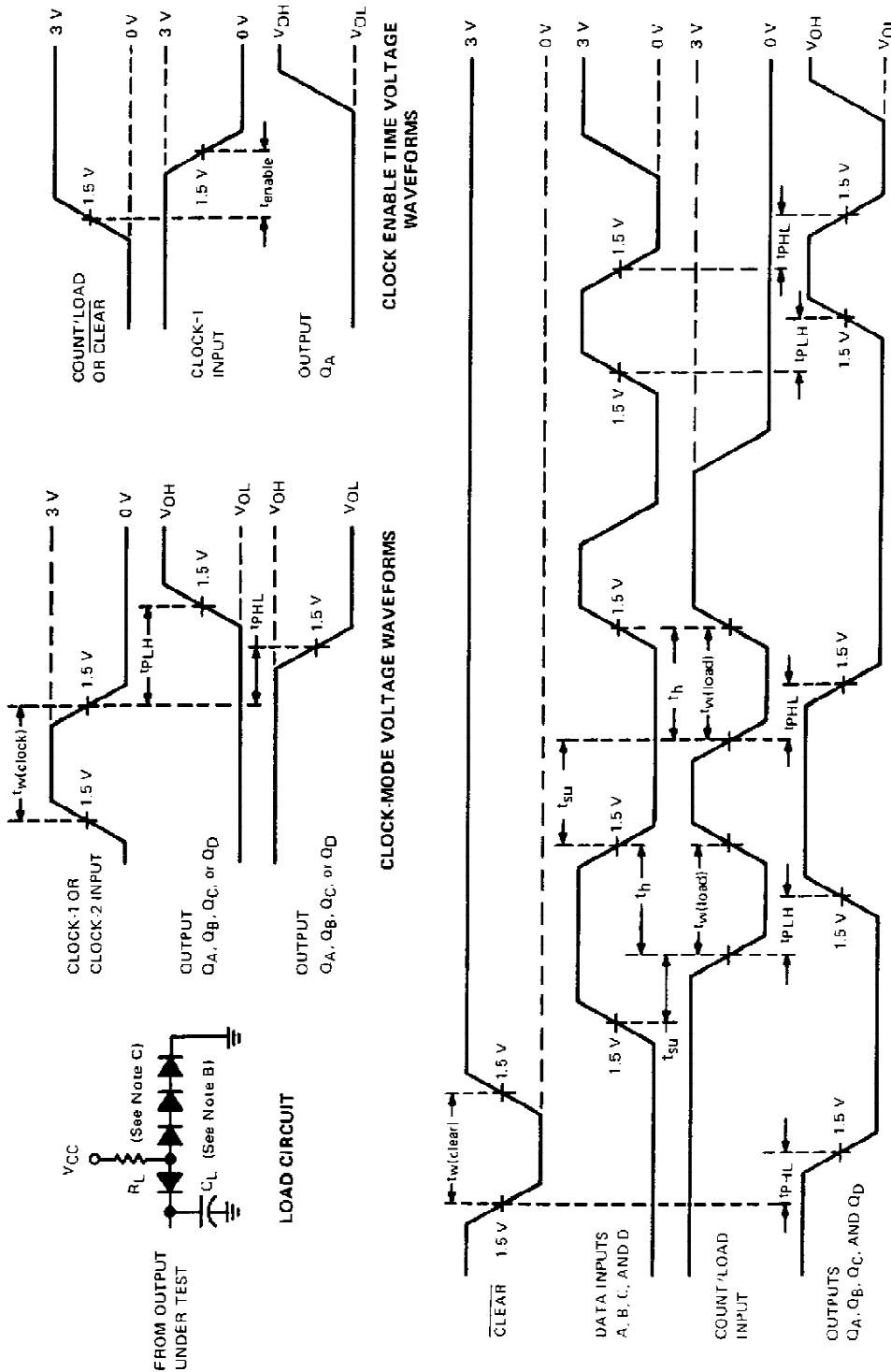
t_{PHL} = propagation delay time, high-to-low-level output.



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PARAMETER MEASUREMENT INFORMATION



CLEAR AND LOAD VOLTAGE WAVEFORMS

FIGURE 1

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r < 5$ ns, and unless specified, $t_f < 5$ ns. When testing t_{max} , vary PRR.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.
 D. Unless otherwise specified, Q_A is connected to clock 2.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74177N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.