Saratoga Semiconductor

SSM7161/2

64K 16,384 Words by 4 Bits BiCMOS TTL Static RAM
with Separate Data Inputs and Outputs

FEATURES

- **Fast Access Times**
  15/20/25ns Commercial Temperature
  20/25/35ns Military Temperature
- **Separate Data Inputs & Outputs**
- **Full Military 883B Compliant**
- **Industry Standard 28-Pin DIP Packages**
- **Transparent Write (SSM7161)**
- **SABiC BiCMOS Fabrication Technology**

DESCRIPTION

The SSM7161 and SSM7162 are high performance 64K BiCMOS static RAMs organized 16,384 words by 4 bits with separate data inputs and outputs. The devices are targeted for use in main, cache and buffer memories, as well as writeable control store in mid-range computers. They are also designed for use in communication, industrial and military equipment applications.

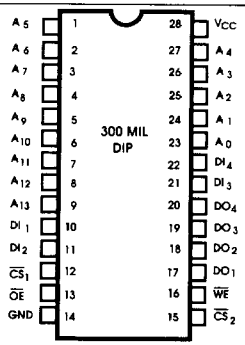
The high speed (15ns), low active power consumption (125mA) and high output drive (16mA) of the SSM7161 and SSM7162 when compared to equivalent CMOS TTL circuits is achieved through utilization of Saratoga Semiconductor's exclusive "Self-Aligned Bipolar CMOS" (SABiC) wafer fabrication technology. SABiC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in both performance and reliability.

Writing to the device occurs when both the Chip Select inputs ($\overline{CS}_1$, $\overline{CS}_2$) and the Write Enable ($\overline{WE}$) input are low. Data on the four Data Input pins (DI_1 - DI_4) is written into the memory cell specified by the 14 bit address placed on the Address Inputs (A_0 - A_{13}). With $\overline{CS}$ and $\overline{CS}$ low, $\overline{WE}$ high and the Output Enable input ($\overline{OE}$) low, the content of the addressed memory cell is transfered to the Input/Output pins (DO_1 - DO_4).

The SSM7161 offers a transparent write feature where the Data Output pins (DO_1 - DO_4) contain the information found on the Data Input pins (DI_1 - DI_4) while the device is in write mode. The SSM7162 Data Output pins remain in a high impedance state while the device is in write mode.

All inputs and outputs of the device are TTL compatible and operate from a single 5V supply. Fully static circuitry is used and balanced read and write cycles are provided.

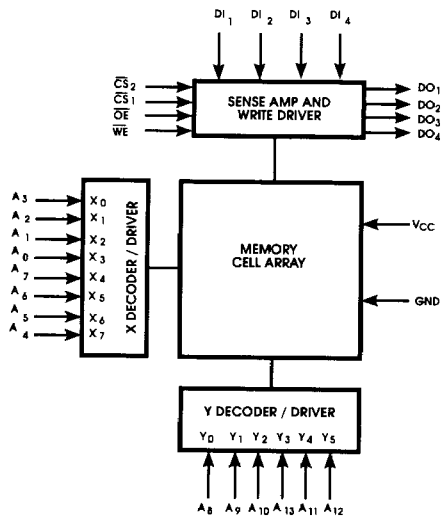
PIN CONFIGURATION



PIN IDENTIFICATION

A_0 - A_{13}	Address Inputs
DI_1 - DI_4	Data Inputs
DO_1 - DO_4	Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
Vcc	Power Supply Pin
GND	Ground Pin

FUNCTIONAL BLOCK DIAGRAM



April 1989

TRUTH TABLE

MODE	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	DIn	DO_n SSM7161	DO_n SSM7162	POWER
Read	L	L	H	L	X	DO	DO	ACTIVE
Write '0'	L	L	L	X	L	L	HIGH Z	ACTIVE
Write '1'	L	L	L	X	H	H	HIGH Z	ACTIVE
Output Disabled	L	L	H	H	X	HIGH Z	HIGH Z	ACTIVE
Disabled	H	X	X	X	X	HIGH Z	HIGH Z	STANDBY
Disabled	X	H	X	X	X	HIGH Z	HIGH Z	STANDBY

H = High Voltage Level X = Irrelevant
L = Low Voltage Level DO = Valid Data Out

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Storage Temperature	T_{STG}	-65	+150	°C
Temperature Under Bias	T_A	-65	+125	°C
Output Current (DC, Output High)	I_{OUT}		20	mA
Power Dissipation	P_D		1.0	W
Power Supply Voltage	V_{CC}	-0.5	+7	V

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

SPECIFIED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Commercial Temperature Range	T_A	0	+70	°C
MilitaryTemperature Range	T_A	-55	+125	°C
Supply Voltage	V_{CC}	+4.5	+5.5	V
Input High Voltage	V_{IH}	2	V_{CC}	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

NOTE: Specified Operating Conditions define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{CC} = 5V ±10% over specified temperature range

SYMBOL	PARAMETER	TEST CONDITIONS	SSM7161/2 MIN	SSM7161/2 MAX	UNIT
V_{OH}	Output High Voltage	I_{OH} =-4mA; V_{CC} = min	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=16mA ; V_{CC}= min		0.4	V
I_{IX}	Input Leakage Current	V_{CC} = max GND ≤ V_{IN} ≤ V_{CC}	-10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{CS}$ = V_{IH} ; V_{CC}= max GND ≤ V_{OUT} ≤ V_{CC}	-50	+50	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= max; V_{OUT}= GND		-150	mA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL} ; V_{CC} = max Output Open		125	mA

[1] Duration of short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.

AC CHARACTERISTICS

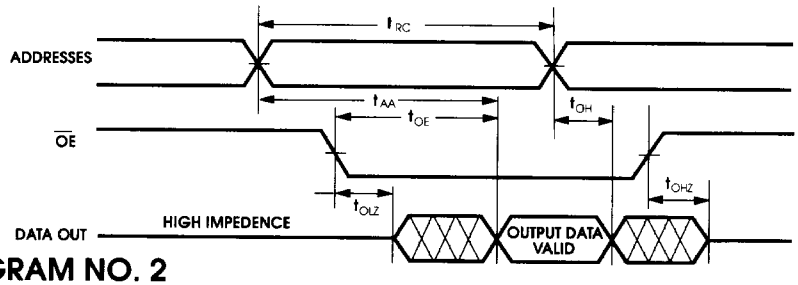
READ CYCLE

PARAMETER	SYMBOL	VALUE				UNIT
		COM SSM7161/2-15*	COM/MIL SSM7161/2-20	COM/MIL SSM7161/2-25	MIL SSM7161/2-35	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
Read Cycle Time	t_{RC}	15	20	25	35	ns
Address Access Time	t_{AA}	15	20	25	35	ns
Chip Select Access Time	t_{ACS}	12	15	20	25	ns
Output Hold from Address Change	t_{OH}	3	3	3	3	ns
Chip Selection to Output in LOW Z	t_{LZ}	3	3	3	3	ns
Chip Selection to Output in HIGH Z	t_{HZ}	8	15	20	25	ns
Output Enable to Output Valid	t_{OE}	12	15	18	20	ns
Output Enable to Output in LOW Z	t_{OLZ}	0	0	0	0	ns
Output Disable to Output in HIGH Z	t_{OHZ}	8	12	15	20	ns

[2] These parameters are sampled and not 100% tested. * Advance Information.

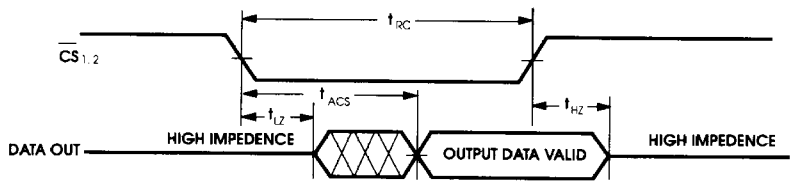
READ CYCLE TIMING DIAGRAM NO. 1

$\overline{WE}$ = V_{IH}, $\overline{CS}_{1,2}$ = V_{IL}. Transition is measured ±500mV from steady state.



READ CYCLE TIMING DIAGRAM NO. 2

$\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}. Transition is measured ±500mV from steady state.
Address valid prior to $\overline{CS}$ transition low.



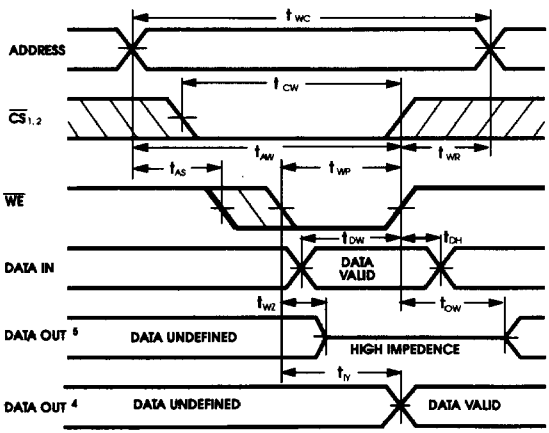
WRITE CYCLE

		VALUE				
		COM SSM7161/2-15*	COM/MIL SSM7161/2-20	COM/MIL SSM7161/2-25	MIL SSM7161/2-35	
	SYMBOL	MIN MAX	MIN MAX	MIN MAX	MIN MAX	UNIT
Write Cycle Time	t_{WC}	15	20	25	35	ns
Chip Selection to End of Write	t_{CW}	15	20	25	35	ns
Address Valid to End of Write	t_{AW}	15	20	25	35	ns
Address Set-up Time	t_{AS}	0	0	0	0	ns
Write Pulse Width	t_{WP}	15	20	25	35	ns
Write Recovery Time	t_{WR}	0	0	0	0	ns
Data Valid to End of Write	t_{DW}	9	12	15	20	ns
Data Hold Time	t_{DH}	0	0	0	0	ns
Data Valid to Output Valid	t_{IY}[2]	15	20	20	30	ns
Write Enable to Output Valid	t_{WY}[2]	15	20	20	30	ns
Write Enable to Output in HIGH Z	t_{WZ}[2]	8	8	10	15	ns
Output Active from End of Write	t_{OW}[2]	0	0	0	0	ns

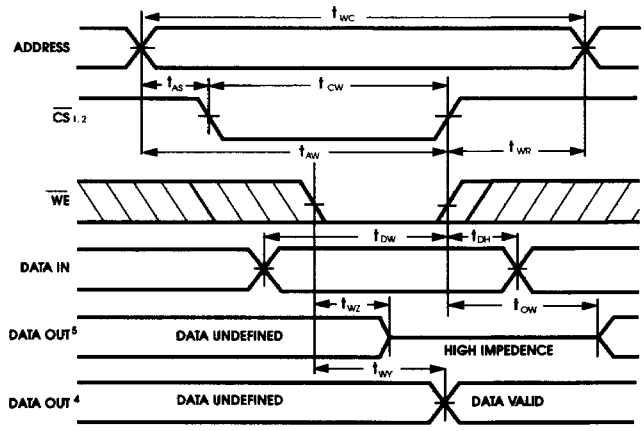
[2] These parameters are sampled and not 100% tested. * Advance Information.

WRITE CYCLE TIMING DIAGRAMS

(WE CONTROLLED) [3]

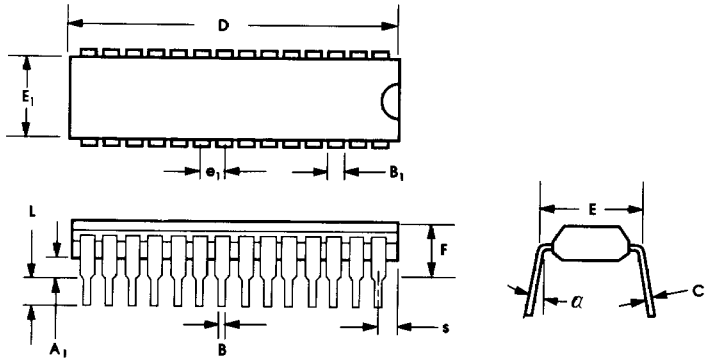


NO.2 ($CS_{1,2}$ CONTROLLED) [3]



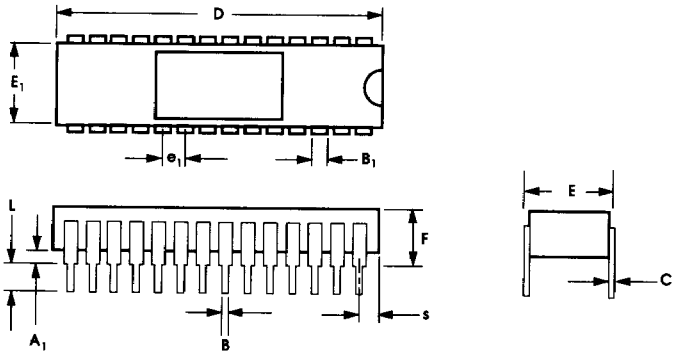
[3] If CS goes high simultaneously with WE high, the output remains in a high impedence state. CS or WE must be high during address transitions. All write timings are referenced from the last valid address to the first transitioning address. Transition is measured ±500mV from steady state voltage.

PACKAGE DIMENSIONS



28 LEAD 300 MIL PDIP

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	
B	.016	.020
B_1	.045	.055
C	.008	.012
D	1.345	1.355
E	.300	.325
E_1	.270	.290
e_1	.100	
F		.170
L	.125	.135
s	.020	.030
α	0°	15°



28 LEAD 300 MIL SIDEBRAZE DIP

	INCHES	
PARAMETER	MIN	MAX
A_1	.015	.060
B	.014	.023
B_1	.038	.065
C	.008	.015
D	1.385	1.415
E	.290	.310
E_1	.285	.305
e_1	.100	
F		.232
L	.125	.200
s		.100

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE MIN	MAX	UNIT
SSM7161-15PC	15ns	28-Pin PDIP	0	+70	°C
SSM7161-20PC	20ns				
SSM7161-25PC	25ns				
SSM7161-15SC	15ns	28-Pin PDIP			
SSM7161-20SC	20ns				
SSM7161-25SC	25ns				
SSM7161-20SB	20ns	28-Pin Sidebraze DIP	-55	+125	°C
SSM7161-25SB	25ns				
SSM7161-35SB	35ns				
SSM7162-15PC	15ns	28-Pin PDIP	0	+70	°C
SSM7162-20PC	20ns				
SSM7162-25PC	25ns				
SSM7162-15SC	15ns	28-Pin PDIP			
SSM7162-20SC	20ns				
SSM7162-25SC	25ns				
SSM7162-20SB	20ns	28-Pin Sidebraze DIP	-55	+125	°C
SSM7162-25SB	25ns				
SSM7162-35SB	35ns				

NOTE: Please contact factory regarding CERDIP, SOG and SOJ packages.