



## THIS SPEC IS OBSOLETE

Spec No: 38-05169

Spec Title: CY7C1049B 512K x 8 Static RAM

Sunset Owner: Anuj Chakrapani (AJU)

Replaced by: None

# 512K x 8 Static RAM

## Features

- **High speed**
  - $t_{AA} = 12 \text{ ns}$
- **Low active power**
  - 1320 mW (max.)
- **Low CMOS standby power (Commercial L version)**
  - 2.75 mW (max.)
- **2.0V Data Retention (400  $\mu\text{W}$  at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **Available in Pb-free and non Pb-free 36-Lead (400-Mil) Molded SOJ**

## Functional Description<sup>[1]</sup>

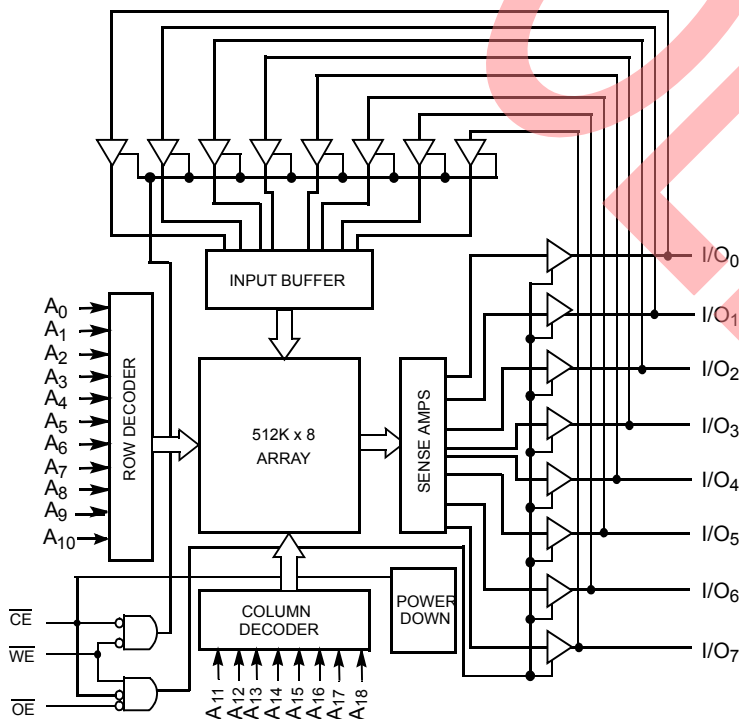
The CY7C1049B is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{\text{CE}}$ ), an active LOW Output Enable ( $\overline{\text{OE}}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1049B is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



## Pin Configuration

SOJ  
Top View

A <sub>0</sub>	1	36	NC
A <sub>1</sub>	2	35	A <sub>18</sub>
A <sub>2</sub>	3	34	A <sub>17</sub>
A <sub>3</sub>	4	33	A <sub>16</sub>
A <sub>4</sub>	5	32	A <sub>15</sub>
$\overline{\text{CE}}$	6	31	$\overline{\text{OE}}$
I/O <sub>0</sub>	7	30	I/O <sub>7</sub>
I/O <sub>1</sub>	8	29	I/O <sub>6</sub>
V <sub>CC</sub>	9	28	GND
GND	10	27	V <sub>CC</sub>
I/O <sub>2</sub>	11	26	I/O <sub>5</sub>
I/O <sub>3</sub>	12	25	I/O <sub>4</sub>
$\overline{\text{WE}}$	13	24	A <sub>14</sub>
A <sub>5</sub>	14	23	A <sub>13</sub>
A <sub>6</sub>	15	22	A <sub>12</sub>
A <sub>7</sub>	16	21	A <sub>11</sub>
A <sub>8</sub>	17	20	A <sub>10</sub>
A <sub>9</sub>	18	19	NC

### Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Selection Guide**

		-12	-15	-17
Maximum Access Time (ns)		12	15	17
Maximum Operating Current (mA)		240	220	195
Maximum CMOS Standby Current (mA)	Commercial	8	8	8
	Industrial	-	-	-
	Commercial   L	-	-	0.5

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	4.5V–5.5V
Industrial	-40°C to +85°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-12		-15		-17		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V	
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V	
$V_{IL}$	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.3	V	
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	$\mu\text{A}$	
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	-1	+1	$\mu\text{A}$	
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}$ , $f = f_{MAX} = 1/t_{RC}$		240		220		195	mA	
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		40		40		40	mA	
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$	Com'l		8		8		8	mA
			Com'l   L		-		-		0.5	mA
			Ind'l		-		-		8	mA

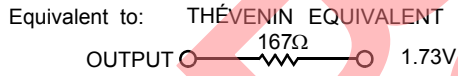
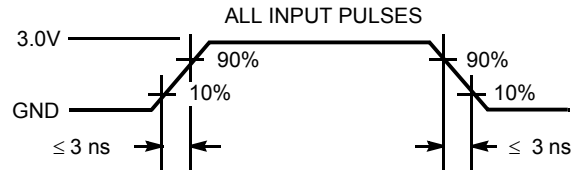
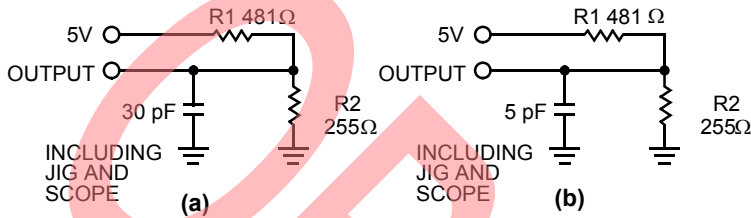
**Note:**

2. Minimum voltage is -2.0V for pulse durations of less than 20 ns.

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

**AC Test Loads and Waveforms**



**Note:**  
3. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics** Over the Operating Range<sup>[4]</sup>

Parameter	Description	-12		-15		-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
$t_{power}$	$V_{CC}$ (typical) to the First Access <sup>[5]</sup>	1		1		1		ms
$t_{RC}$	Read Cycle Time	12		15		17		ns
$t_{AA}$	Address to Data Valid		12		15		17	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		12		15		17	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		12		15		17	ns
<b>Write Cycle<sup>[8, 9]</sup></b>								
$t_{WC}$	Write Cycle Time	12		15		17		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	10		12		12		ns
$t_{AW}$	Address Set-Up to Write End	10		12		12		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		12		12		ns
$t_{SD}$	Data Set-Up to Write End	7		8		8		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		6		7		8	ns

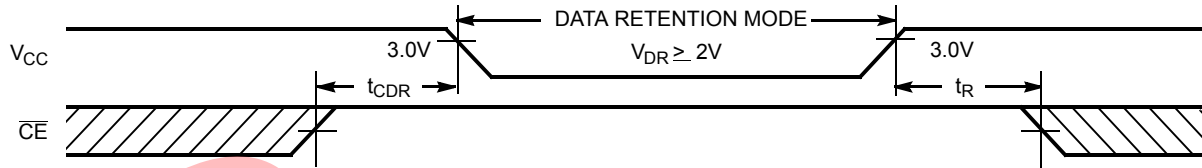
**Data Retention Characteristics** Over the Operating Range

Parameter	Description		Conditions <sup>[11]</sup>		Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention				2.0		V
$I_{CCDR}$	Data Retention Current	Com'l	L	$V_{CC} = V_{DR} = 2.0V$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	$\mu A$
$t_{CDDR}^{[3]}$	Chip Deselect to Data Retention Time				0		ns
$t_R^{[10]}$	Operation Recovery Time				$t_{RC}$		ns

**Notes:**

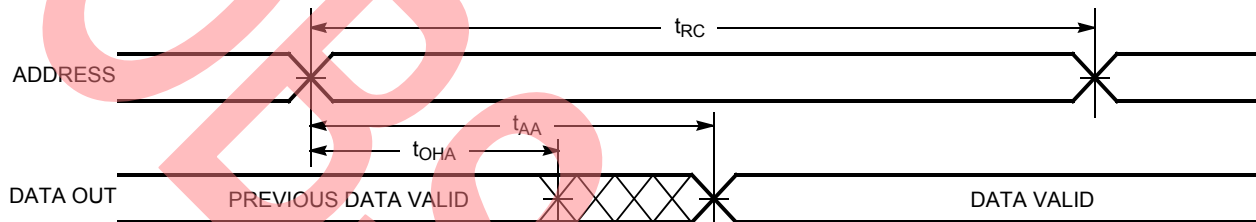
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally.  $t_{power}$  time has to be provided initially before a read/write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- $t_r \leq 3$  ns for all the speeds
- No input may exceed  $V_{CC} + 0.5V$ .

**Data Retention Waveform**

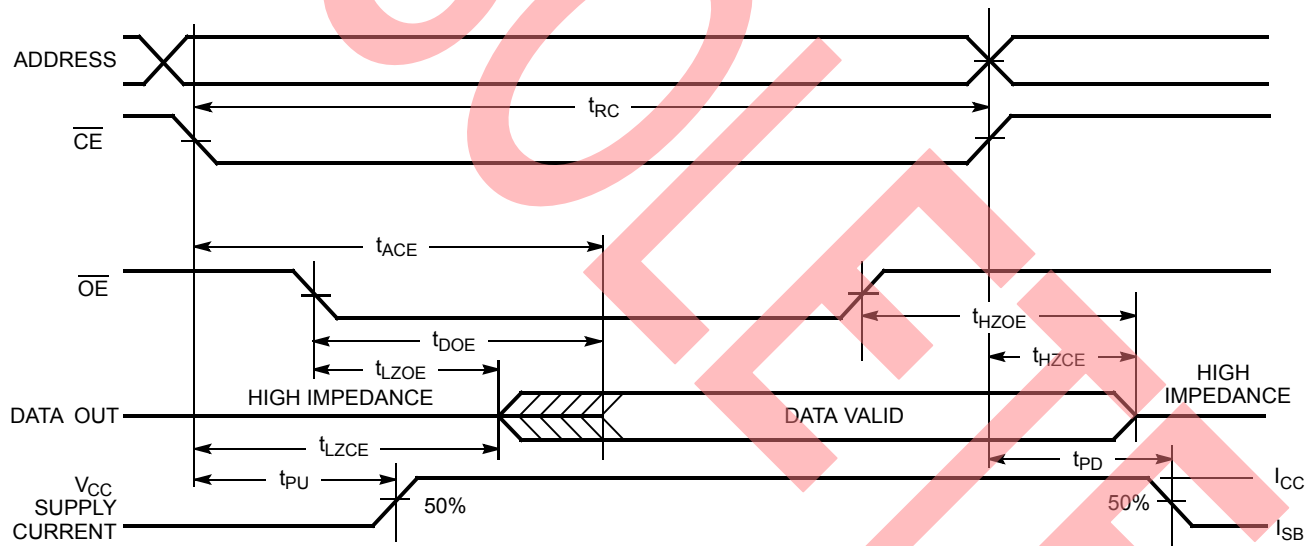


**Switching Waveforms**

**Read Cycle No. 1<sup>[12, 13]</sup>**



**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[13, 14]</sup>**

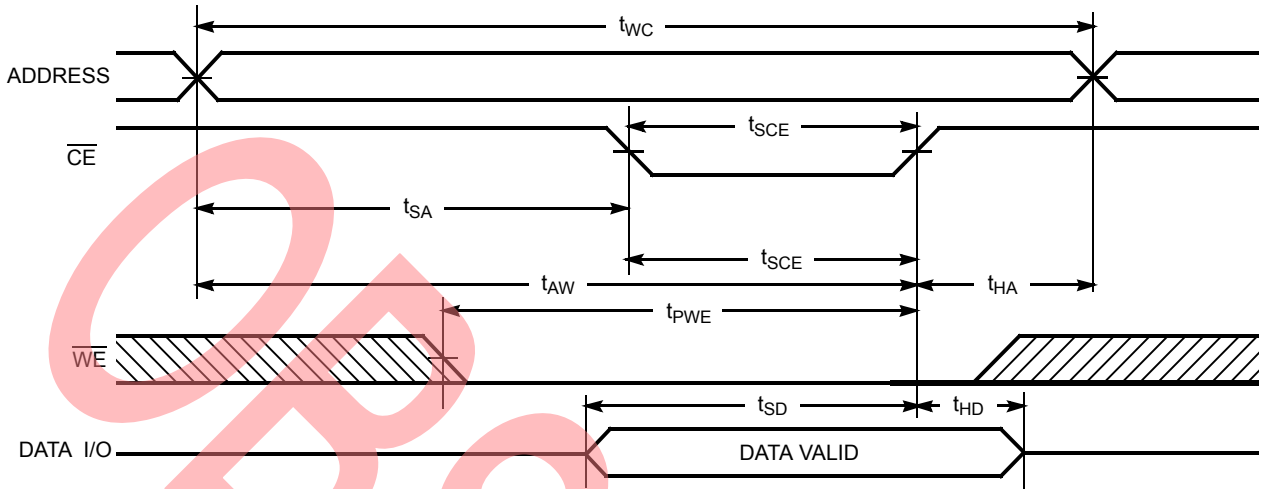


**Notes:**

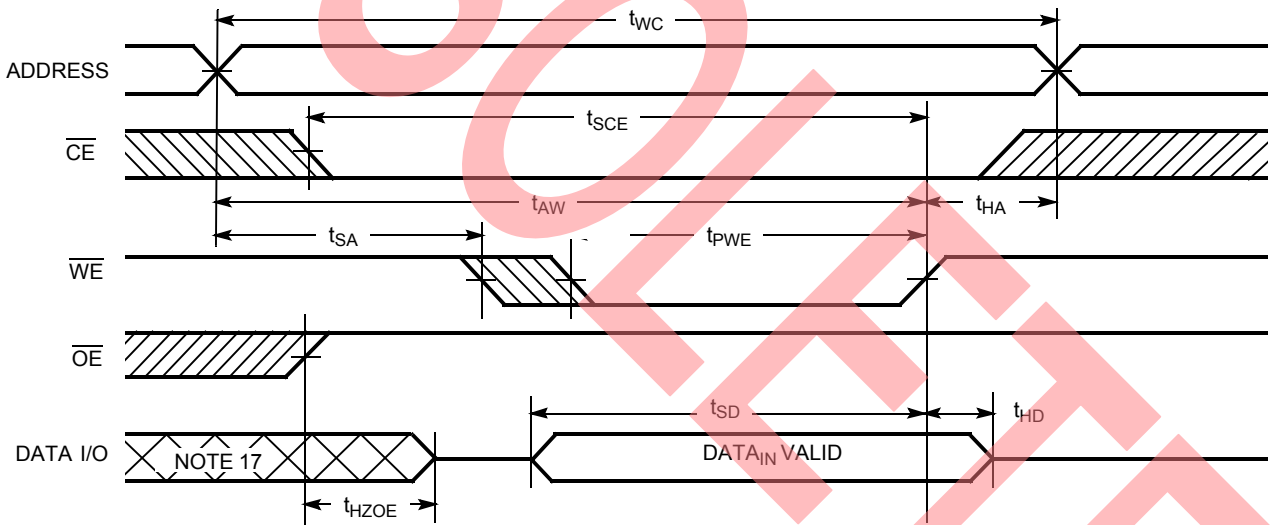
- 12. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 13.  $\overline{WE}$  is HIGH for read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[15, 16]</sup>



Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write)<sup>[15, 16]</sup>

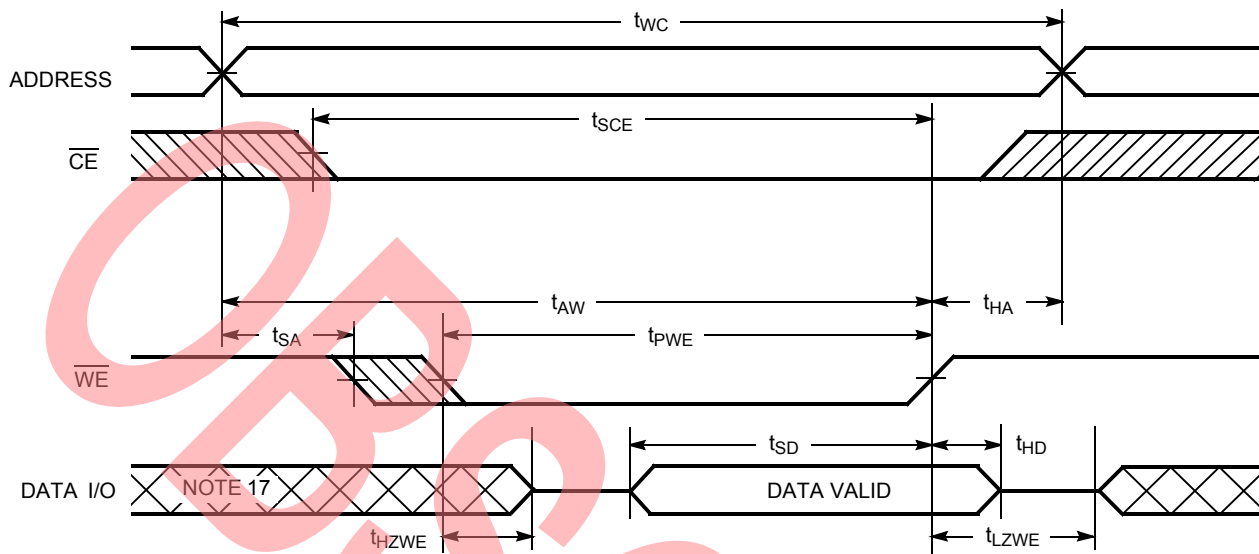


Notes:

- 15. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
- 16. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
- 17. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16]</sup>



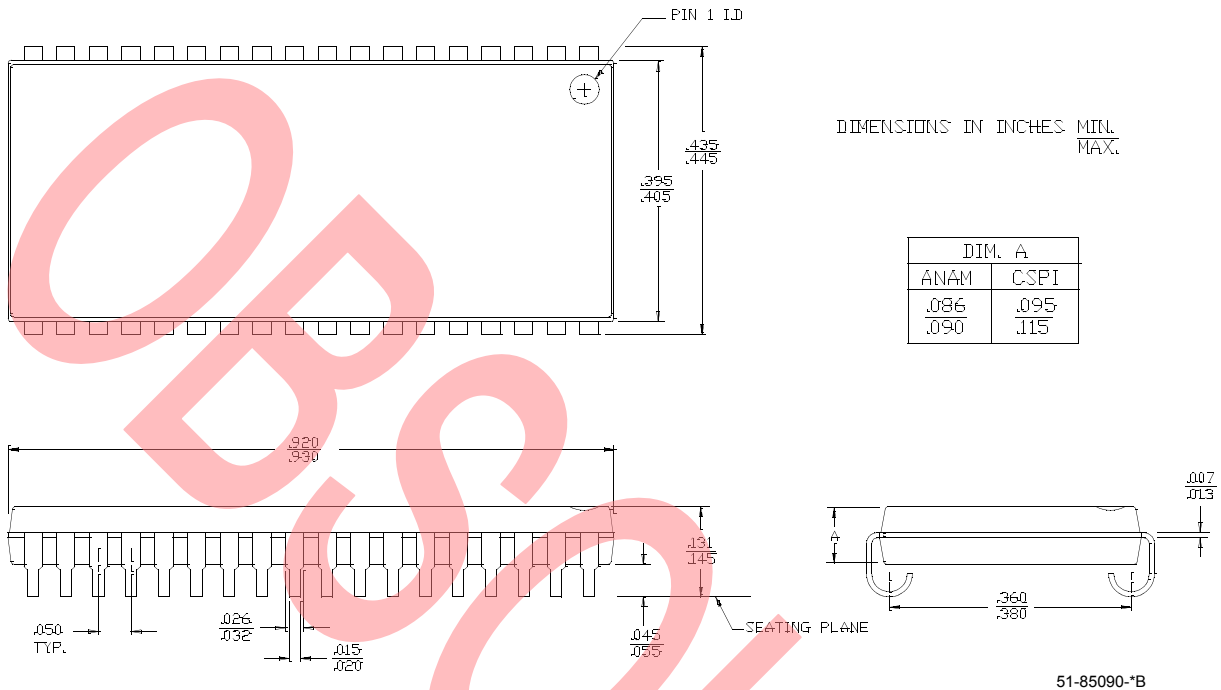
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1049B-12VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049B-12VXC		36-Lead (400-Mil) Molded SOJ (Pb-free)	
15	CY7C1049B-15VC		36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049B-15VXC		36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049B-15VI		36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049B-15VXI		36-Lead (400-Mil) Molded SOJ (Pb-free)	
17	CY7C1049BL-17VC	36-Lead (400-Mil) Molded SOJ	Commercial	



Package Diagram

36-lead (400-Mil) Molded SOJ (51-85090)



**Document History Page**

Document Title: CY7C1049B 512K x 8 Static RAM Document Number: 38-05169				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	110209	12/02/01	SZV	Change from Spec number: 38-00937 to 38-05169
*A	116465	09/16/02	CEA	Add applications foot note to data sheet, page 1
*B	498501	See ECN	NXR	Removed 20 ns and 25 ns speed bin Changed the description of I <sub>LX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*C	2895678	03/19/2010	AJU	Inactive parts; Obsolete data sheet

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