



HCT/SC245

Octal Bus Transceivers with 3-State Outputs

Product Summary

Device Parameter	Outputs	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
Octal Bus Transceiver	Non-inverting	74HCT245	74SC245	54HCT245
Operating temperature range (°C)		-40 to +85	-40 to +85	-55 to +125
Recommended operating voltage (V)		4.75 to 5.25	4.75 to 5.25	4.50 to 5.50
Maximum gate propagation delay (ns)		20	30	30

Features

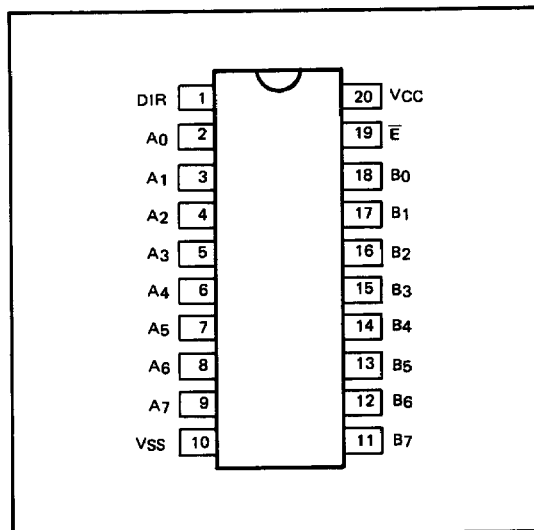
- Pin and function compatible to 54/74LS245
- Typical DC operating supply current: 10 μ A
- Typical propagation delay (port-to-port):
16ns (74HCT series)
22ns (SC series)
- Typical enable/disable time: 24 ns
- Fan out of 30 LSTTL loads.
- Input hysteresis to improve noise margins
- Fully TTL and CMOS compatible
- 3-State outputs drive bus directly
- 40°C to +85°C operating temperature range
- High speed silicon-gate CMOS technology
- Capable of operating over 3-volt to 6-volt range
- Ideal for interfacing with microprocessors
- MIL STD 883B Screening/Leadless chip carrier available.

General Description

The 245 series of Octal Bus Transceiver circuits are designed for high speed asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

Each device allows data transmission between buses depending on the logic level at the direction (DIR) input. The enable (\bar{E}) input can be used to disable the device so that the buses are effectively isolated.

Pin Configuration



Absolute Maximum Ratings

Rating	Value
Supply voltage, VCC	-0.5V to +7.0V
Input voltage, VI	-0.3V to VCC+0.3V
Short circuit output current, ISC (not more than 1 output for 1 second)	±100mA
Operating temperature range, TA 74HCT, 74SC (commercial) 54HCT (military)	-40°C to +85°C -55°C to +125°C
Storage temperature, TS	-65°C to +150°C
Power dissipation, PD	500mW

Recommended Operating Conditions

Symbol	Parameter	54 HCT			74HCT/74SC			Unit	Conditions
		min	typ	max	min	typ	max		
VCC	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V	
VI	Input voltage	0		VCC	0		VCC	V	
TA	Operating free-air temperature	-55		125	-40		+85	°C	
VCCF	Functional operating VCC range	3.00		6.00	3.00		6.00	V	

Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter	54HCT			74HCT/74SC			Unit	Conditions
		min	typ	max	min	typ	max		
V _{IH}	High-level input voltage	2.0			2.0			V	
V _{IL}	Low-level input voltage			0.8			0.8		
	Hysteresis, A or B input (V _{T+} - V _{T-})		0.3			0.3			VCC = min
V _{OH}	High-level output voltage	2.4			2.4			V	VCC = min, I _{OH} = -10mA V _{IL} = 0.8V, V _{IH} = 2V
V _{OL}	Low-level output voltage			0.4			0.4		VCC = min, I _{OL} = 12mA V _{IL} = 0.8V, V _{IH} = 2V
I _{OZH}	OFF-state output current, high-level voltage applied			20			20	μA	VCC = max, \bar{E} at 2V, V _O = 2.7V V _{IL} = 0.8V, V _{IH} = 2V
I _{OZL}	OFF-state output current, low-level voltage applied			-20			-20		VCC = max, \bar{E} at 2V, V _O = 0.4V V _{IL} = 0.8V, V _{IH} = 2V
I _I	Input current			5			1	μA	VCC = max, V _I = VCC
I _{CC}	Supply current		.01	0.5		.01	0.1	mA	VCC = max, V _I = VCC or GND, outputs open

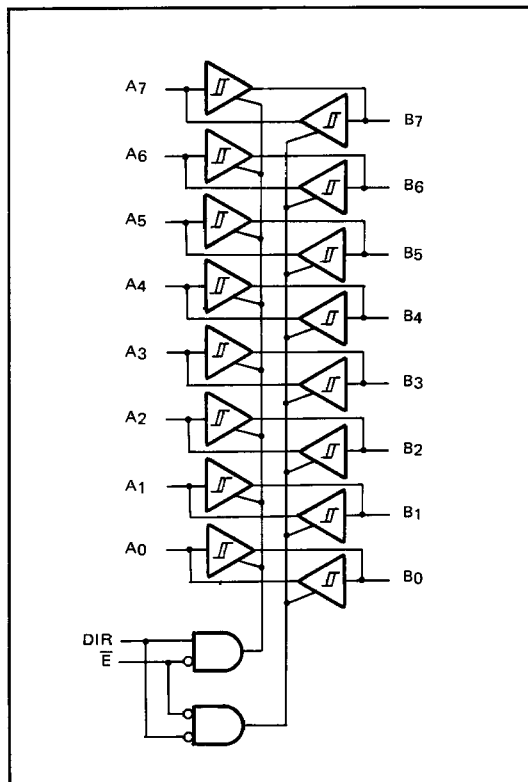
Switching Characteristics (VCC = 5V, TA = 25°C)

Symbol	Parameter	54HCT/74HCT			74SC			Unit	Conditions
		min	typ	max	min	typ	max		
tPLH	Propagation delay time, low-to-high-level output		16	20		22	30	ns	CL = 50pF, RL = 1KΩ
tPHL	Propagation delay time, high-to-low-level output		16	20		22	30		
tPZL	Output enable time to low-level		24	40		24	40	ns	CL = 50pF, RL = 1KΩ
tPZH	Output enable time from high-level		24	40		24	40		
tPLZ	Output disable time from low-level		24	40		24	40	ns	CL = 50pF, RL = 1KΩ
tPHZ	Output disable time from high-level		24	40		24	40		
CI	Input Capacitance		8			8		pF	

Ordering Information

Package	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
20-pin plastic DIP	74HCT245P	74SC245P	N/A
20-pin CERDIP	74HCT245D	74SC245D	54HCT245D
20-pin ceramic side-brazed DIP	74HCT245C	74SC245C	54HCT245C

Functional Block Diagram



Function Table

Enable (\bar{E})	Direction (DIR)	Operation
L	L	B → A
L	H	A → B
H	X	Hi-Z

NOTE: See Switching Wave Forms and Test Circuit at end of this section.