CY7B164
CY7B166

CYPRESS SEMICONDUCTOR

16K x 4 Static R/W RAM

Features

- **Ultra high speed**
  - **— t_{AA} = 8 ns**
- **Low active power**
  - **— 700 mW**
- **Low standby power**
  - **— 250 mW**
- **BiCMOS for optimum speed/power**
- **Output enable ($\overline{OE}$) feature (7B166)**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

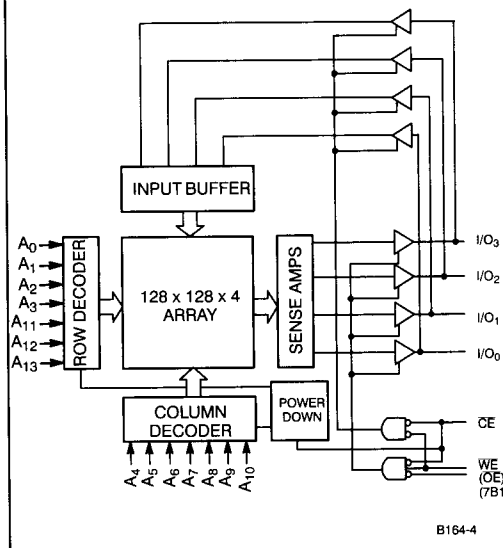
The CY7B164 and CY7B166 are high-performance BiCMOS static RAMs organized as 16,384 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7B166 has an active LOW output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7B166) while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW (or output enable ($\overline{OE}$) is HIGH for 7B166).

Logic Block Diagram



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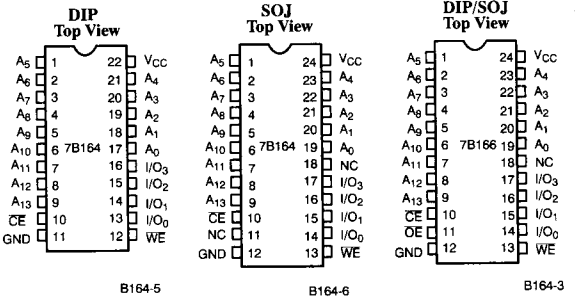
Pin Configurations



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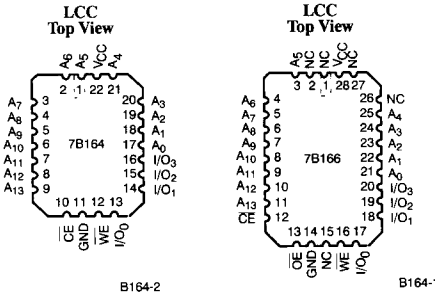

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Selection Guide

		7B164–8 7B166–8	7B164–10 7B166–10	7B164–12 7B166–12	7B164–15 7B166–15
Maximum Access Time (ns)		8	10	12	15
Maximum Operating Current (mA)	Commercial	140	130	120	
	Military		145	140	135
Maximum Operating Current (mA)	Commercial	50	40	40	
	Military		60	55	50

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to + 150°C

Ambient Temperature with Power Applied ..... − 55°C to + 125°C

Supply Voltage to Ground Potential ..... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to + 7.0V

DC Input Voltage[1] ..... − 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	
Commercial	0°C to + 70°C	− 8	5V ±5%
		−10, −12	5V ±10%
Military[2]	− 55°C to + 125°C	5V ±10%	

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions			7B164−8 7B166−8 Min.	7B164−8 7B166−8 Max.	7B164−10 7B166−10 Min.	7B164−10 7B166−10 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil					
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		Com'l		140		130	mA
				Mil				145	
I_{SB}	$\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3V, I_{OUT} = 0 mA Other Inputs ≤ 0.8V or >3V, V_{CC} = Max.		Com'l		50		40	mA
				Mil				60	

Parameters	Description	Test Conditions			7B164−12 7B166−12 Min.	7B164−12 7B166−12 Max.	7B164−15 7B166−15 Min.	7B164−15 7B166−15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = − 2.0 mA	Mil					
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		Com'l		120			mA
				Mil		140		135	
I_{SB}	$\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ 3V, I_{OUT} = 0 mA Other Inputs ≤ 0.8V or >3V, V_{CC} = Max.		Com'l		40			mA
				Mil		55		50	

Shaded area contains preliminary information.

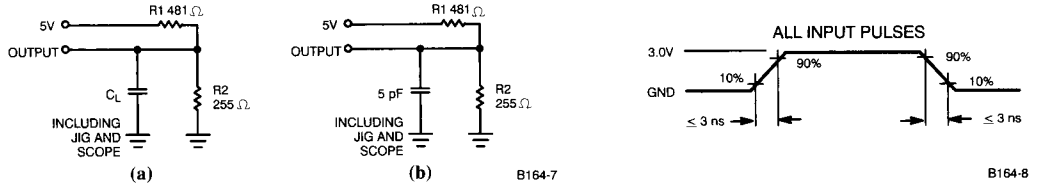
Notes:

1. V_{IL} (min.) = −3.0V for pulse width <20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.

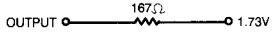
Capacitance[4]

Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		6	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

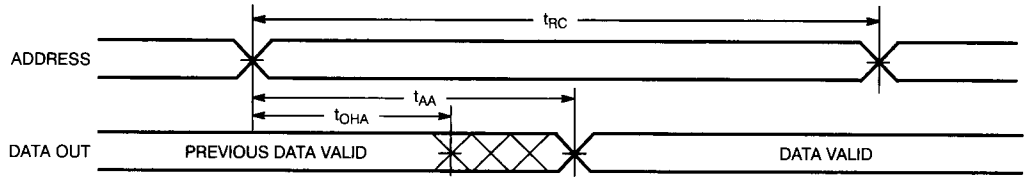
Parameters	Description		7B164–8 7B166–8 Min.	7B164–8 7B166–8 Max.	7B164–10 7B166–10 Min.	7B164–10 7B166–10 Max.	7B164–12 7B166–12 Min.	7B164–12 7B166–12 Max.	7B164–15 7B166–15 Min.	7B164–15 7B166–15 Max.	Units
READ CYCLE											
t_{RC}	Read Cycle Time		8		10		12		15		ns
t_{AA}	Address to Data Valid			8		10		12		15	ns
t_{OHA}	Output Hold from Address Change		2.5		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7B166		4.2		5		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7B166	1.5		2		2		2		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]	7B166		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]		2		2		2		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]			4		5		6		7	ns
WRITE CYCLE[9]											
t_{WC}	Write Cycle Time		8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		7		8		8		10		ns
t_{AW}	Address Set-Up to Write End		7		8		8		10		ns
t_{HA}	Address Hold from Write End		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		6.5		8		8		10		ns
t_{SD}	Data Set-Up to Write End		4		5		6		7		ns
t_{HD}	Data Hold from Write End		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z		2		2		2		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]			4	0	5	0	6	0	7	ns

Notes:

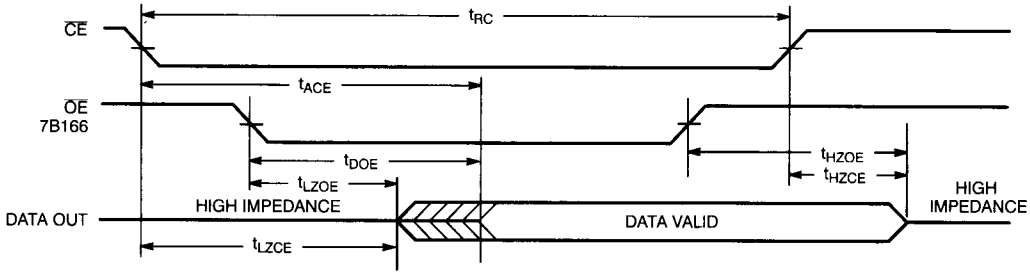
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except cerDIP (D10, D14), which has maximums of C_{IN} = 9.5 pF, C_{OUT} = 8 pF.
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.
7. t_{HZCE}, t_{HZWE}, and t_{HZOE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±200 mV from steady state voltage. This parameter is guaranteed and not 100% tested.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

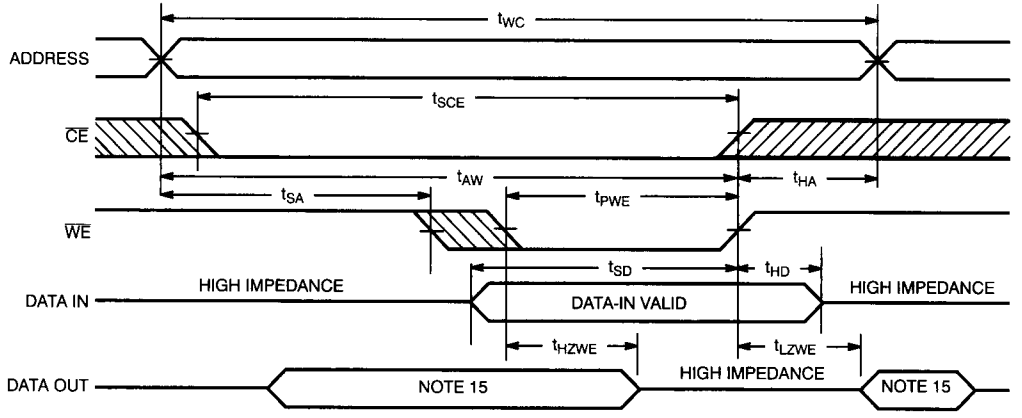
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



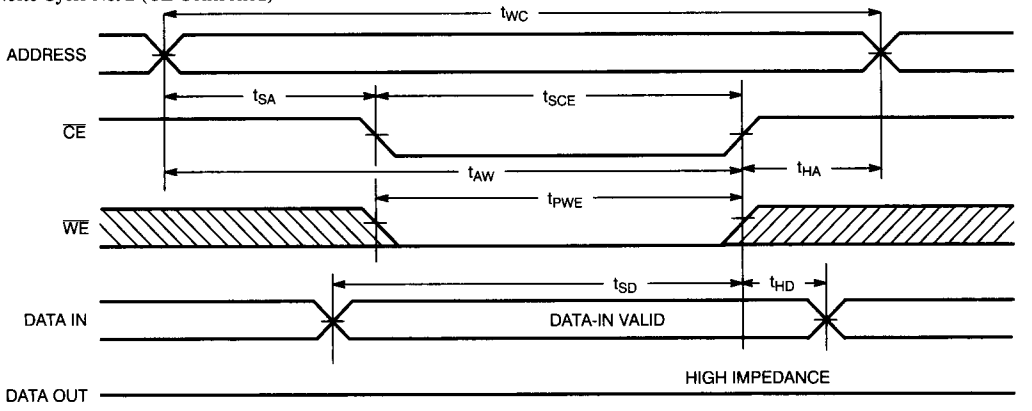
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13, 14]



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL}. (7B166: $\overline{OE}$ = V_{IL} also).
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. 7B166 only: Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period the I/O pins are in the output state, and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 13, 14, 16]



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Note:
16. If the $\overline{CE}$ LOW transition occurs after the WE transition, the output remains in a high-impedance state.

7B164 Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7B166 Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B164–8VC	V13	32-Lead (400-Mil) Molded SOJ	Commercial
10	CY7B164–10DC	D10	22-Lead (300-Mil) CerDIP	Commercial
	CY7B164–10PC	P9	22-Lead (300-Mil) Molded DIP	
	CY7B164–10VC	V13	32-Lead (400-Mil) Molded SOJ	
	CY7B164–10DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7B164–10LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
12	CY7B164–12DC	D10	22-Lead (300-Mil) CerDIP	Commercial
	CY7B164–12PC	P9	22-Lead (300-Mil) Molded DIP	
	CY7B164–12VC	V13	32-Lead (400-Mil) Molded SOJ	
	CY7B164–12DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7B164–12LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
15	CY7B164–15DMB	D10	22-Lead (300-Mil) CerDIP	Military
	CY7B164–15LMB	L52	22-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7B166–8VC	V13	24-Lead Molded SOJ	Commercial
10	CY7B166–10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B166–10PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B166–10VC	V13	24-Lead Molded SOJ	
	CY7B166–10DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7B166–10LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
12	CY7B166–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B166–12PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B166–12VC	V13	24-Lead Molded SOJ	
	CY7B166–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7B166–12LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
15	CY7B166–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7B166–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

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Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}[17]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
17. 7B166 only.