

# P54/74FCT646/A/C (P54/74PCT646/A/C) P54/74FCT648/A/C (P54/74PCT648/A/C) OCTAL TRANSCEIVER/REGISTER



## FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-C speed at 5.4ns max. (Com'I)  
FCT-A speed at 6.3ns max. (Com'I)
- CMOS  $V_{OH}$  Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'I), 48 mA (MII)  
15 mA Source Current (Com'I), 12 mA (MII)
- Independent Register for A and B Buses
- Choice of Non-Inverting and Inverting Data Paths
- Multiplexed Real-Time and Stored Data
- 3-State Output
- Manufactured in 0.8 micron PACE Technology™



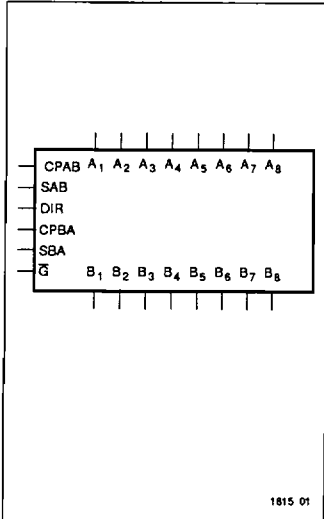
## DESCRIPTION

The 'FCT646 and 'FCT648 consist of a bus transceiver circuit with 3-state, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control  $\bar{G}$  and direction pins are provided to control the transceiver function.

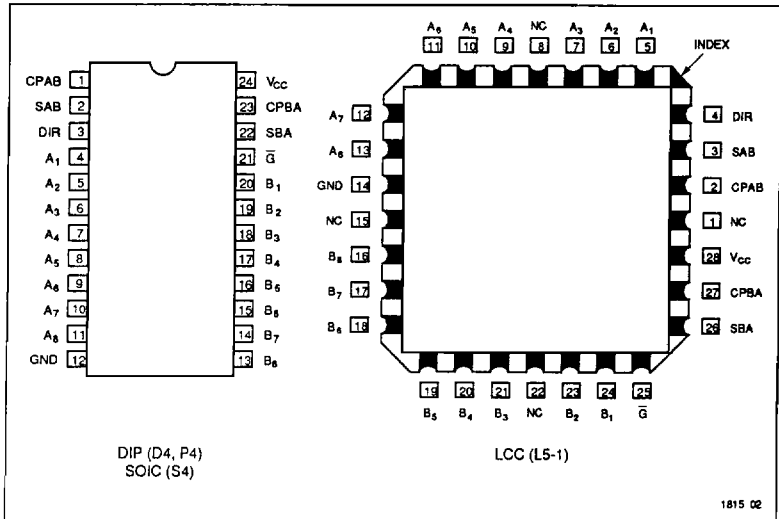
In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\bar{G}$  is Active LOW. In the isolation mode (enable Control  $\bar{G}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.



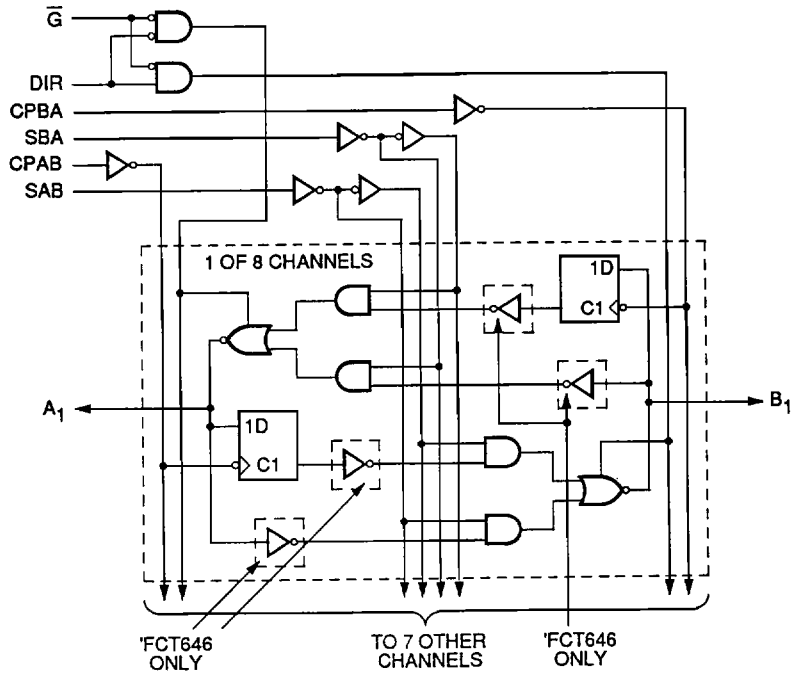
## LOGIC SYMBOL



## PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



1815 03

**ABSOLUTE MAXIMUM RATINGS<sup>1,2</sup>**

Symbol	Parameter	Value	Unit
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>A</sub>	Ambient Temperature Under Bias	-65 to +135	°C
V <sub>CC</sub>	V <sub>CC</sub> Potential to Ground	-0.5 to +7.0	V
I <sub>IN</sub>	Input Current	-30 to +5.0	mA

**Notes:** 1815 Tbl 01  
 1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I <sub>OUTPUT</sub>	Current Applied to Output	120	mA
V <sub>IN</sub>	Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	Voltage Applied to Output	-0.5 to V <sub>CC</sub> + 0.5	V

1815 Tbl 02  
 2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

**RECOMMENDED OPERATING CONDITIONS**

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V <sub>CC</sub> )	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions)

Symbol	Parameter	Min	Typ <sup>1</sup>	Max	Units	V <sub>CC</sub>	Conditions	
V <sub>IH</sub>	Input HIGH Voltage	2.0			V			
V <sub>IL</sub>	Input LOW Voltage			0.8	V			
V <sub>H</sub>	Hysteresis		0.35		V		All inputs	
V <sub>CD</sub>	Input Clamp Diode Voltage		-0.7	-1.2	V	MIN	I <sub>IN</sub> = -18mA	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = 0.2V, or V <sub>CC</sub> - 0.2V		V <sub>CC</sub> - 0.2	V <sub>CC</sub>	V	I <sub>OH</sub> = -32µA	
		Military/Commercial (CMOS)	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	V	MIN	I <sub>OH</sub> = -300µA	
		Military (TTL)	2.4		V	MIN	I <sub>OH</sub> = -12mA	
		Commercial (TTL)	2.4		V	MIN	I <sub>OH</sub> = -15mA	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = 0.2V, or V <sub>CC</sub> - 0.2V			GND	0.2	V	I <sub>OL</sub> = 300µA
		Military/Commercial (CMOS)		GND	0.2	V	MIN	I <sub>OL</sub> = 300µA
		Military (TTL)		0.3	0.55	V	MIN	I <sub>OL</sub> = 48mA
		Commercial (TTL)		0.3	0.55	V	MIN	I <sub>OL</sub> = 64mA
I <sub>IH</sub>	Input HIGH Current (Except I/O Pins)			5	µA	MAX	V <sub>IN</sub> = V <sub>CC</sub>	
I <sub>IL</sub>	Input LOW Current (Except I/O Pins)			-5	µA	MAX	V <sub>IN</sub> = GND	
I <sub>IH</sub>	Input HIGH Current <sup>3</sup> (Except I/O Pins)			5	µA	MAX	V <sub>IN</sub> = 2.7V	
I <sub>IL</sub>	Input LOW Current <sup>3</sup> (Except I/O Pins)			-5	µA	MAX	V <sub>IN</sub> = 0.5V	
I <sub>IH</sub>	Input HIGH Current (I/O Pins only)			15	µA	MAX	V <sub>IN</sub> = V <sub>CC</sub>	
I <sub>IL</sub>	Input LOW Current (I/O Pins only)			-15	µA	MAX	V <sub>IN</sub> = GND	
I <sub>IH</sub>	Input HIGH Current <sup>3</sup> (I/O Pins only)			15	µA	MAX	V <sub>IN</sub> = 2.7V	
I <sub>IL</sub>	Input LOW Current <sup>3</sup> (I/O Pins only)			-15	µA	MAX	V <sub>IN</sub> = 0.5V	
I <sub>OS</sub>	Output Short Circuit Current <sup>2</sup>	-60	-120		mA	MAX	V <sub>OUT</sub> = 0.0V	
C <sub>IN</sub>	Input Capacitance <sup>3</sup>		5	10	pF		All inputs	
C <sub>OUT</sub>	Output Capacitance <sup>3</sup>		9	12	pF		All outputs	

**Notes:** 1815 Tbl 05  
 1. Typical limits are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = +25°C ambient.  
 2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.  
 3. This parameter is guaranteed but not tested.



**DC CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ <sup>1</sup>	Max	Units	Conditions
$I_{CC}$	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	$V_{CC} = \text{MAX}$ , $f_1 = 0$ , Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	$V_{CC} = \text{MAX}$ , Outputs Open, $f_1 = 0$ , $V_{IN} = 3.4V$
$I_{CCD}$	Dynamic Power Supply Current <sup>3</sup>	0.15	0.25	mA/ MHz	$V_{CC} = \text{MAX}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $\bar{G} = \text{GND}$ , and $\text{DIR} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
$I_C$	Total Power Supply Current <sup>5</sup>	1.7	4.0	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$ , 50% Duty Cycle, $\bar{G} = \text{GND}$ , $\text{DIR} = \text{GND}$ , $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$ , 50% Duty Cycle, $\bar{G} = \text{GND}$ , $\text{DIR} = \text{GND}$ , $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		7.0	12.8 <sup>4</sup>	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling, $\text{DIR} = \text{GND}$ , $\bar{G} = \text{GND}$ , $f_1 = 5\text{MHz}$ , 50% Duty Cycle, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8 <sup>4</sup>	mA	$V_{CC} = \text{MAX}$ , $f_0 = 10\text{MHz}$ , 50% Duty Cycle, Outputs Open, Eight Bits Toggling, $\text{DIR} = \text{GND}$ $\bar{G} = \text{GND}$ , $f_1 = 5\text{MHz}$ , 50% Duty Cycle, $V_{IN} = 3.4V$ , $V_{IN} = \text{GND}$

**Notes:**

- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient and maximum loading.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} \cdot D_H \cdot N_T + I_{CCD} (f_0/2 + f_1 \cdot N_1)$$

$$I_{CC} = \text{Quiescent Current with CMOS input levels}$$

- $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )
  - $D_H$  = Duty Cycle for TTL Inputs High
  - $N_T$  = Number of TTL Inputs at  $D_H$
  - $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
  - $f_0$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)
  - $f_1$  = Input Frequency
  - $N_1$  = Number of Inputs at  $f_1$
- All currents are in milliamps and all frequencies are in megahertz.

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### FUNCTION TABLE

Inputs						Data I/O <sup>1</sup>		Operation or Function			
$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>1</sub> thru A <sub>8</sub>	B <sub>1</sub> thru B <sub>8</sub>	'FCT646		'FCT648	
H	X	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data		Isolation Store A and B Data	
H	X	$\downarrow$	$\downarrow$	X	X						
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus		Real Time $\bar{B}$ Data to A Bus	
L	L	X	H or L	X	H			Stored B Data to A Bus		Stored $\bar{B}$ Data to A Bus	
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus		Real Time $\bar{A}$ Data to B Bus	
L	H	H or L	X	H	X			Stored A Data to B Bus		Stored $\bar{A}$ Data to B Bus	

**Notes:**  
 1. The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.  
 2. H = HIGH, L = LOW, X = Don't Care,  $\downarrow$  = LOW-to-HIGH Transition

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### AC CHARACTERISTICS

Symbol	Parameter	'FCT646/648				'FCT646A/648A				'FCT646C/648C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Bus to Bus	2.0	9.0	2.0	8.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 3
$t_{PZH}$ $t_{PZL}$	Output Enable Time Enable to Bus and DIR to A or B	2.0	10.5	2.0	8.5	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time Enable to Bus and Direction to Bus	2.0	10.5	2.0	8.5	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 7, 8
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay SBA or SAB to A or B	2.0	11.0	2.0	9.5	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 5

**Note:**  
 1. AC Characteristics guaranteed with  $C_L = 50\text{pF}$  as shown in Figure 1.

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### AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT646/648				'FCT646A/648A				'FCT646C/648C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	-	4.0	-	2.0	-	2.0	-	2.0	-	2.0	-	ns	4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	-	2.0	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW	6.0	-	6.0	-	5.0	-	5.0	-	5.0	-	5.0	-	ns	5

**Note:**  
 1. Minimum limits are guaranteed but not tested on Propagation Delays.

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### ORDERING INFORMATION

<u>PxxFCT</u> Temp. Class	<u>xxxx</u> Device type	<u>xx</u> Package	<u>x</u> Processing	
				Blank Commercial
				M Military Temperature
				MB MIL-STD-883, Class B
				P Plastic DIP
				D CERDIP
				SO Small Outline IC
				L Leadless Chip Carrier
				646 Non-inverting Octal Transceiver/Register
				646A Fast Non-inverting Octal Transceiver/Register
				646C Ultra Fast Non-inverting Octal Transceiver/Register
				648 Inverting Octal Transceiver/Register
				648A Fast Inverting Octal Transceiver/Register
				648C Ultra Fast Inverting Octal Transceiver/Register
				74 Commercial
				54 Military

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