DATA SHEET

74LVC162245A; 74LVCH162245A

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

Product specification
Supersedes data of 1998 Feb 17

2003 Dec 08

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FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Integrated 30 Ω termination resistors
- High-impedance when V_{CC} = 0 V
- All data inputs have bushold (74LVCH162245A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC(H)162245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC(H)162245A is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74LVC(H)162245A features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH162245A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

The 74LVC(H)162245A is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nAn to nBn; nBn to nAn	C_L = 50 pF; V_{CC} = 3.3 V	3.3	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; notes 1 and 2	28	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC162245ADL	–40 to +125 °C	48	SSOP48	plastic	SOT370-1
74LVCH162245ADL	–40 to +125 °C	48	SSOP48	plastic	SOT370-1
74LVC162245ADGG	–40 to +125 °C	48	TSSOP48	plastic	SOT362-1
74LVCH162245ADGG	–40 to +125 °C	48	TSSOP48	plastic	SOT362-1

PINNING

SYMBOL	PIN	DESCRIPTION
1DIR	1	direction control input
n.c.	–	not connected
1B0	2	data input/output
1B1	3	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
1B2	5	data input/output
1B3	6	data input/output
V_{CC}	7, 18, 31, 42	supply voltage
1B4	8	data input/output
1B5	9	data input/output
1B6	11	data input/output
1B7	12	data input/output
2B0	13	data input/output
2B1	14	data input/output
2B2	16	data input/output
2B3	17	data input/output
2B4	19	data input/output
2B5	20	data input/output
2B6	22	data input/output
2B7	23	data input/output
2DIR	24	direction control input
$2\overline{OE}$	25	output enable input (active LOW)
2A7	26	data input/output
2A6	27	data input/output
2A5	29	data input/output
2A4	30	data input/output
2A3	32	data input/output
2A2	33	data input/output
2A1	35	data input/output
2A0	36	data input/output
1A7	37	data input/output
1A6	38	data input/output
1A5	40	data input/output
1A4	41	data input/output
1A3	43	data input/output
1A2	44	data input/output
1A1	46	data input/output
1A0	47	data input/output
$1\overline{OE}$	48	output enable input (active LOW)

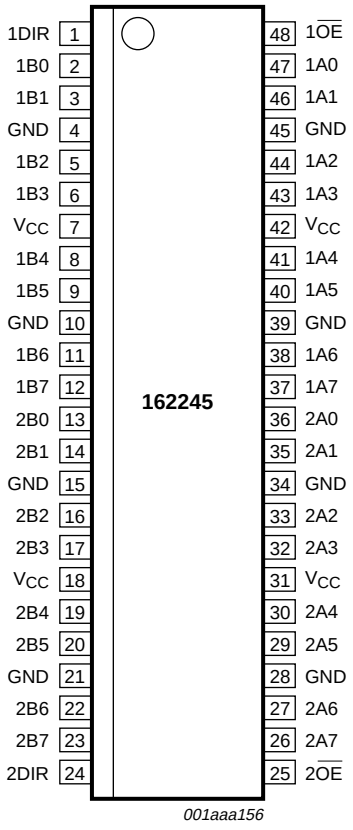


Fig.1 Pin configuration SSOP48 and TSSOP48.

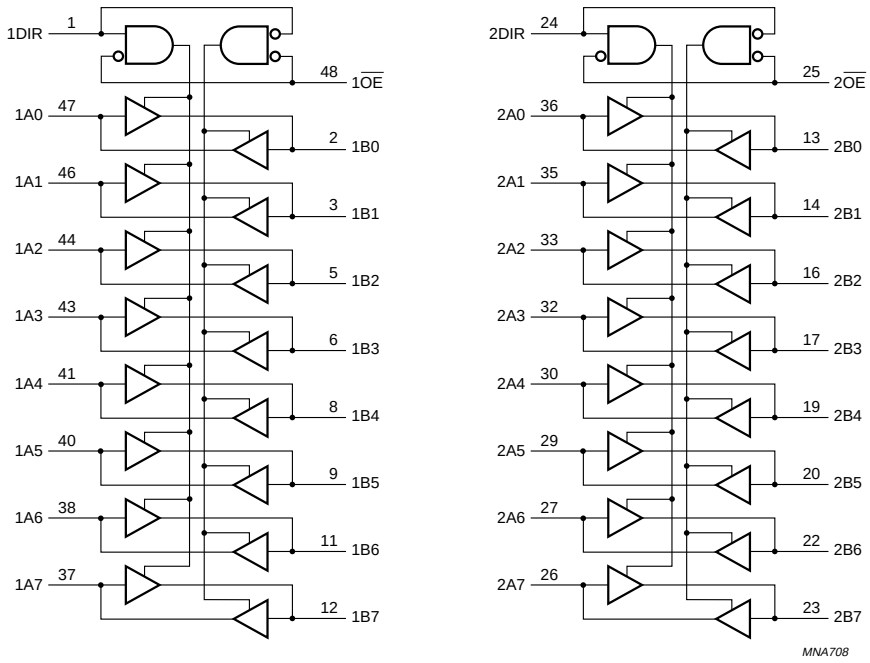


Fig.2 Logic symbol.

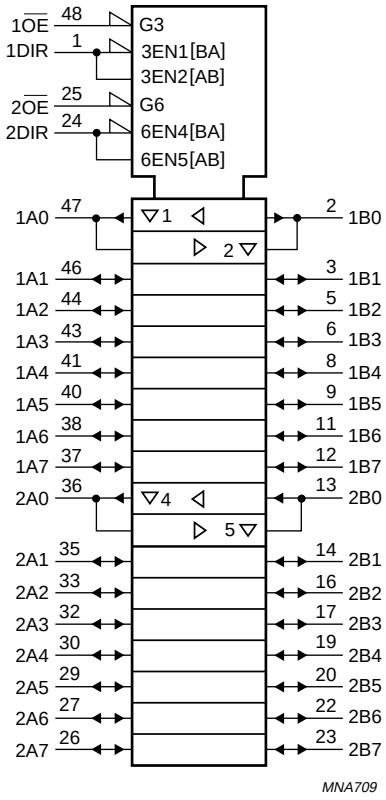


Fig.3 Logic symbol (IEEE/IEC).

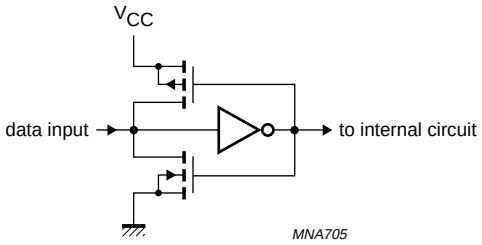


Fig.4 Bushold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	ambient temperature	in free air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		output 3-state; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 μA	2.7 to 3.6	V_{CC} – 0.2	V_{CC}	–	V
		I_O = –6 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –12 mA	3.0	V_{CC} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	0	0.20	V
		I_O = 6 mA	2.7	–	–	0.40	V
		I_O = 12 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; notes 2 and 3	3.6	–	±0.1	±5	μA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V	0.0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	0.1	20	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0	2.7 to 3.6	–	5	500	μA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 4 and 5	3.0	75	–	–	μA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 4 and 5	3.0	–75	–	–	μA
I_{BHLO}	bushold LOW overdrive current	notes 4 and 6	3.6	500	–	–	μA
I_{BHHO}	bushold HIGH overdrive current	notes 4 and 6	3.6	–500	–	–	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 μA	2.7 to 3.6	V_{CC} – 0.3	–	–	V
		I_O = –6 mA	2.7	V_{CC} – 0.65	–	–	V
		I_O = –12 mA	3.0	V_{CC} – 1	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					V
		I_O = 100 μA	2.7 to 3.6	–	–	0.3	
		I_O = 6 mA	2.7	–	–	0.6	V
		I_O = 12 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	–	±20	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; notes 2 and 3	3.6	–	–	±20	μA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V	0.0	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	–	80	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0	2.7 to 3.6	–	–	5000	μA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 4 and 5	3.0	60	–	–	μA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 4 and 5	3.0	–60	–	–	μA
I_{BHLO}	bushold LOW overdrive current	notes 4 and 6	3.6	500	–	–	μA
I_{BHHO}	bushold HIGH overdrive current	notes 4 and 6	3.6	–500	–	–	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For bushold parts, the bushold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input terminal.
3. For I/O ports the parameter I_{OZ} includes the input leakage current.
4. Valid for data inputs of bushold parts (LVCH162245A) only. For data inputs only, control inputs do not have a bushold circuit.
5. The specified sustaining current at the data input holds the input below the specified V_I level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

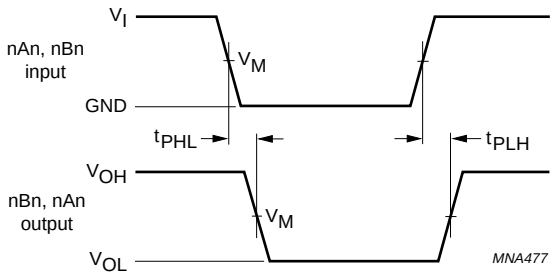
GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nAn to nBn; nBn to nAn	see Figs 5 and 7	1.2	–	12	–	ns
			2.7	1.0	4.2	6.7	ns
			3.0 to 3.6	1.0	3.3(2)	5.7	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nAn; n$\overline{OE}$ to nBn	see Figs 6 and 7	1.2	–	18	–	ns
			2.7	1.5	5.1	8.5	ns
			3.0 to 3.6	1.0	3.4(2)	7.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nAn; n$\overline{OE}$ to nBn	see Figs 6 and 7	1.2	–	10	–	ns
			2.7	1.5	3.5	7.5	ns
			3.0 to 3.6	1.5	3.3(2)	6.5	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nAn to nBn; nBn to nAn	see Figs 5 and 7	1.2	–	–	–	ns
			2.7	1.0	–	8.5	ns
			3.0 to 3.6	1.0	–	9.5	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nAn; n$\overline{OE}$ to nBn	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.5	–	7.5	ns
			3.0 to 3.6	1.0	–	9.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nAn; n$\overline{OE}$ to nBn	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.5	–	11.0	ns
			3.0 to 3.6	1.5	–	8.5	ns

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

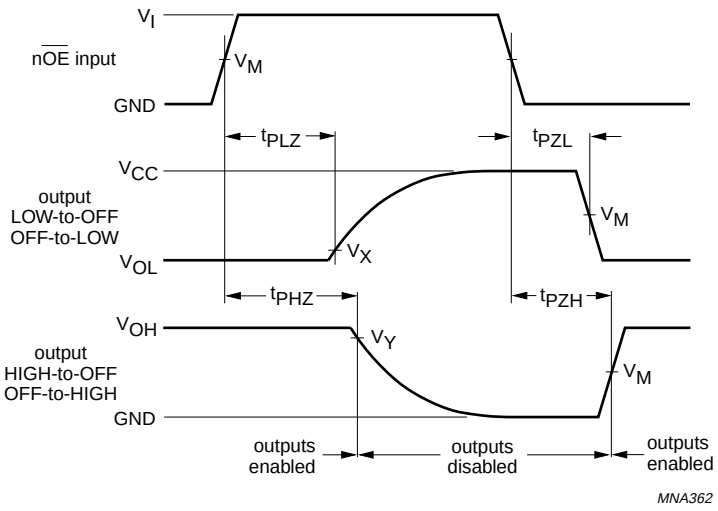
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 The input (nAn, nBn) to outputs (nBn, nAn) propagation delays.

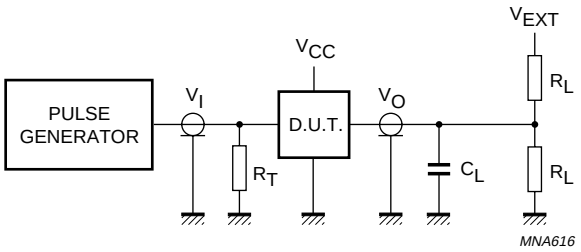


V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.1$ V at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.1$ V at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω(1)	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuits:

R_L = Load resistor.

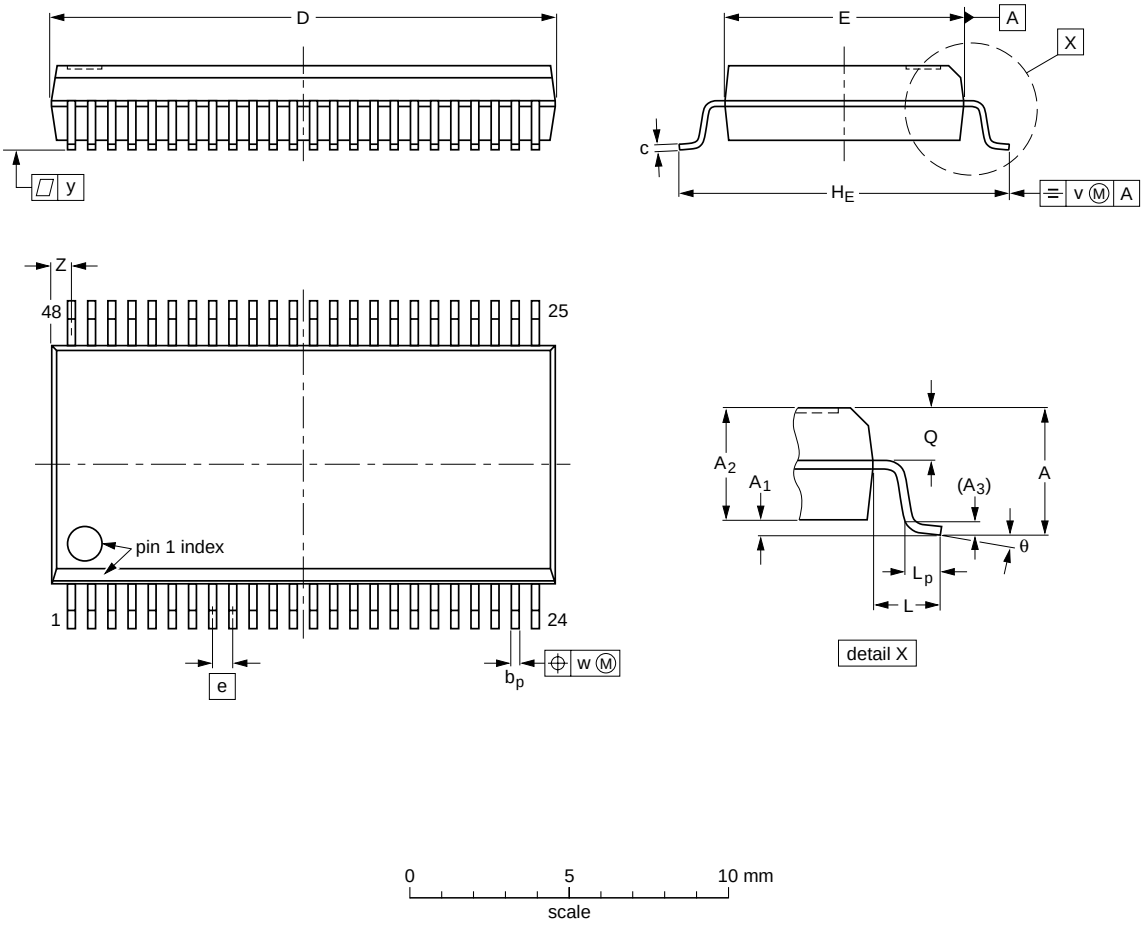
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

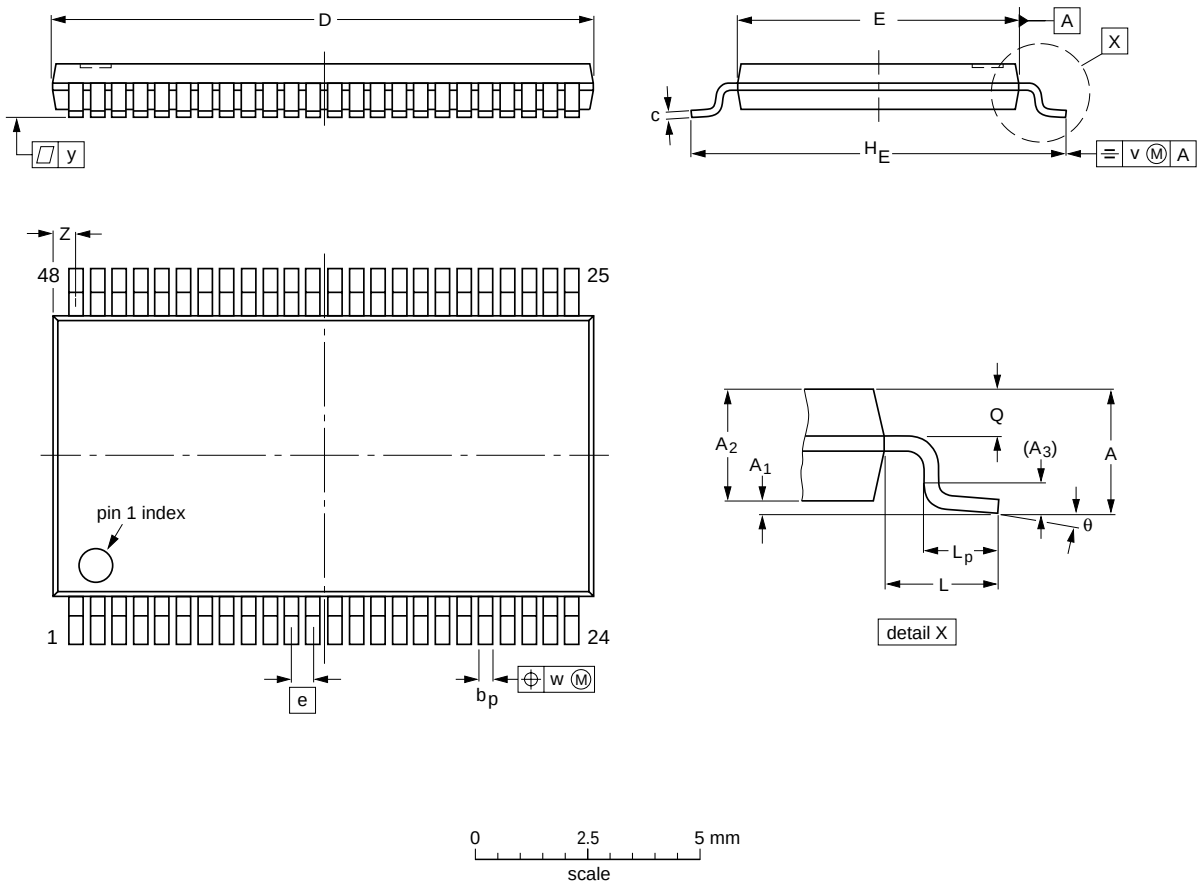
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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74LVC_LVCH162245A

Preview Product information Selection guide

Datasheet

(Product Specification)
v.5.0, 2003-12-08
Pages, 112kB

Download datasheet
Download all documentation

16-bit transceiver with direction pin, 30 Ohm series termination resistors; 5 V tolerant input/output; 3-state

General description

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The 74LVC(H)162245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC(H)162245A is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74LVC(H)162245A features two output enable (nOE) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. nOE controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH162245A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

The 74LVC(H)162245A is designed with 30 Ohm series termination resistors in both HIGH and LOW output stages to reduce line noise.

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Features and benefits

Hide

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Integrated 30 Ohm termination resistors
- High-impedance when V_{CC} =0 V
- All data inputs have bushold (74LVCH162245A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to +85 Cel and -40 to +125 Cel.

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Parametrics/similar products

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Type number	Package	Package name	Nr of pins	Family	Description	Voltage (V)	Logic switching levels	Output drive capability(mA)	t_{pd}(ns)	Power dissipation considerations
74LVC162245ADGG	SOT362-1 (TSSOP48)	TSSOP48	48	LVC	Wide supply voltage range from 1.2 to 3.6 V	1.2-3.6	TTL	+/- 12 mA	3.3@3.3V	Low Power or Battery Applications
74LVC162245ADL	SOT370-1 (SSOP48)	SSOP48	48	LVC	Wide supply voltage range from 1.2 to 3.6 V	1.2-3.6	TTL	+/- 12 mA	3.3@3.3V	Low Power or Battery Applications
74LVCH162245ADGG	SOT362-1 (TSSOP48)	TSSOP48	48	LVC	Wide supply voltage range from 1.2 to 3.6 V	1.2-3.6	TTL	+/- 12 mA	3.3@3.3V	Low Power or Battery Applications
74LVCH162245ADL	SOT370-1 (SSOP48)	SSOP48	48	LVC	Wide supply voltage range from 1.2 to 3.6 V	1.2-3.6	TTL	+/- 12 mA	3.3@3.3V	Low Power or Battery Applications

Similar products

74LVC_LVCH162245A links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

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Pricing/ordering/availability

Hide

Type number	Ordering code (12NC)	Orderable part number	Region	Distributor	In stock	Order quantity	Inventory date	Buy online	Samples
74LVC162245ADGG	9352 377 00112	74LVC162245ADGG,11	NA	DIGI-KEY CORPORATION	3,717		5/3/2011	Buy online	Order samples
			NA	FUTURE ELECTRONICS	1,866		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	1,450		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	no		4/15/2011	Buy online	
74LVC162245ADGG	9352 377 00118	74LVC162245ADGG:11	NA	AVNET ELECTRONICS MARKETING	4,000		5/3/2011	Buy online	Order samples
			ASIA	WPI	4,000	2000	05/03/2011	Buy online	

			NA	FUTURE ELECTRONICS	3,998		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	yes		4/15/2011	Buy online	
			ASIA	SACL - Hong Kong/China	yes	2000	05/01/2011	Buy online	
74LVC162245ADL	9352 376 90112	74LVC162245ADL,112	NA	AVNET ELECTRONICS MARKETING	1,561		5/3/2011	Buy online	not available
			NA	AVNET ELECTRONICS MARKETING	1,561		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	no		4/15/2011	Buy online	
74LVC162245ADL	9352 376 90118	74LVC162245ADL,118	NA	AVNET ELECTRONICS MARKETING	1,561		5/3/2011	Buy online	Order samples
			NA	MOUSER ELECTRONICS	1,090		5/3/2011	Buy online	
			NA	MOUSER ELECTRONICS	1,090		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	0		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	0		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	yes		4/15/2011	Buy online	
74LVCH162245ADGG	9352 387 30112	74LVCH162245ADGG,1	NA	MOUSER ELECTRONICS	1,905		5/3/2011	Buy online	not available
			NA	MOUSER ELECTRONICS	1,905		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	0		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	yes		4/15/2011	Buy online	
74LVCH162245ADGG	9352 387 30118	74LVCH162245ADGG:1	AS	FUTURE ELECTRONICS- ASIA	14,000		5/3/2011	Buy online	Order samples
			NA	DIGI-KEY CORPORATION	11,805		5/3/2011	Buy online	
			NA	DIGI-KEY CORPORATION	10,000		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	4,000		5/3/2011	Buy online	
			NA	FUTURE ELECTRONICS	2,450		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	yes		4/15/2011	Buy online	
74LVCH162245ADL	9352 387 20112	74LVCH162245ADL,11	NA	FUTURE ELECTRONICS	3,710		5/3/2011	Buy online	not available
			NA	MOUSER ELECTRONICS	1,752		5/3/2011	Buy online	
			NA	MOUSER ELECTRONICS	1,752		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	658		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	658		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	yes		4/15/2011	Buy online	
74LVCH162245ADL	9352 387 20118	74LVCH162245ADL:11	NA	FUTURE ELECTRONICS	3,000		5/3/2011	Buy online	Order samples
			NA	AVNET ELECTRONICS MARKETING	1,000		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	1,000		5/3/2011	Buy online	
			NA	AVNET ELECTRONICS MARKETING	658		5/3/2011	Buy online	
			NA	MOUSER ELECTRONICS	200		5/3/2011	Buy online	
			NA	MOUSER ELECTRONICS	200		5/3/2011	Buy online	
			JAPAN	CHIP ONE STOP	yes		4/15/2011	Buy online	

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Products/packages Hide

Type number	Orderable part number	Ordering code (12NC)	Product status	Package	Packing	Marking	ECCN
74LVC162245ADGG	74LVC162245ADGG,11	9352 377 00112	Volume production	SOT362-1 (TSSOP48)	Tube	Standard Marking	
74LVC162245ADGG	74LVC162245ADGG:11	9352 377 00118	Volume production	SOT362-1 (TSSOP48)	Reel Pack, SMD, 13"	Standard Marking	
74LVC162245ADL	74LVC162245ADL,112	9352 376 90112	Volume production	SOT370-1 (SSOP48)	Tube	Standard Marking	
74LVC162245ADL	74LVC162245ADL,118	9352 376 90118	Volume production	SOT370-1 (SSOP48)	Tape reel smd	Standard Marking	
74LVCH162245ADGG	74LVCH162245ADGG,1	9352 387 30112	Volume production	SOT362-1 (TSSOP48)	Tube	Standard Marking	
74LVCH162245ADGG	74LVCH162245ADGG:1	9352 387 30118	Volume production	SOT362-1 (TSSOP48)	Reel Pack, SMD, 13"	Standard Marking	
74LVCH162245ADL	74LVCH162245ADL,11	9352 387 20112	Volume production	SOT370-1 (SSOP48)	Tube	Standard Marking	
74LVCH162245ADL	74LVCH162245ADL:11	9352 387 20118	Volume production	SOT370-1 (SSOP48)	Tape reel smd	Standard Marking	

The variants in the table below are discontinued. See the table Discontinued information for more information.

Type number	Orderable part number	Ordering code (12NC)	Product status	Package	Packing	Marking	ECCN
74LVC162245ADGG	74LVC162245ADGG,51	9352 377 00512	Withdrawn Replacement product	SOT362-1 (TSSOP48)	Tube Dry Pack	Standard Marking	
74LVC162245ADGG	74LVC162245ADGG:51	9352 377 00518	Withdrawn Replacement product	SOT362-1 (TSSOP48)	Reel Dry Pack, SMD, 13"	Standard Marking	
74LVCH162245ADGG	74LVCH162245ADGG:5	9352 387 30518	Discontinued Replacement product	SOT362-1 (TSSOP48)	Reel Dry Pack, SMD, 13"	Standard Marking	
74LVCH162245ADGG	74LVCH162245ADGG,5	9352 387 30512	Withdrawn Replacement product	SOT362-1 (TSSOP48)	Tube Dry Pack	Standard Marking	

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Quality/reliability/chemical content Hide

Type number	Orderable part number	Chemical content	RoHS	Leadfree conversion date	RHF	IFR (FIT)	MTBF (hours)	MSL	MSL LF
74LVC162245ADGG	74LVC162245ADGG,11	74LVC162245ADGG	EU/CN RoHs COMPLIANT Pb	Always Pb-free	D	3,87	2,58E+08	1	1
74LVC162245ADGG	74LVC162245ADGG:11	74LVC162245ADGG	EU/CN RoHs COMPLIANT Pb	Always Pb-free	D	3,87	2,58E+08	1	1
74LVC162245ADL	74LVC162245ADL,112	74LVC162245ADL	EU/CN RoHs COMPLIANT Pb	week 13, 2005	G	3,87	2,58E+08	1	1
74LVC162245ADL	74LVC162245ADL,118	74LVC162245ADL	EU/CN RoHs COMPLIANT Pb	week 13, 2005	G	3,87	2,58E+08	1	1
74LVCH162245ADGG	74LVCH162245ADGG,1	74LVCH162245ADGG	EU/CN RoHs COMPLIANT Pb	Always Pb-free	D	3,87	2,58E+08	1	1
74LVCH162245ADGG	74LVCH162245ADGG:1	74LVCH162245ADGG	EU/CN RoHs COMPLIANT Pb	Always Pb-free	D	3,87	2,58E+08	1	1
74LVCH162245ADL	74LVCH162245ADL,11	74LVCH162245ADL	EU/CN RoHs COMPLIANT Pb	week 13, 2005	G	3,87	2,58E+08	1	1
74LVCH162245ADL	74LVCH162245ADL:11	74LVCH162245ADL	EU/CN RoHs COMPLIANT Pb	week 13, 2005	G	3,87	2,58E+08	1	1

The variants in the table below are discontinued. See the table Discontinued information for more information.

Type number	Orderable part number	Chemical content	RoHS	Leadfree conversion date	RHF	IFR (FIT)	MTBF (hours)	MSL	MSL LF
74LVC162245ADGG	74LVC162245ADGG,51	74LVC162245ADGG	EU/CN RoHs COMPLIANT Pb	week 14, 2005	G	3,87	2,58E+08	2	2
74LVC162245ADGG	74LVC162245ADGG:51	74LVC162245ADGG	EU/CN RoHs COMPLIANT Pb	week 14, 2005	G	3,87	2,58E+08	2	2
74LVCH162245ADGG	74LVCH162245ADGG:5	74LVCH162245ADGG	EU/CN RoHs COMPLIANT Pb	week 14, 2005	G	3,87	2,58E+08	2	2
74LVCH162245ADGG	74LVCH162245ADGG,5	74LVCH162245ADGG	EU/CN RoHs COMPLIANT Pb	week 14, 2005	G	3,87	2,58E+08	2	2

Quality and reliability disclaimer

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Discontinued information Hide

Type number	Ordering code (12NC)	Last-time buy date	Last-time delivery date	Replacement product	DN Notice	Status	Comments
74LVC162245ADGG	935237700512				DN		
74LVC162245ADGG	935237700518				DN		
74LVCH162245ADGG	935238730518				DN		
74LVCH162245ADGG	935238730512				DN		

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Design support Hide

Application note

Interfacing 3 Volt and 5 Volt Applications (v.1.0, 1995-09-15)
Power considerations when using CMOS and BiCMOS logic devices (v.2.0, 2002-02-05)
Pin FMEA for LVC family (v.1.0, 2011-02-04)

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Quality and reliability disclaimer