MS62256CLL
32K x 8 CMOS STATIC RAM

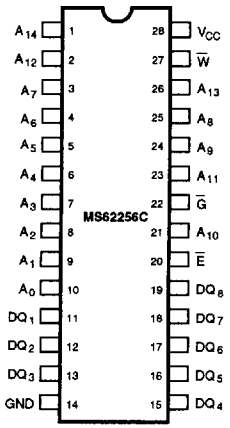
Features

- High-speed – 70/100 ns
- Low Power dissipation:
  - — 385mW (Max) Operating
  - — 16.5mW (Max) Standby
  - — 0.55mW (Max) Power-down
  - — 5µA (Max) I_{CCDR}
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V
- Data retention as low as 2V

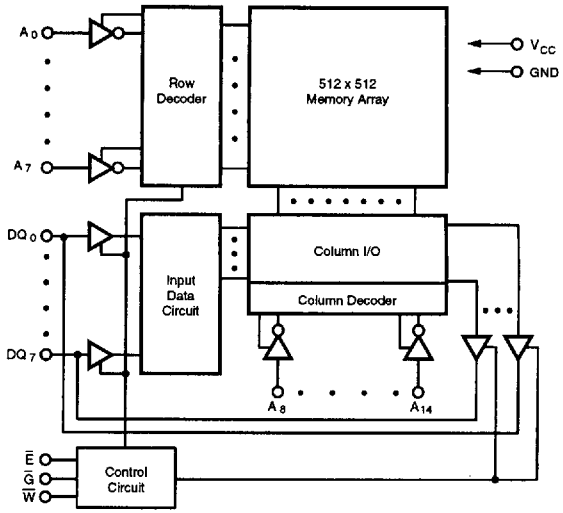
Descriptions

The MS62256CLL is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL-VITELIC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256CLL is available in a standard 28-pin 600 and 300 mil plastic DIP and 330 mil wide SOG.

Pin Configurations



Functional Block Diagram



Pin Descriptions

A_0 - A_{14} Address Inputs

These 15 address inputs select one of the 32,768 x 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Units
V_{CC}	Supply Voltage	–0.3 to 7	V
V_{IN}	Input Voltage	–0.3 to 7	
V_{DQ}	Input/Output Voltage Applied	–0.3 to 6	
T_{BIAS}	Temperature Under Bias	–10 to +125	°C
T_{STG}	Storage Temperature	–40 to +150	°C

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Temperature	V_{cc}
Commercial	0°C to +70°C	5V ± 10%

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions		-70 Min.	-70 Typ.(1)	-70 Max.	-10 Min.	-10 Typ.(1)	-10 Max.	Units
V_{IL}	Guaranteed Input LOW Voltage(2)(3)			–0.3	-	+0.8	–0.3	-	+0.8	V
V_{IH}	Guaranteed Input HIGH Voltage(2)			2.2	-	6	2.2	-	6	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}		–2	-	2	–2	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E} = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}		–2	-	2	–2	-	2	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.1mA		-	-	0.4	-	-	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –1mA		2.4	-	-	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IL}$, $I_{I/O}$ = 0mA, F=F_{max}(4)		-	-	80	-	-	70	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E} = V_{IH}$, $I_{I/O}$ = 0mA		-	-	3	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E} \geq V_{CC} - 0.2V$	MS62256CL	-	-	0.1	-	-	0.1	mA
			MS62256CLL			20			20	µA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
3. $F_{MAX} = 1/t_{RC}$.

Capacitance(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

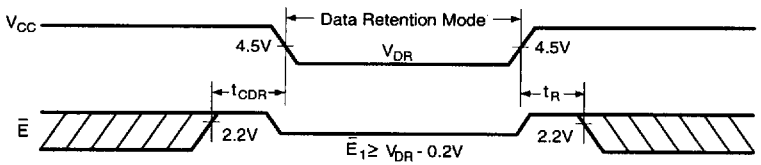
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E} \geq V_{CC}$ -0.2V	2.0	-	5.5	V
I_{CCDR}	Data Retention Current MS62256CLL	V_{DR} = 3.0V, $\overline{E} \geq V_{DR} - 0.2V$	-	1.0	10(2)	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(3)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. V_{DR} = 3.0 V, T_A = 0°C to 40°C, I_{CCDR} = 5µA
3. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



AC Test Conditions

Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

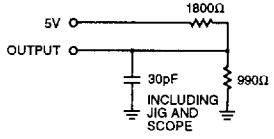


Figure 1a

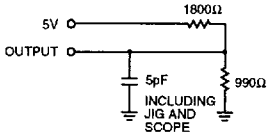


Figure 1b

Equivalent to:

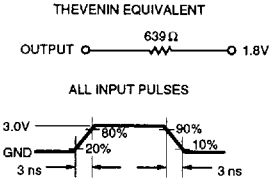


Figure 2

AC Electrical Characteristics (over the commercial operating range)

Read Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256C-70 Min.	Typ.	Max.	MS62256C-10 Min.	Typ.	Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	70		-	100		-	ns
t_{AVQV}	t_{AA}	Address Access Time	-		70	-		100	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-		70	-		100	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-		40	-		50	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	10		-	10		-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		-	5		-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-		30	-		35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-		30	-		35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5		-	10		-	ns

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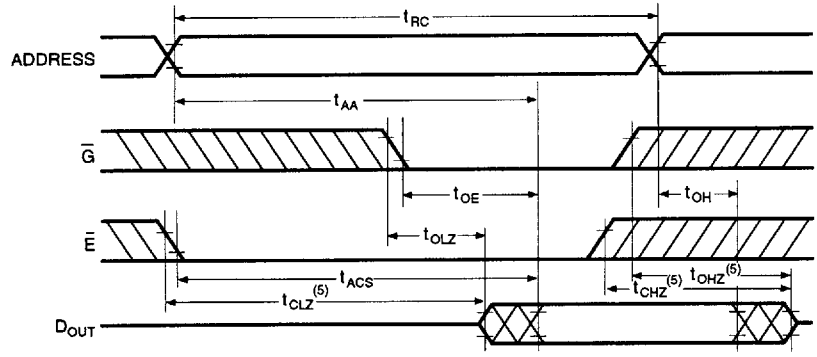
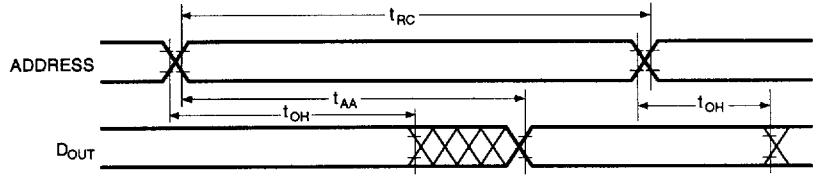
Switching Waveforms (Read Cycle)

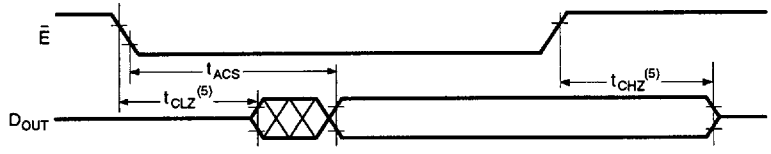
READ CYCLE 1(1)



READ CYCLE 2(1, 2, 4)



READ CYCLE 3(1, 3, 4)



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

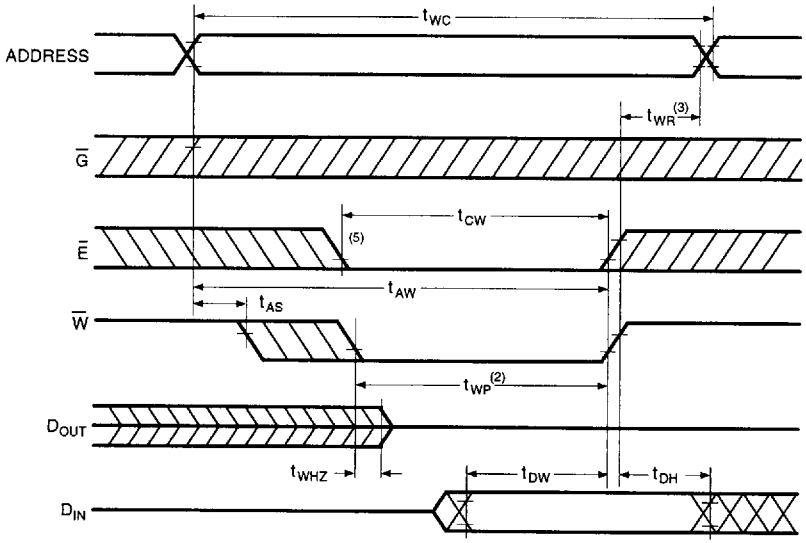
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256C-70			MS62256C-10			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	70		-	100		-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	65		-	90		-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0		-	0		-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	65		-	90		-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	55		-	75		-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	5		-	5		-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0		30	0		35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	35		-	40		-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		-	0		-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	-		30	-		40	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5		-	5		-	ns

Switching Waveforms (Write Cycle)

WRITE CYCLE 1(1)



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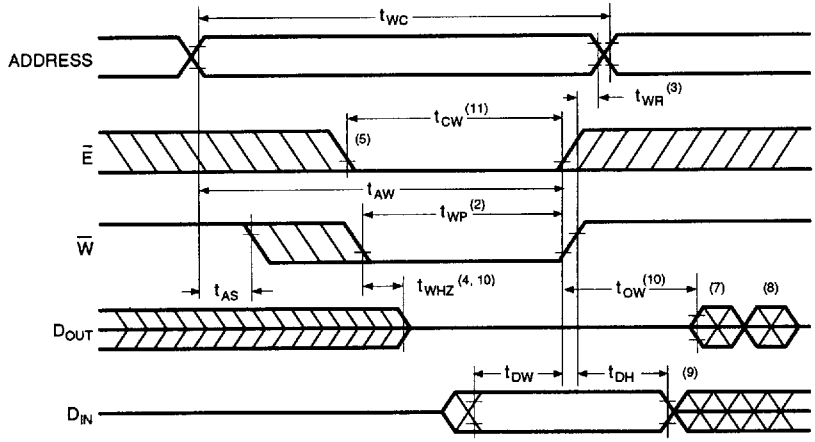
Switching Waveforms (Write Cycle)

Write Cycle 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

Ordering Information

Speed (Ns)	Ordering Part Number	Package	Temperature Range
70	MS62256CLL-70PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
70	MS62256CLL-70FC	28 Pin 330 mil SOG	0°C to +70°C
70	MS62256CLL-70NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
100	MS62256CLL-10PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
100	MS62256CLL-10FC	28 Pin 330 mil SOG	0°C to +70°C
100	MS62256CLL-10NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C