



128Kx8 MONOLITHIC SRAM, SMD 5962-96691 (pending)

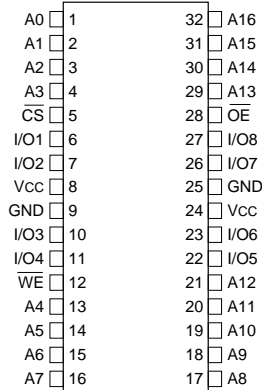
FEATURES

- Access Times 70, 85, 100, 120ns
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
 - 32 lead Ceramic SOJ (Package 101)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
 - 32 pin Ceramic DIP (Package 300)
 - 32 lead Ceramic SOJ (Package 101)
 - 32 lead Ceramic Flat Pack (Package 206)
- MIL-STD-883 Compliant Devices Available
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs

REVOLUTIONARY PINOUT

32 CSOJ (DR)

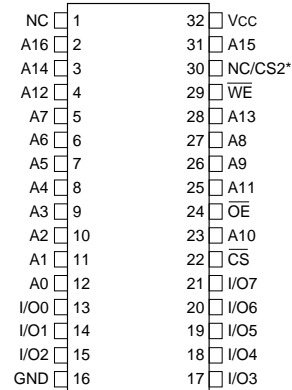
TOP VIEW



EVOLUTIONARY PINOUT

32 DIP 32 CSOJ (DE) 32 FLATPACK (FE)

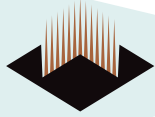
TOP VIEW



* NC for single chip select devices
CS2 for dual chip select devices

PIN DESCRIPTION

A0-16	Address Inputs
I/O 0-7	Data Input/Output
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
Vcc	+5.0V Power
GND	Ground



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Package	Speed (ns)	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	32 Pin CSOJ, DIP, Flat Pack Evolutionary	70 to 120	12	pF
			32 Pin CSOJ Revolutionary	70 to 120	20	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	32 Pin CSOJ, DIP, Flat Pack Evolutionary	70 to 120	12	pF
			32 Pin CSOJ Revolutionary	70 to 120	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10		10	µA
Output Leakage Current	I _{LO}	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND$ to V _{CC}		10		10		10		10	µA
Operating Supply Current	I _{CC}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5MHz, V_{CC} = 5.5$		30		30		30		30	mA
Standby Current	I _{SB}	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5MHz, V_{CC} = 5.5$		1.0		1.0		0.6		0.6	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		20	400		20	400		20	400		20	400	µA



AC CHARACTERISTICS
(VCC = 5.0V, TA = -55°C To +125°C)

Parameter	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	70		85		100		120		ns
Address Access Time	t _{AA}		70		85		100		120	ns
Output Hold from Address Change	t _{OH}	3		3		3		3		ns
Chip Select Access Time	t _{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t _{OE}		35		45		50		60	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	5		5		5		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		25		25		35		35	ns
Output Disable to Output in High Z	t _{OHZ} ¹		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(VCC = 5.0V, TA = -55°C To +125°C)

Parameter	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	70		85		100		120		ns
Chip Select to End of Write	t _{CW}	60		75		80		100		ns
Address Valid to End of Write	t _{AW}	60		75		80		100		ns
Data Valid to End of Write	t _{DW}	30		35		40		50		ns
Write Pulse Width	t _{WP}	50		55		70		80		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	5		5		5		5		ns
Output Active from End of Write	t _{OW} ¹	5		5		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		25		30		35		35	ns
Data Hold Time	t _{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

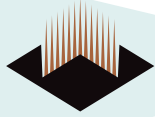
AC TEST CIRCUIT

The diagram shows a Device Under Test (D.U.T.) connected to a bridge circuit. The bridge consists of four diodes. Two current sources are connected to the bridge nodes, labeled I_{OL} and I_{OH}. A bipolar supply V_Z ≈ 1.5V is connected across the bridge. A capacitor C_{eff} = 50 pf is connected to the D.U.T. input.

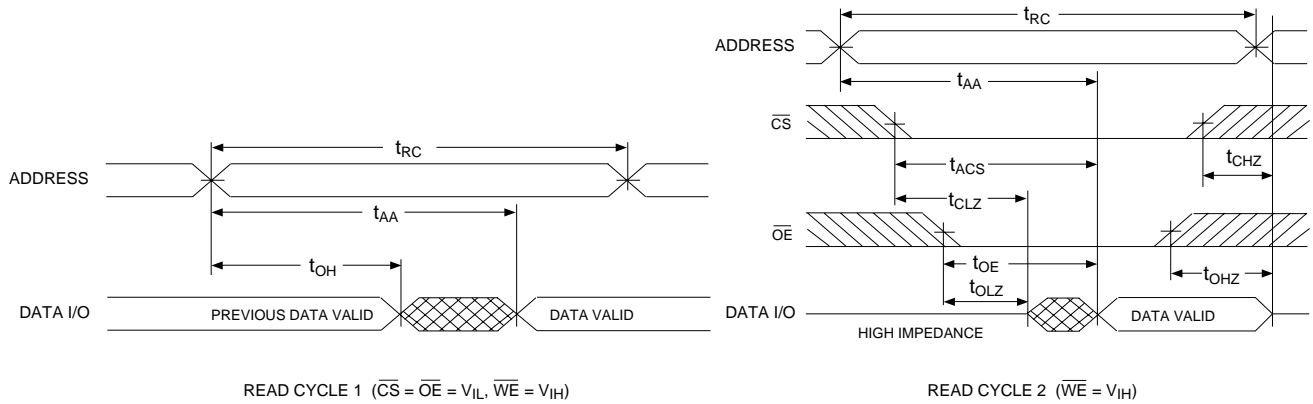
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

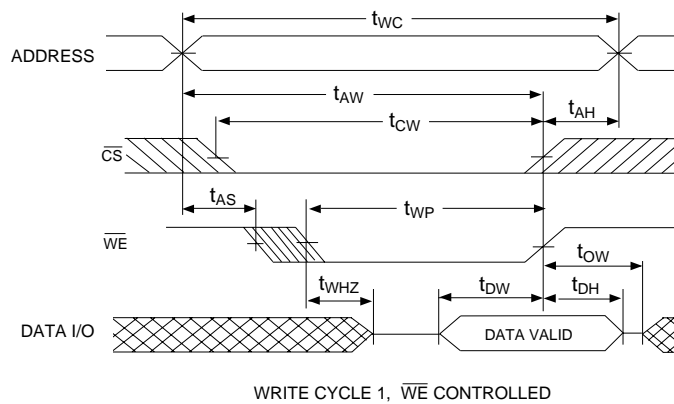
NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



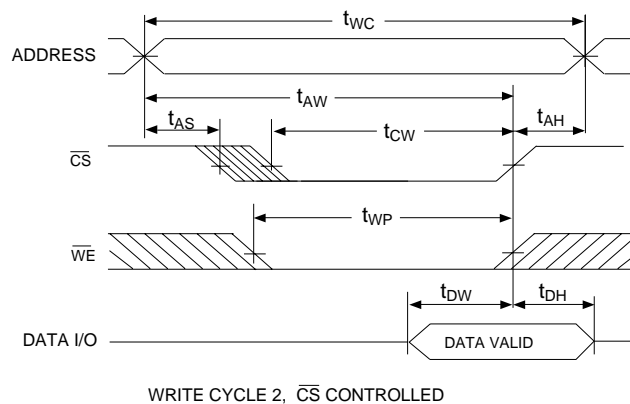
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED

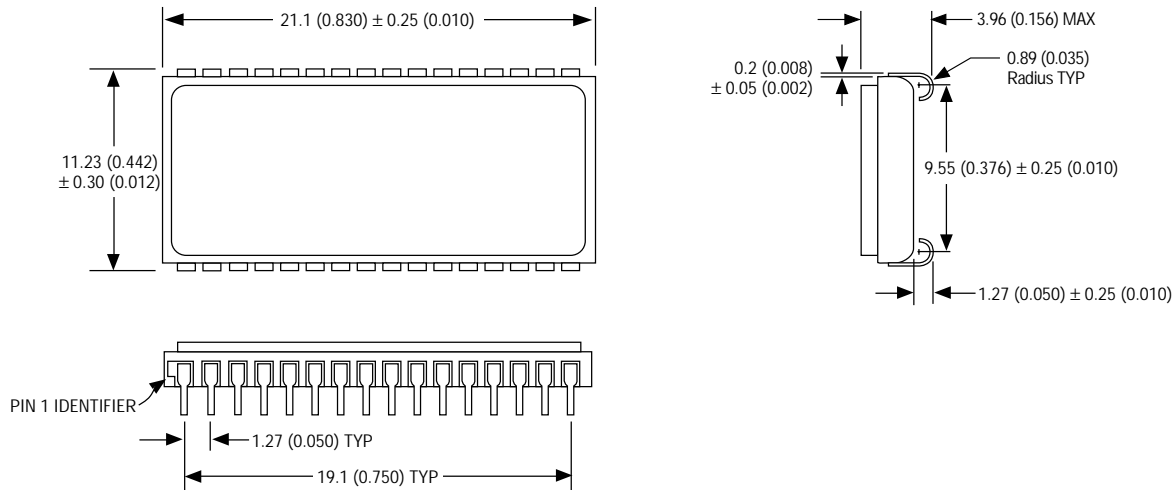


WRITE CYCLE - \overline{CS} CONTROLLED



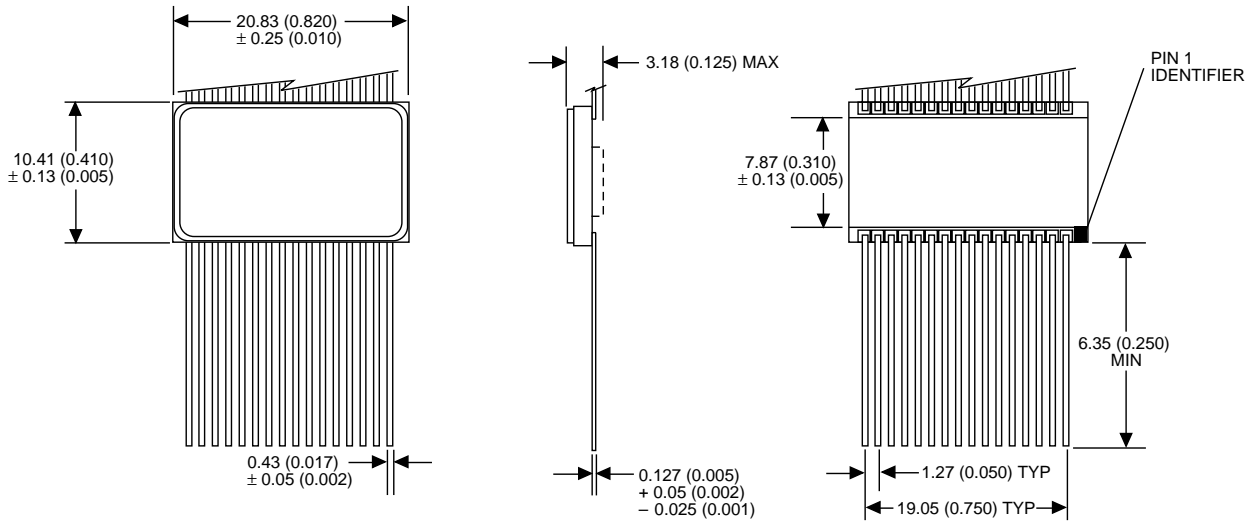


PACKAGE 101: 32 LEAD, CERAMIC SOJ

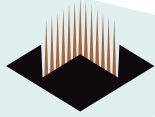


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

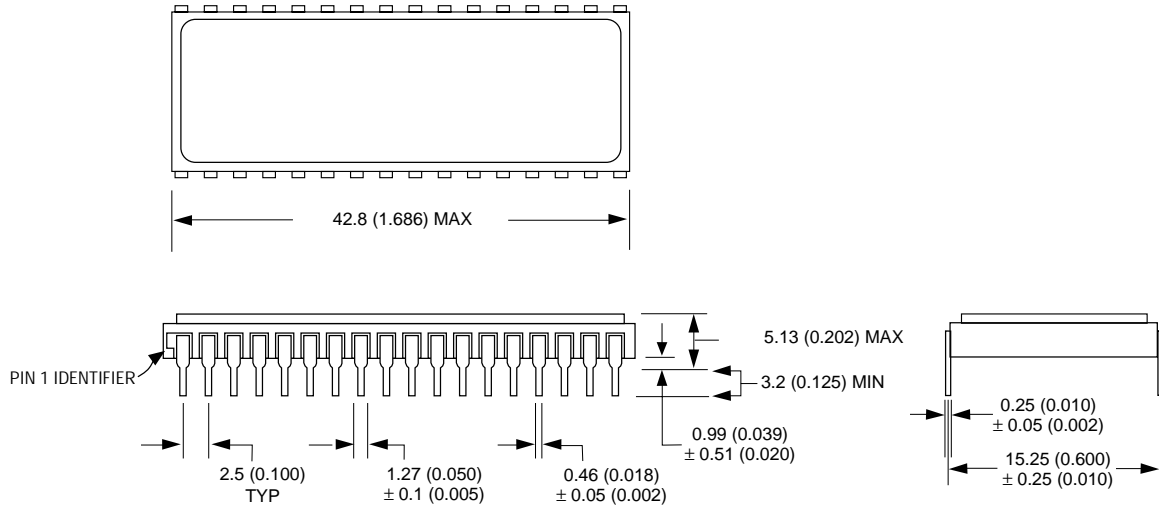
PACKAGE 206: 32 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



DATA RETENTION CHARACTERISTICS

(TA = -55°C to +125°C)

LOW POWER VERSION ONLY

Parameter	Symbol	Conditions			Units
			Min	Max	
Data Retention Supply Voltage	V _{DR}	CS ≥ V _{CC} - 0.2V	2.0	5.5	V
Data Retention Current	I _{CCDR3}	V _{CC} = 2V		400	μ

ORDERING INFORMATION

W M S 128K 8 X - XXX X X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

SPECIAL PROCESSING:

E = Epitaxial Layer

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE:

C = 32 Pin Ceramic .600" DIP (Package 300)

DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary

DR = 32 Lead Ceramic SOJ (Package 101) Revolutionary

FE = 32 Lead Ceramic Flat Pack (Package 206)

ACCESS TIME (ns)

IMPROVEMENT MARK

C = Dual Chip Select Device

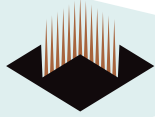
L = Low Power for 2V Data Retention

ORGANIZATION, 128K x 8

SRAM

MONOLITHIC

WHITE MICROELECTRONICS



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 8 SRAM Monolithic	120ns	32 lead SOJ Revol (DR)	5962-9669101HUX*
128K x 8 SRAM Monolithic	100ns	32 lead SOJ Revol (DR)	5962-9669102HUX*
128K x 8 SRAM Monolithic	85ns	32 lead SOJ Revol (DR)	5962-9669103HUX*
128K x 8 SRAM Monolithic	70ns	32 lead SOJ Revol (DR)	5962-9669104HUX*
128K x 8 SRAM Monolithic	120ns	32 lead SOJ Evol (DE)	5962-9669101HTX*
128K x 8 SRAM Monolithic	100ns	32 lead SOJ Evol (DE)	5962-9669102HTX*
128K x 8 SRAM Monolithic	85ns	32 lead SOJ Evol (DE)	5962-9669103HTX*
128K x 8 SRAM Monolithic	70ns	32 lead SOJ Evol (DE)	5962-9669104HTX*
128K x 8 SRAM Monolithic	120ns	32 pin DIP (C)	5962-9669101HYX*
128K x 8 SRAM Monolithic	100ns	32 pin DIP (C)	5962-9669102HYX*
128K x 8 SRAM Monolithic	85ns	32 pin DIP (C)	5962-9669103HYX*
128K x 8 SRAM Monolithic	70ns	32 pin DIP (C)	5962-9669104HYX*
128K x 8 SRAM Monolithic	120ns	36 lead Flatpack (F)	5962-9669101HXX*
128K x 8 SRAM Monolithic	100ns	36 lead Flatpack (F)	5962-9669102HXX*
128K x 8 SRAM Monolithic	85ns	36 lead Flatpack (F)	5962-9669103HXX*
128K x 8 SRAM Monolithic	70ns	36 lead Flatpack (F)	5962-9669104HXX*

* Pending