Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT646T/AT/CT
IDT54/74FCT648T/AT/CT
IDT54/74FCT651T/AT/CT
IDT54/74FCT652T/AT/CT

T-52-31

FEATURES:

- IDT54/74FCT646T/648T/651T/652T equivalent to FAST™ speed
- **IDT54/74FCT646AT/648AT/651AT/652AT 30% faster than FAST™**
- **IDT54/74FCT646CT/648CT/651CT/652CT 40% faster than FAST™**
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of true and inverting data paths
- I_{OL} = 64mA (commercial), 48mA (military)
- CMOS power levels
- TTL input and output level compatible
- Available in 24-pin (300 mil) CERDIP, plastic DIP, SOIC, CERPACK, 28-pin LCC and PLCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

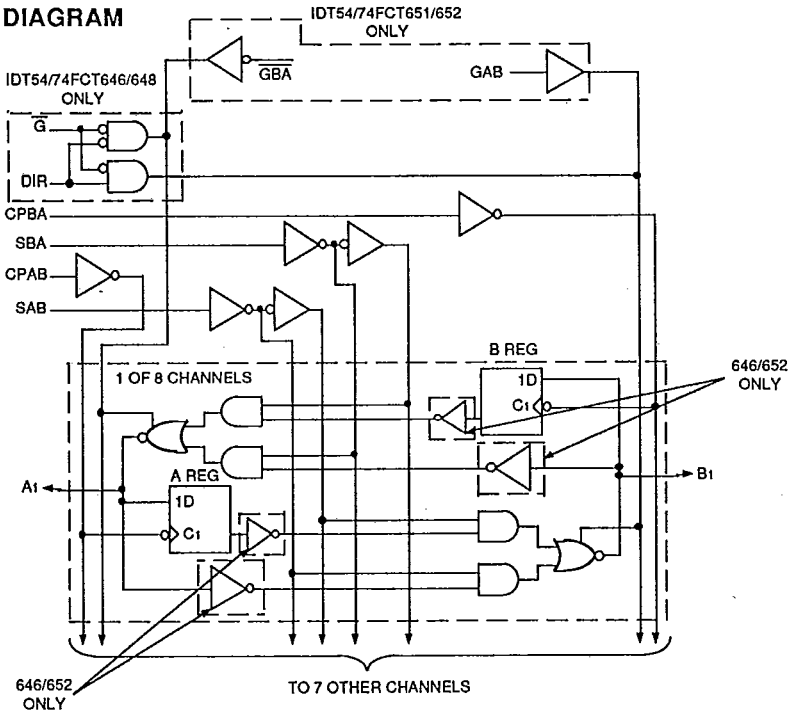
The IDT54/74FCT646/648T/AT/CT and IDT54/74FCT651/652T/AT/CT consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

The '651/652 utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The '646/648 utilize the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor, Inc.

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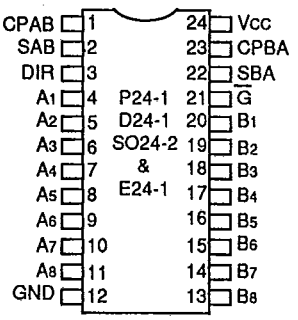
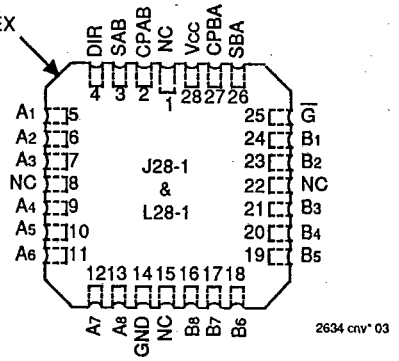
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

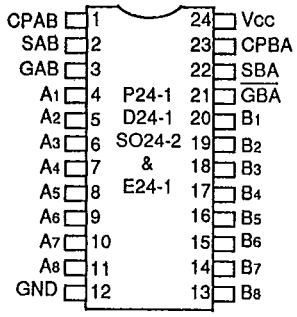
2634 cnv* 02

IDT54/74FCT646T/648T



2634 cnv* 03

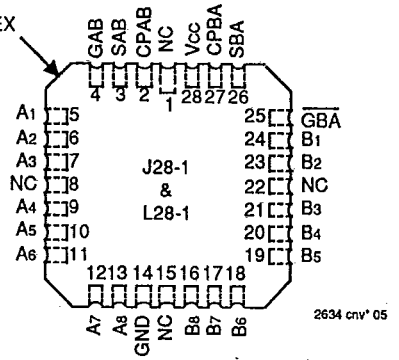
LCC/PLCC
TOP VIEW



DIP/SOIC/CERPACK
TOP VIEW

2634 cnv* 04

IDT54/74FCT651T/652T

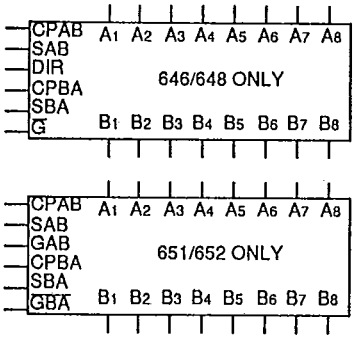


2634 cnv* 05

LCC/PLCC
TOP VIEW

6

LOGIC SYMBOLS



2634 cnv* 05

PIN DESCRIPTION

Pin Names	Description
A1 - A8	Data Register A Inputs Data Register B Outputs
B1 - B8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (646/648)
GAB, $\overline{GBA}$	Output Enable Inputs (651/652)

2634 tbl 01

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FUNCTION TABLE IDT54/74FCT646/648T/AT/CT

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	IDT54/74FCT646T	IDT54/74FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

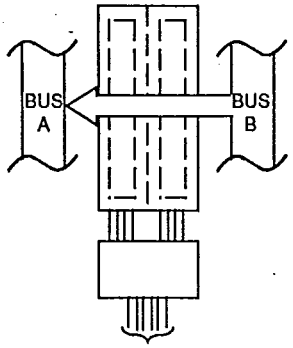
2634 tbl 02

FUNCTION TABLE IDT54/74FCT651/652T/AT/CT

Inputs						Data I/O		Operation or Function	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	IDT54/74FCT651T	IDT54/74FCT652T
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in Both Registers[3]	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in Both Registers[4]	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

2634 tbl 03

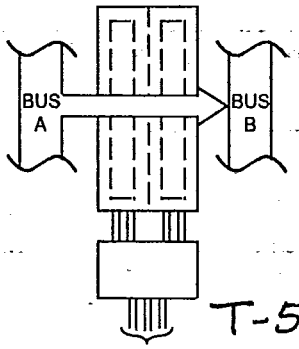
NOTES:
1. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ≠ = LOW-to-HIGH transition.
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.



	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
651/652	L	L	X	X	X	L
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO A

2634 cnv* 07



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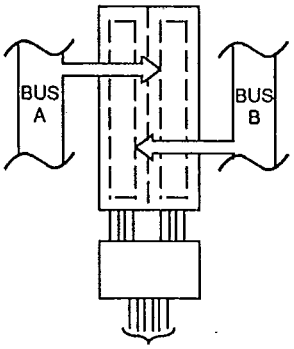
	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
651/652	H	H	X	X	L	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO B

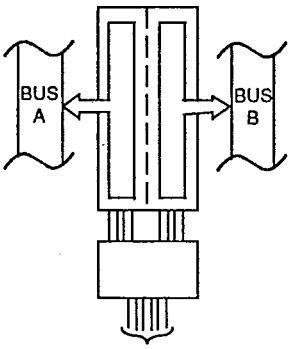
2634 cnv* 08



	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
651/652	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM
A AND/OR B

2634 cnv* 09



	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
651/652	H	L	H or L	H or L	H	H
646/648[1]	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X

TRANSFER STORES
DATA TO A AND/OR B

2634 cnv* 10

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NOTE:
1. 646/648 cannot transfer data to A bus and B bus simultaneously.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2634 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2634 tbl 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE T-52-31

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	−5	µA
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = 2.7V	—	—	15	µA
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	−15	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		−60	−120	−225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.	—	0.3	0.55	V
			I_{OL} = 64mA COM'L.[4]	—	0.3	0.55	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2634 tbl 06

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

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POWER SUPPLY CHARACTERISTICS

T-52-31

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{GAB}$ = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{GAB}$ = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{GAB}$ = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2634 tbl 07

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition(1)	646T/648T/651T/652T				646AT/648AT/651AT/652AT				646CT/648CT/651CT/652CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	1.5	6.0	ns
tPZH tPZL	Output Enable Time, $\overline{G}$, DIR to Bus(3)		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	1.5	8.9	ns
tPHZ tPLZ	Output Disable Time, $\overline{G}$, DIR to Bus(3)		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	1.5	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	1.5	6.3	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	1.5	7.0	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

2634 tbl 08

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. GAB, $\overline{GBA}$ to Bus for 651, 652.

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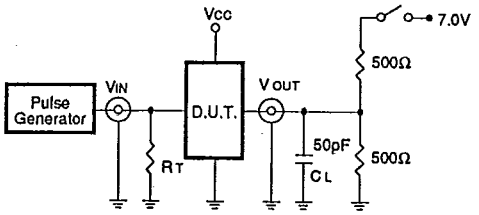
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

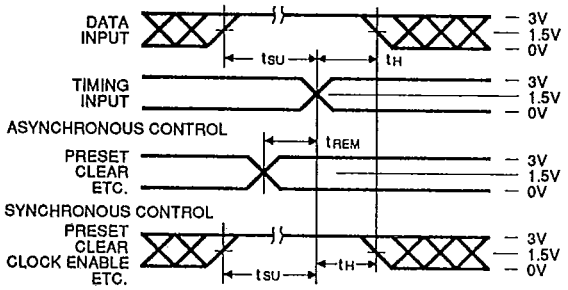
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2537 tbl 08

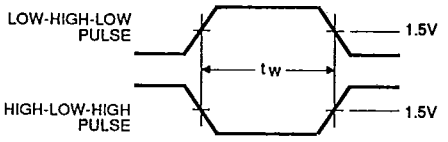
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

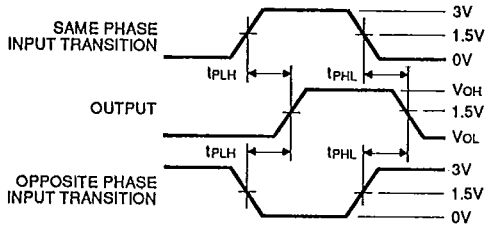
SET-UP, HOLD AND RELEASE TIMES



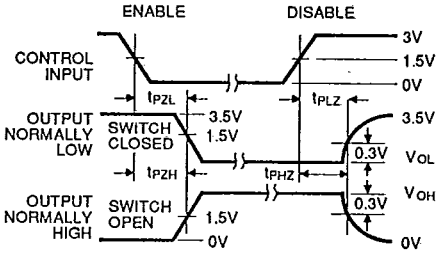
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



2634 drw 15

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

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ORDERING INFORMATION

IDT XX FCT XXXX X X

	Temperature Range	Device Type	Package	Process/ Temperature Range
				Blank — Commercial
				B — MIL-STD-883, Class B
			P — Plastic DIP	
			D — CERDIP	
			SO — Small Outline IC	
			L — Leadless Chip Carrier	
			E — CERPACK	
			J — Plastic Leaded Chip Carrier	
		646T — Non-inverting Octal Transceiver/Register		
		646AT — Fast Non-inverting Octal Transceiver/Register		
		646CT — Super Fast Non-inverting Octal Transceiver/Register		
		648T — Inverting Octal Transceiver/Register		
		648AT — Fast Inverting Octal Transceiver/Register		
		648CT — Super Fast Inverting Octal Transceiver/Register		
		651T — Inverting Octal Transceiver/Register		
		651AT — Fast Inverting Octal Transceiver/Register		
		651CT — Super Fast Inverting Octal Transceiver/Register		
		652T — Non-inverting Octal Transceiver/Register		
		652AT — Fast Non-inverting Octal Transceiver/Register		
		652CT — Super Fast Non-inverting Octal Transceiver/Register		
	54 — –55°C to +125°C			
	74 — 0°C to +70°C			

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