CY2XP61

125 MHz LVPECL Clock Generator

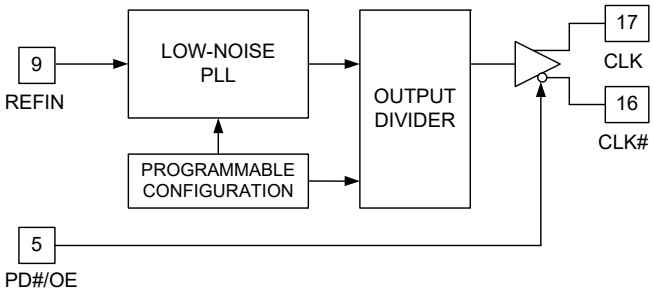
Features

- Output: 125 MHz LVPECL output pair
- Input: 15 MHz 1.8-V external reference clock
- RMS phase jitter:
  - 12 kHz to 20 MHz offset: 2.60 ps (typical)
- Package: Pb-free 24-pin QFN
- Supply voltage: 3.3 V
- Temperature range: Commercial and Industrial

Functional Description

The CY2XP61 is a PLL-based high performance clock generator that uses Cypress's low-noise VCO technology to achieve less than 4 ps typical RMS phase jitter. The CY2XP61 uses a 1.8 V external reference clock input to generate one LVPECL output pair, which can be asynchronously enabled/disabled with an OE pin (Pin 5). The device operates at 3.3 V. Pin 5 can also be programmed as PD#. The OE function is used to enable or disable the CLK output quickly, but it does not reduce core power consumption. The PD# function puts the device into a low-power state.

Logic Block Diagram



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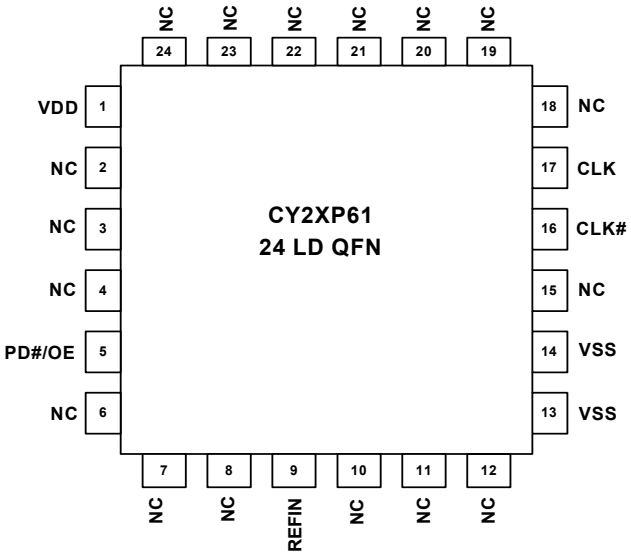
Pinouts

Figure 1. 24-pin QFN pinout



Pin Definitions

Pin	Name	Type	Description
1	VDD	Power	3.3 V power supply.
2, 3, 4, 6, 7, 8, 10, 11, 12, 15, 18, 19, 20, 21, 22, 23, 24	NC		No Connection
5	PD#/OE	Input	Power Down (Active Low)/Output Enable
9	REFIN	Input	Reference Clock Input
13, 14	VSS	Power	Ground
16,17	CLK#, CLK	LVPECL Output	Differential clock output

Absolute Maximum Conditions

Parameter	Description	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.4	V
V_{IN}[1]	DC input voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Storage temperature	Non-operating	–65	150	°C
T_J	Junction temperature		–	135	°C
ESD_{HBM}	ESD protection, Human body model	JEDEC STD 22-A114-B	2000	–	V
UL–94	Flammability rating	At 1/8 in.	V–0		
Θ_{JA}[2]	Thermal resistance, junction to ambient	0 m/s airflow	20		°C/W

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	3.3 V supply voltage	3.135	3.465	V
T_A	Ambient temperature, Commercial	0	70	°C
T_A	Ambient temperature, industrial	–40	85	°C
T_{PU}	Power-up time for all V_{DD} to reach minimum specified supply voltage (power ramp must be monotonic)	0.05	500	ms

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Simulated using Sentinel TI software. Layer thicknesses are 2/1/1/2oz, with the assumption that 5% area under the package is vias.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Operating supply current with output unterminated	V_{DD} = 3.465 V, F_{OUT} = 125 MHz	–	–	125	mA
I_{DDT}	Operating supply current with output terminated	V_{DD} = 3.465 V, F_{OUT} = 125 MHz	–	–	150	mA
I_{OZ}	LVPECL output leakage current	OE = V_{SS}	–35	–	35	µA
V_{OH}	LVPECL output high voltage	V_{DD} = 3.3 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} – 1.15	–	V_{DD} – 0.75	V
V_{OL}	LVPECL output low voltage	V_{DD} = 3.3 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} – 2.0	–	V_{DD} – 1.625	V
V_{OD1}	LVPECL differential output voltage	V_{DD} = 3.3 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	600	–	1000	mV
V_{OCM}	LVPECL output common mode voltage (V_{OH} + V_{OL}) / 2	V_{DD} = 3.3 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	1.2	–	–	V
V_{IH1}	Input high voltage, OE		0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL1}	Input low voltage, OE		–0.3	–	0.3 × V_{DD}	V
V_{IH2}	Input high voltage, REFIN		1.25	–	1.8	V
V_{IL2}	Input low voltage, REFIN		–	–	0.25	V
I_{IH}	Input high current, OE	OE = V_{DD}	–	–	115	µA
I_{IL}	Input low current, OE	OE = V_{SS}	–50	–	–	µA
C_{IN}[3]	Input capacitance, OE		–	15	–	pF
C_{INREF}[3]	Pin capacitance, REFIN		–	4.5	–	pF

AC Electrical Characteristics

Parameter [3]	Description	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output frequency	15 MHz reference input		125		MHz
T_R, T_F	Output rise or fall time	20% to 80% of full output swing	–	0.5	1.0	ns
$T_{Jitter(\phi)}$	RMS phase jitter (Random)	12 kHz to 20 MHz offset	–	2.6	4	ps
T_{DC}	Output duty cycle	Measured at zero crossing point	45	50	55	%
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min)	–	–	5	ms
T_{OHZ}	Output disable time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T_{OE}	Output enable time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns

Note
3. Not 100% tested, guaranteed by design and characterization.

Parameter Measurements

Figure 2. 3.3 V Output Load AC Test Circuit

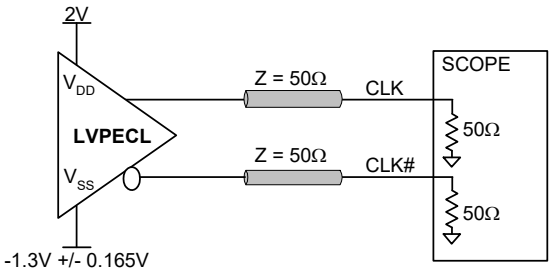


Figure 3. Output DC Parameters

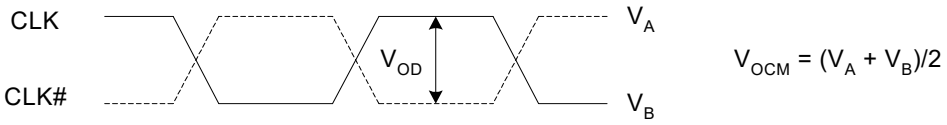


Figure 4. Output Rise and Fall Time

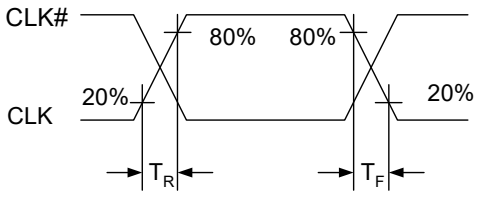


Figure 5. RMS Phase Jitter

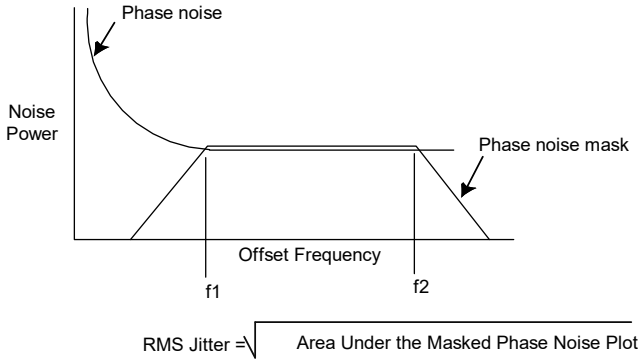


Figure 6. Output Duty Cycle

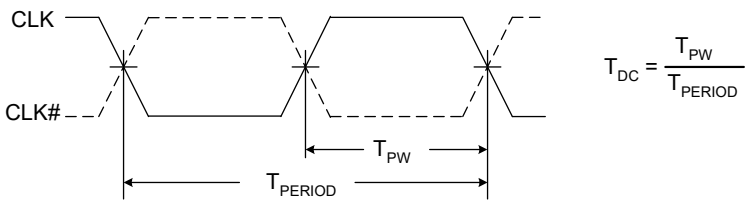
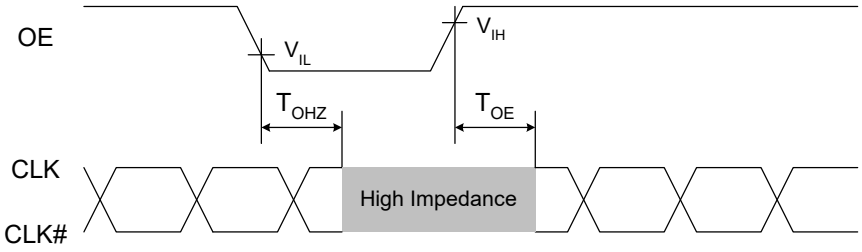


Figure 7. Output Enable and Disable Timing

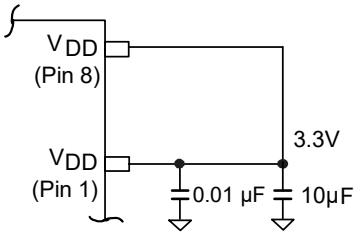


Application Information

Power Supply Filtering Techniques

As in any high-speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 8 illustrates a typical filtering scheme. Since all the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 µF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 µF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

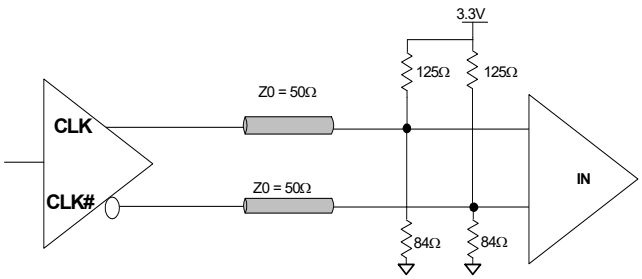
Figure 8. Power Supply Filtering



Termination for LVPECL Output

The CY2XP61 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm DC termination on each of the two output signals. For 3.3 V operation, this datasheet specifies output levels for termination to V_{DD} – 2.0 V. Note that it is also possible to terminate with 50 ohms to ground (V_{SS}), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance (Z_0) should match the termination impedance. Figure 9 shows a standard termination scheme.

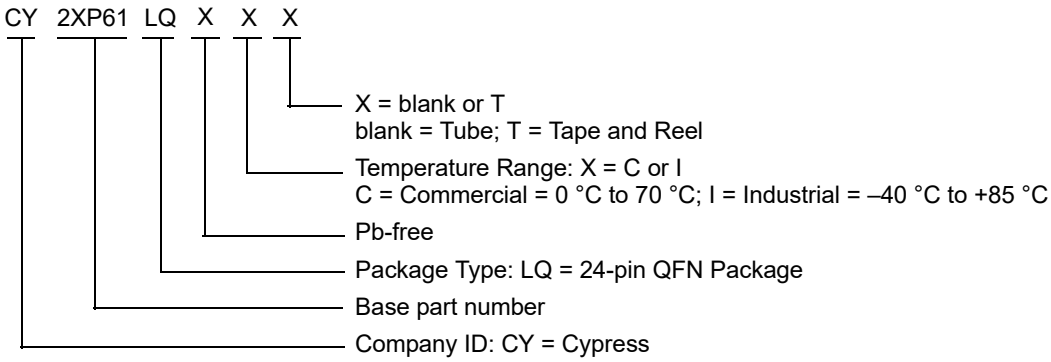
Figure 9. LVPECL Output Termination



Ordering Information

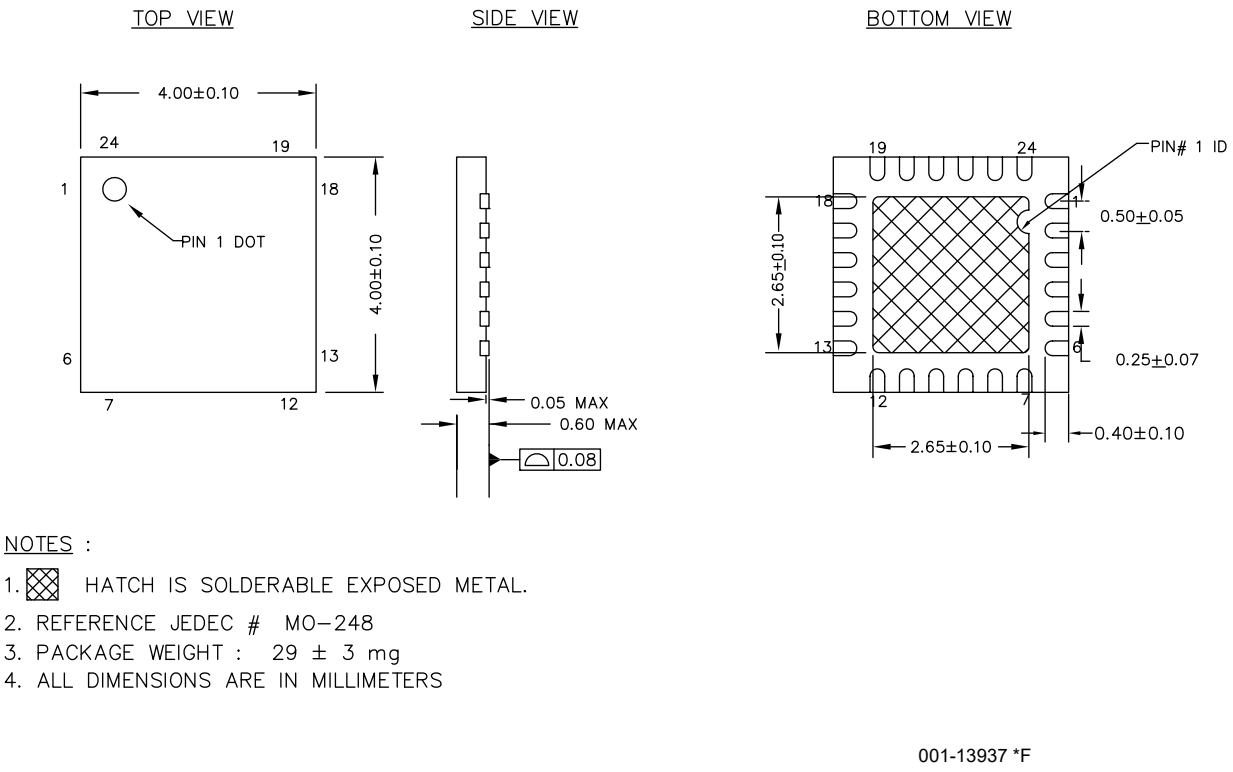
Part Number	Package Type	Product Flow
CY2XP61LQXC	24-pin QFN	Commercial, 0 °C to 70 °C
CY2XP61LQXCT	24-pin QFN – Tape and Reel	Commercial, 0 °C to 70 °C
CY2XP61LQXI	24-pin QFN	Industrial, –40 °C to 85 °C
CY2XP61LQXIT	24-pin QFN – Tape and Reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Diagram

Figure 10. 24-pin QFN (4 × 4 × 0.55 mm) LQ24A (2.65 × 2.65) E-Pad (Sawn) Package Outline, 001-13937



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Acronyms

Acronym	Description
ESD	Electrostatic Discharge
JEDEC	Joint Electron Devices Engineering Council
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
OE	Output Enable
PLL	Phase-Locked Loop
QFN	Quad-Flat No-lead
VCO	Voltage-Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
kHz	kilohertz
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt

Document History Page

Document Title: CY2XP61, 125 MHz LVPECL Clock Generator Document Number: 001-75768				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3516636	PURU	02/09/2012	New data sheet.
*A	4020868	CINM	06/05/2013	Changed status from Preliminary to Final. Updated Package Diagram: spec 001-13937 – Changed revision from *C to *E.
*B	4724046	TAVA	04/14/2015	Updated to new template. Completing Sunset Review.
*C	6010792	PAWK	01/02/2018	Updated Package Diagram: spec 001-13937 – Changed revision from *E to *F. Updated to new template.

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