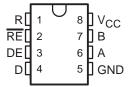
SLLS295A - APRIL 1998 - REVISED DECEMBER 1999

- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27
- Recommended for PROFIBUS Applications
- Operates at Data Rates up to 35 MBaud
- Operating Temperature Range ...-25°C to 85°C
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirement
 ... 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design
- Package Options Include Plastic Small-Outline (D) Package and (P) DIPs

D[†] OR P PACKAGE (TOP VIEW)



†The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN65ALS1176DR).

description

The SN65ALS1176 differential bus transceiver is designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS1176 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS1176 is characterized for operation from -25°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Function Tables

DRIVERS

INPUT	ENABLE	OUT	PUTS
D	DE	Α	В
Н	Н	Н	L
L	Н	L	Н
×	L	Z	Z

RECEIVER

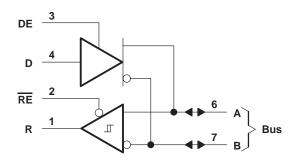
DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
V _{ID} ≥ 0.2 V	L	Н
$-0.2 \text{ V} < \text{V}_{1D} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	Н	Z
Inputs open	L	Н

H = high level, L = low level, X = irrelevant,

logic symbol†

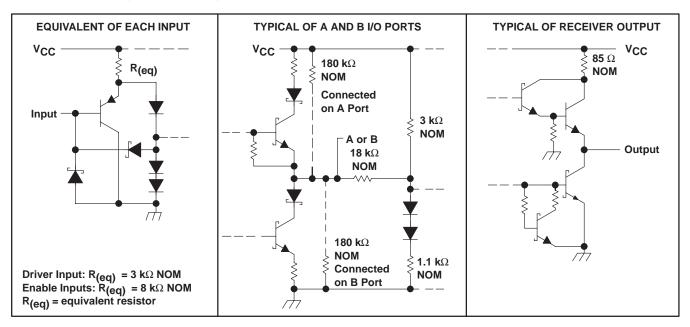
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



^{? =} Indeterminate, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	7 V
Voltage range at any bus terminal	–7 V to 12 V
Enable input voltage, V _I	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
P package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T _{sta}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V _I or V _{IC}				12	V
Imput voltage at any bus terminal (separately of common mode), vp or vpc				-7	V
High-level input voltage, VIH	D, DE, and RE	2			V
Low-level input voltage, V _{IL}	D, DE, and RE			0.8	V
Differential input voltage, V _{ID} (see Note 3)				±12	V
High-level output current, IOH	Driver			-60	mA
I riightievel output current, IOH	Receiver			-400	μΑ
Low level output current lev	Driver			60	mA
Low-level output current, IOL	Receiver			8	IIIA
Operating free-air temperature, T _A	-	-25		85	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



^{2.} The package thermal impedance is calculated in accordance with JESD 51.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	DITIONS†	MIN	TYP‡	MAX	UNIT	
VIK	Input clamp voltage	I _I = -18 mA				-1.5	V	
٧o	Output voltage	I _O = 0		0		6	V	
V _{OD1}	Differential output voltage	I _O = 0		1.5		6	V	
11/1 1	Differential autout valle as	$R_L = 100 \Omega$,	See Figure 1	1/2 V _{OD 1} c	or 2§		V	
IVOD2l	Differential output voltage	$R_L = 54 \Omega$,	See Figure 1	2.1	2.5	5	V	
V _{OD3}	Differential output voltage	$V_{test} = -7 V to 12 V$,	See Figure 2	1.5		5	V	
Δ VOD	Change in magnitude of differential output voltage¶					±0.2	V	
Voc	Common-mode output voltage	$R_L = 54 \Omega \text{ or } 100 \Omega,$	See Figure 1			3 -1	٧	
∆ V _{OC}	Change in magnitude of common-mode output voltage¶					±0.2	V	
1-	Output current	Outputs disabled,	V _O = 12 V			1	mA	
Ю	Output current	See Note 4	$V_O = -7 \text{ V}$			-0.8	IIIA	
I _{IH}	High-level input current	V _I = 2.4 V				20	μΑ	
I _{IL}	Low-level input current	V _I = 0.4 V				-400	μΑ	
		V _O = -4 V				-250		
1	Chart aircuit autaut aurrant#	V _O = 0				-150	mA	
los	Short-circuit output current#	VO = VCC			250	IIIA		
		VO = 8 V			250			
loo	Supply current	No load	Outputs enabled		23	30		
ICC	Supply current	INO IOAU	Outputs disabled		19	26	mA	

[†] The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

NOTE 4: This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

[§] The minimum V_{OD2} with a 100- Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

 $[\]P_{\Delta}|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from one logic state to the other.

[#] Duration of the short circuit should not exceed one second for this test.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

	PARAMETER	TEST CO	TEST CONDITIONS			MAX	UNIT
td(OD)	Differential output delay time					15	ns
t _{sk(p)}	Pulse skew [‡]	$R_L = 54 \Omega$, See Figure 3	$C_L = 50 \text{ pF},$		0	2	ns
t _t (OD)	Differential output transition time	Goo'r iguro o			8		ns
^t PZH	Output enable time to high level	R_L = 110 Ω, See Figure 4	$C_L = 50 \text{ pF},$			80	ns
tPZL	Output enable time to low level	R _L = 110 Ω , See Figure 5	$C_L = 50 \text{ pF},$			30	ns
t _{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4	$C_L = 50 \text{ pF},$			50	ns
^t PLZ	Output disable time from low level	R_L = 110 Ω, See Figure 5	C _L = 50 pF,			30	ns

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
Vo	V_{oa}, V_{ob}	V _{oa} , V _{ob}
IV _{OD1} I	Vo	V _O
IV _{OD2}	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
IV _{OD3} I	None	V _t (test termination measurement 2)
Δ V _{OD}	$ V_t - \overline{V}_t $	$ V_t - \overline{V}_t $
Voc	V _{os}	V _{os}
∆ VOC	$ V_{OS} - \overline{V}_{OS} $	$ V_{OS} - \overline{V}_{OS} $
los	I _{sa} , I _{sb}	None
I _O	I _{xa} , I _{xb}	l _{ia} , l _{ib}

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ Pulse skew is defined as the |tp_{LH} - tp_{HL}| of each channel of the same device.

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RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CO	NDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V,	$I_{O} = -0.4 \text{ mA}$			0.2	V
VIT-	Negative-going input threshold voltage	V _O = 0.5 V,	IO = 8 mA	-0.2‡			V
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT} –)				60		mV
VIK	Enable-input clamp voltage	$I_{I} = -18 \text{ mA}$				-1.5	V
Vон	High-level output voltage	V _{ID} = 200 mV, See Figure 6	$I_{OH} = -400 \mu A$	2.7			V
VOL	Low-level output voltage	V _{ID} = -200 mV, See Figure 6	I _{OL} = 8 mA,			0.45	V
loz	High-impedance-state output current	$V_0 = 0.4 \text{ V to } 2.4 \text{ V}$	V			±20	μΑ
M	Line input current	Other input = 0 V,	V _I = 12 V			1	mA
٧ _I	Line input current	See Note 5	V _I = -7 V			-0.8	mA
lіН	High-level-enable input current	V _{IH} = 2.7 V	-			20	μΑ
IJL	Low-level-enable input current	V _{IL} = 0.4 V				-100	μΑ
rį	Input resistance			12	20		kΩ
los	Short-circuit output current	V _{ID} = 200 mV,	V _O = 0	-15		-85	mA
laa	Cumply ourrent	Nolood	Outputs enabled		23	30	A
ICC	Supply current	No load	Outputs disabled		19	26	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

	PARAMETER	TEST COND	MIN	TYP†	MAX	UNIT	
t _{pd}	Propagation time	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$	C _L = 15 pF,			25	ns
t _{sk(p)}	Pulse skew§	See Figure 7			0	2	ns
^t PZH	Output enable time to high level				11	18	ns
tPZL	Output enable time to low level	C: 45 pF	Coo Figure 0		11	18	ns
^t PHZ	Output disable time from high level	C _L = 15 pF,	See Figure 8			50	ns
tPLZ	Output disable time from low level					30	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25°C.



[‡] The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

[§] Pulse skew is defined as the |tplH - tpHL| of each channel of the same device.

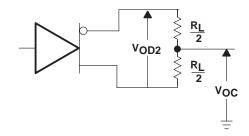


Figure 1. Driver V_{OD2} and V_{OC} Test Circuit

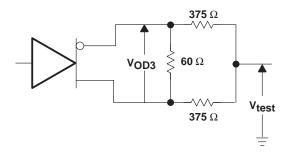
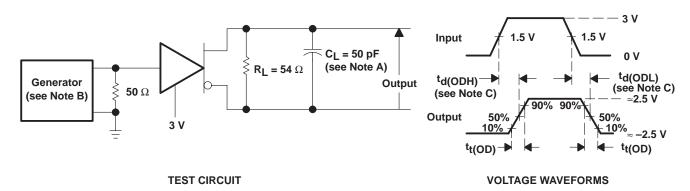


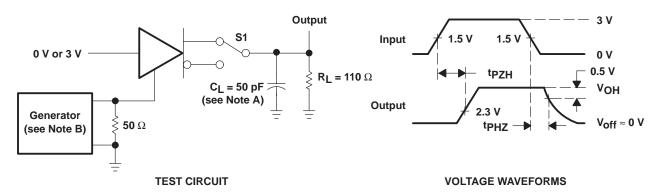
Figure 2. Driver $V_{\mbox{\scriptsize OD3}}$ Test Circuit



NOTES: A. C_L includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
- C. $t_{d(OD)} = t_{d(ODH)}$ or $t_{d(ODL)}$

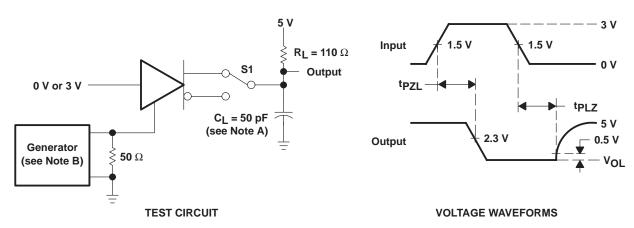
Figure 3. Driver Differential-Output Delay and Transition Times



NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns

Figure 4. Driver Enable and Disable Times



NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{O} = 50 \Omega$.

Figure 5. Driver Enable and Disable Times

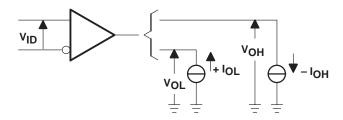
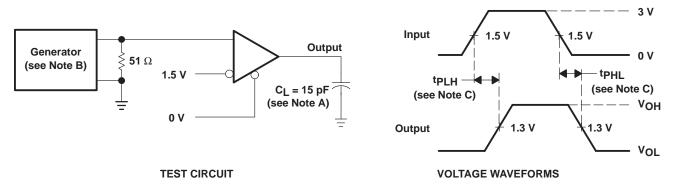


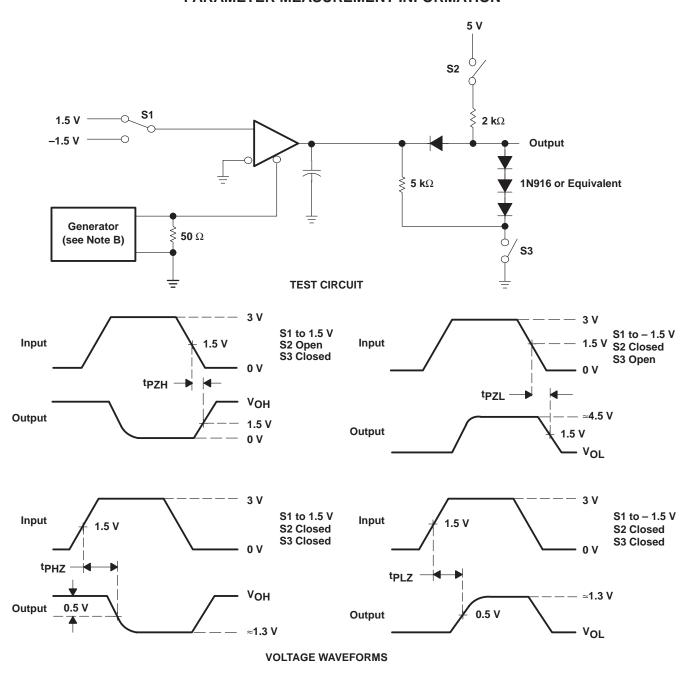
Figure 6. Receiver $V_{\mbox{OH}}$ and $V_{\mbox{OL}}$ Test Circuit



NOTES: A. C_L includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $T_{CO} = 50 \Omega$
- C. $t_{pd} = t_{PLH} \text{ or } t_{PHL}$

Figure 7. Receiver Propagation-Delay Times



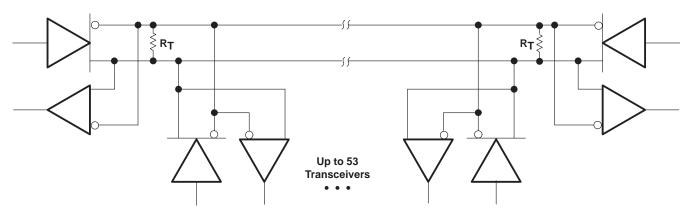
NOTES: A. $\,C_L\,$ includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns

Figure 8. Receiver Output Enable and Disable Times



APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 9. Typical Application Circuit



PACKAGE OPTION ADDENDUM

17-May-2014

PACKAGING INFORMATION

www.ti.com

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS1176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	Samples
SN65ALS1176DE4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-25 to 85		Samples
SN65ALS1176DG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-25 to 85		Samples
SN65ALS1176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	Samples
SN65ALS1176DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	Samples
SN65ALS1176DRG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-25 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Ph-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder humps used between the die and package, or 2) lead-based die adhesive used between

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

17-May-2014

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1





*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN65ALS1176DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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