CMOS Dual 8-Bit Buffered Multiplying DAC

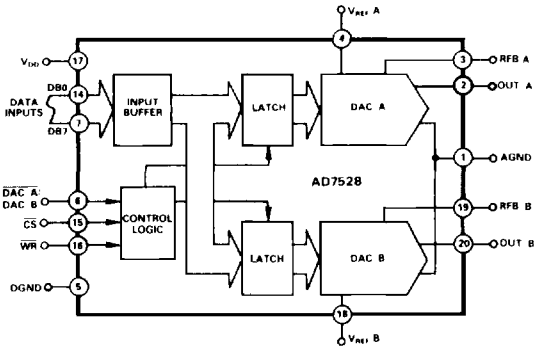
AD7528

FEATURES
- On-Chip Latches for Both DACs
- +5 V to +15 V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible
- Latch Free (Protection Schottkys not Required)

APPLICATIONS

Digital Control of:
- Gain/Attenuation
- Filter Parameters
- Stereo Audio Circuits
- X-Y Graphics

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5 V to +15 V power supply, dissipating only 20 mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin DIP, SOIC, PLCC or LCCC.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7528JN	-40°C to +85°C	±1 LSB	±4 LSB	N-20
AD7528KN	-40°C to +85°C	±1/2 LSB	±2 LSB	N-20
AD7528LN	-40°C to +85°C	±1/2 LSB	±1 LSB	N-20
AD7528JP	-40°C to +85°C	±1 LSB	±4 LSB	P-20A
AD7528KP	-40°C to +85°C	±1/2 LSB	±2 LSB	P-20A
AD7528LP	-40°C to +85°C	±1/2 LSB	±1 LSB	P-20A
AD7528JR	-40°C to +85°C	±1 LSB	±4 LSB	R-20
AD7528KR	-40°C to +85°C	±1/2 LSB	±2 LSB	R-20
AD7528LR	-40°C to +85°C	±1/2 LSB	±1 LSB	R-20
AD7528AQ	-40°C to +85°C	±1 LSB	±4 LSB	Q-20
AD7528BQ	-40°C to +85°C	±1/2 LSB	±2 LSB	Q-20
AD7528CQ	-40°C to +85°C	±1/2 LSB	±1 LSB	Q-20
AD7528SQ	-55°C to +125°C	±1 LSB	±4 LSB	Q-20
AD7528TQ	-55°C to +125°C	±1/2 LSB	±2 LSB	Q-20
AD7528UQ	-55°C to +125°C	±1/2 LSB	±1 LSB	Q-20
AD7528SE	-55°C to +125°C	±1 LSB	±4 LSB	E-20A
AD7528TE	-55°C to +125°C	±1/2 LSB	±2 LSB	E-20A
AD7528UE	-55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

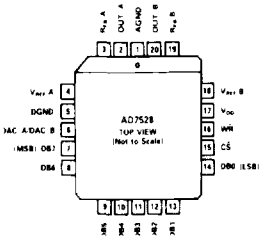
NOTES

[1]Analog Devices reserves the right to ship side-brazed ceramic in lieu of cerdip. Parts will be marked with cerdip designator "Q."

[2]Processing to MIL-STD-883C, Class B is available. To order, add suffix "/883B" to part number. For further information, see Analog Devices' 1990 Military Products Databook.

[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

DIP, SOIC



AD7528–SPECIFICATIONS (V_{REF} A = V_{REF} B = +10 V; OUT A = OUT B = 0 V unless otherwise noted)

Parameter	Version[1]	V_{DD} = +5 V		V_{DD} = +15 V		Units	Test Conditions/Comments
		T_A = +25°C	T_{MIN}, T_{MAX}	T_A = +25°C	T_{MIN}, T_{MAX}		
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±1/2	±1/2	±1/2	±1/2	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5
Gain Temperature Coefficient[3]							
ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF}A, V_{REF}B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300 ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11 kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[1]							
Input High Voltage, V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage, V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current, I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
WR, CS, DAC A/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time, t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time, t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time, t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time, t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time, t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time, t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width, t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA max	All Digital Inputs 0 V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended PC Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5 V		V_{DD} = +15 V		Units	Test Conditions/Comments
		T_A = +25°C	T_{MIN}, T_{MAX}	T_A = +25°C	T_{MIN}, T_{MAX}		
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2 LSB. Out A/Out B Load = 100 Ω. $\overline{WR}$ = $\overline{CS}$ = 0 V. DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10 V. OUT A, OUT B Load = 100 Ω C_{EXT} = 13 pF. $\overline{WR}$ = $\overline{CS}$ = 0 V. DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	160		440		nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT}A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT}B		50	50	50	50	pF max	
C_{OUT}A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT}B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	70	65	70	65	dB max	V_{REF} A, V_{REF} B = 20 V p-p Sine Wave
V_{REF} B to OUT B		70	65	70	65	dB max	@ 100 kHz
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF}A to OUT B	All	77		77		dB typ	V_{REF}A = 20 V p-p Sine Wave @ 100 kHz. V_{REF}B = 0 V. See Figure 6.
V_{REF} B to OUT A		77		77		dB typ	V_{REF}A = 20 V p-p Sine Wave @ 100 kHz. V_{REF}A = 0 V. See Figure 6.
DIGITAL CROSSTALK	All	90		60		nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	85		85		dB typ	V_{IN} = 6 V rms @ 1 kHz

NOTES

[1]Temperature Ranges are J, K, L: −40°C to +85°C
A, B, C: −40°C to +85°C
S, T, U: −55°C to +125°C

[2]Specification applies to both DACs in AD7528.

[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1 nA.

[4]Guaranteed by design but not production tested.

[5]These characteristics are for design guidance only and are not subject to test.

[6]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.