Integrated Device Technology, Inc.

FAST CMOS 16-BIT INVERTING BUS TRANSCEIVER/REGISTER

IDT54/74FCT16651T/AT/CT/ET

FEATURES:

- 0.5 MICRON CMOS Technology
- **High-speed, low-power CMOS replacement for ABT functions**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤ 1μA max.**
- High drive outputs (–32mA I_{OH}, 64mA I_{OL})
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of –40°C to +85°C V_{CC} = 5V ±10%

DESCRIPTION:

The IDT54/74FCT16651T/AT/CT/ET 16-bit inverting registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit inverting bus transceivers with 3-state D-type registers. For example, the xOEAB and $x\overline{OEBA}$ signals control the transceiver functions. The xSAB and xSBA control pins select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A LOW input level selects real-time data and a HIGH level selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (xCLKAB or xCLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16651T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT16651T/AT/CT/ET are plug-in replacements for the 54/74ABT16651 in bus and backplane interface applications.

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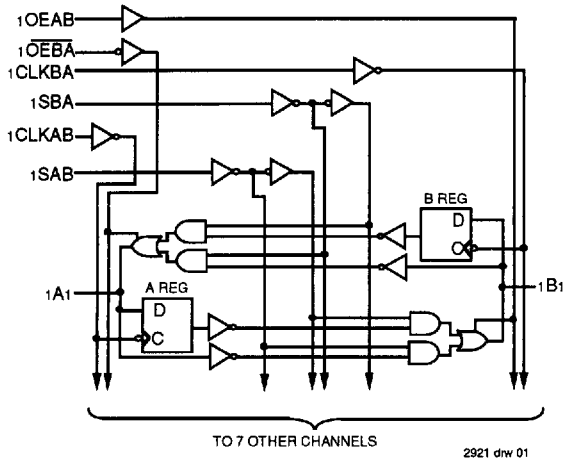
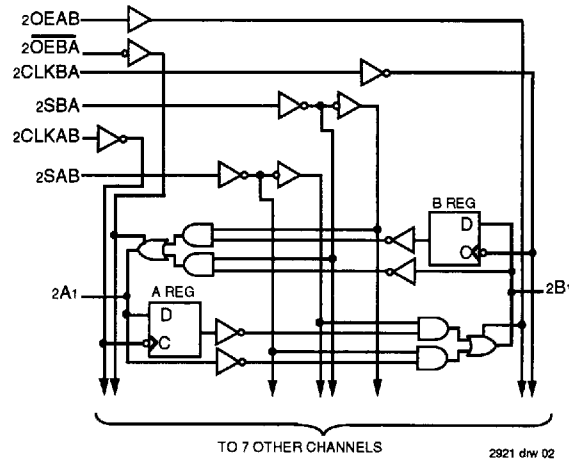
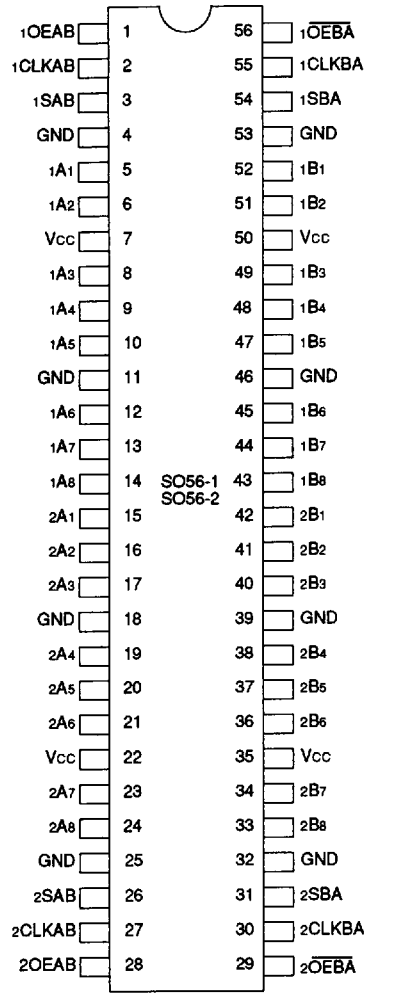
FUNCTIONAL BLOCK DIAGRAM

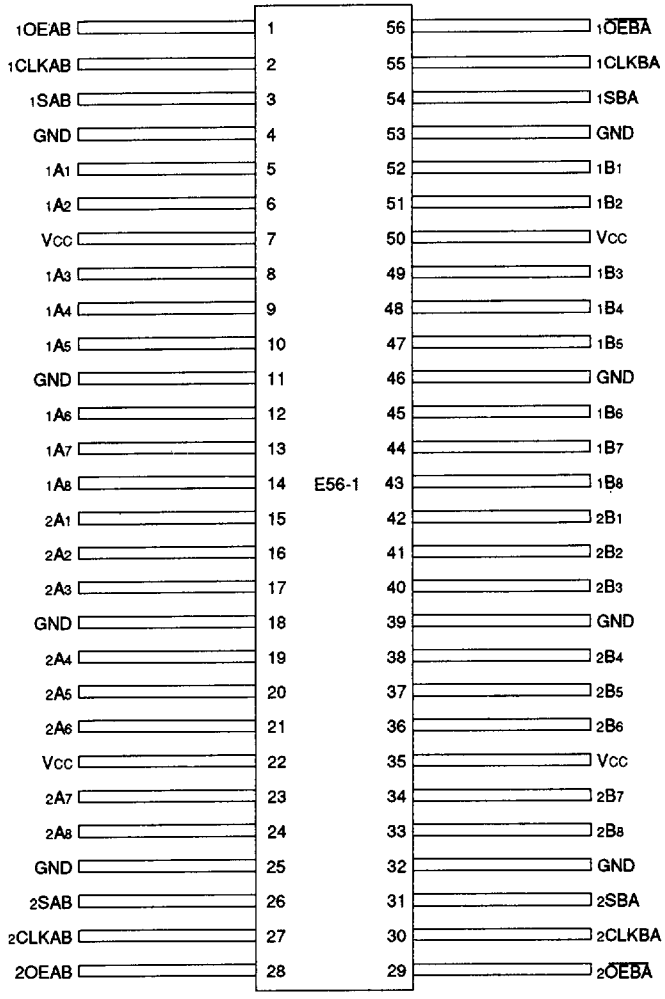




PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW



CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, x$\overline{OEBA}$	Output Enable Inputs

2921 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2921 lnk 02
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(3)

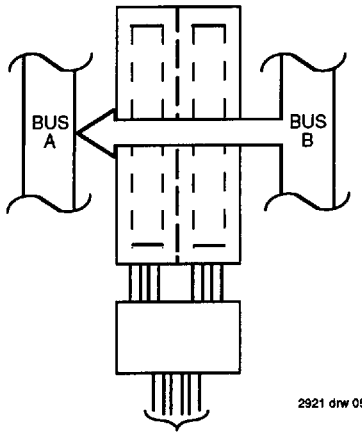
Inputs						Data I/O(1)		Operation or Function
xOEAB	x$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified(1)	Store A, Hold B
H	H	↑	↑	X(2)	X	Input	Output	Store A in Both Registers(4)
L	X	H or L	↑	X	X	Unspecified(1)	Input	Hold A, Store B
L	L	↑	↑	X	X(2)	Output	Input	Store B in both Registers(5)
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus

NOTES: 2921 tbl 03
1. The data output functions may be enabled or disabled by various signals at the xOEAB or x$\overline{OEBA}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L, clocks can occur simultaneously.
   Select control = H, clocks must be staggered in order to load both registers.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
4. $\overline{A}$ in B register
5. $\overline{B}$ in A register

ABSOLUTE MAXIMUM RATINGS(1)

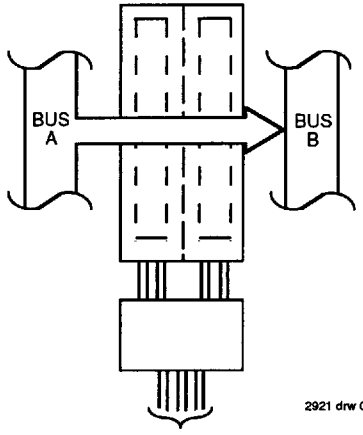
Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2921 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.



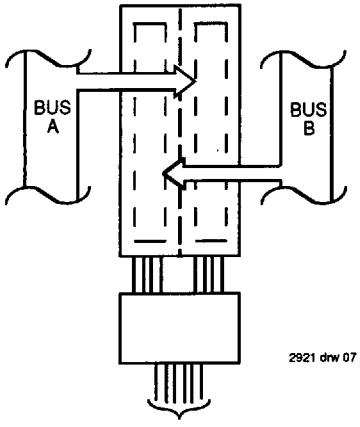
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



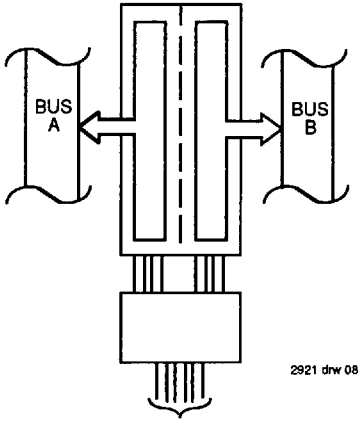
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

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DC OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2921 lnk 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOEAB = $\overline{xOEBA}$=GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		xOEAB = $\overline{xOEBA}$=GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		xOEAB = $\overline{xOEBA}$=GND Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2921 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16651T				FCT16651AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time, HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

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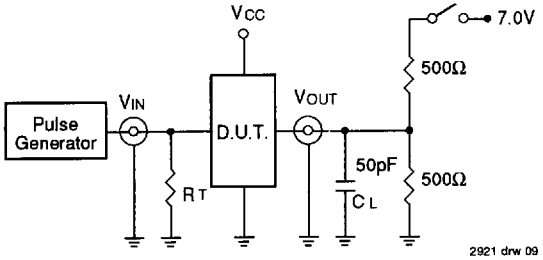
Symbol	Parameter	Condition[1]	FCT16651CT				FCT16651ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
tSU	Set-up Time, HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
tW	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2921 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2921 drw 09

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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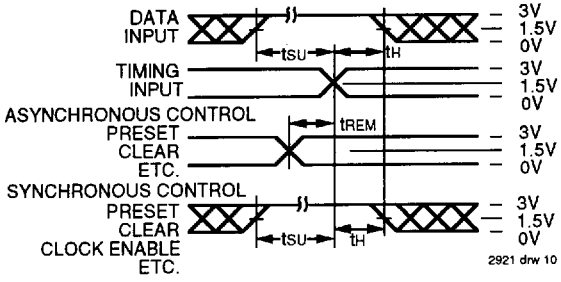
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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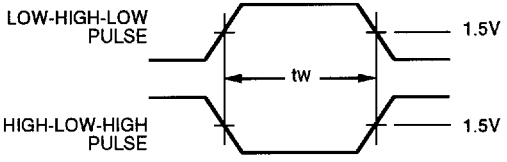
PULSE WIDTH



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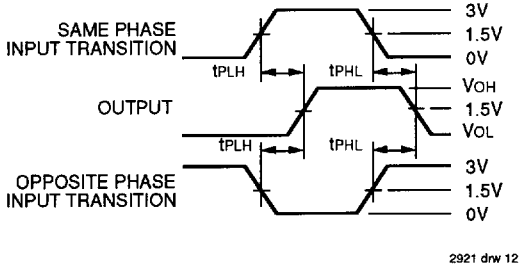
PROPAGATION DELAY



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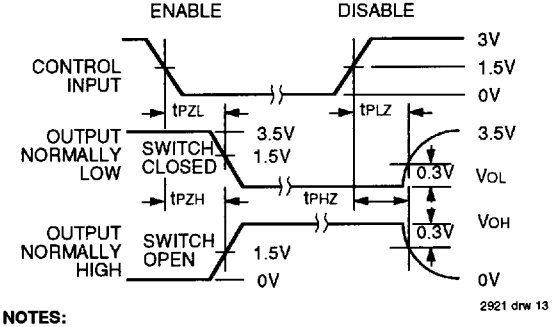
ENABLE AND DISABLE TIMES



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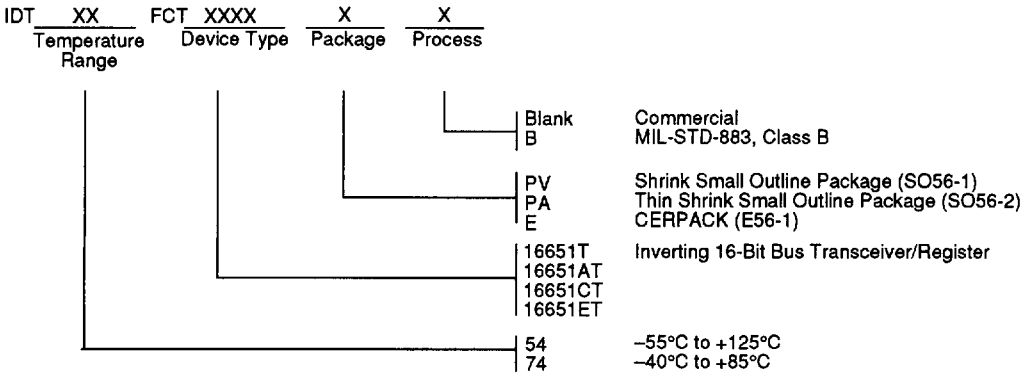
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2921 drw 14

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