HARRIS SEMICONDUCTOR
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AD7520/AD7530 AD7521/AD7531 10/12-Bit Multiplying D/A Converters

GENERAL DESCRIPTION

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Harris' thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

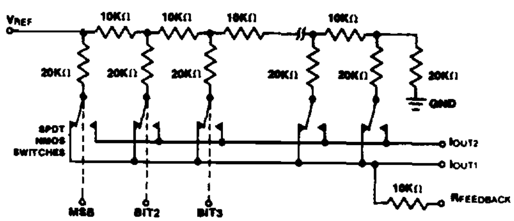
The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications,

FEATURES

- **AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20mW (Max)**
- **Low Nonlinearity Tempco: 2 ppm of FSR/°C**
- **Current Settling Time: 500ns to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **TTL/CMOS Compatible**
- **Full Input Static Protection**
- **/883B Processed Versions Available**

ORDERING INFORMATION

Nonlinearity	Part Number/Package		
	Plastic DIP	CERDIP	CERDIP
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD	AD7520SD AD7520SD/883B AD7521SD/883B
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD	AD7520TD AD7520TD/883B
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD	AD7520UD AD7520UD/883B
TEMPERATURE RANGE	0°C to +70°C	−25°C to +85°C	−55°C to +125°C



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(Switches shown for Digital Inputs "High")
(Resistor values are nominal)
Figure 1: Functional Diagram

300105-004

NOTE: All typical values have been characterized but are not tested.

AD7520/AD7530/AD7521/AD7531

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Supply Voltage (V+) .... +17V
V_{REF} .... ±25V
Digital Input Voltage Range .... V+ to GND
Output Voltage Compliance .... −100mV to V+
Power Dissipation (package)
up to +75°C 450mW
derate above +75°C @ .... 6mW/°C

Operating Temperature
JN, KN, LN Versions .... 0°C to +70°C
JD, KD, LD Versions .... −25°C to 85°C
SD, TD, UD Versions .... −55°C to +125°C
Storage Temperature .... −65°C to 150°C
Lead Temperature (Soldering, 10sec) .... 300°C

CAUTION:

1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and $R_{FEEDBACK}$.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

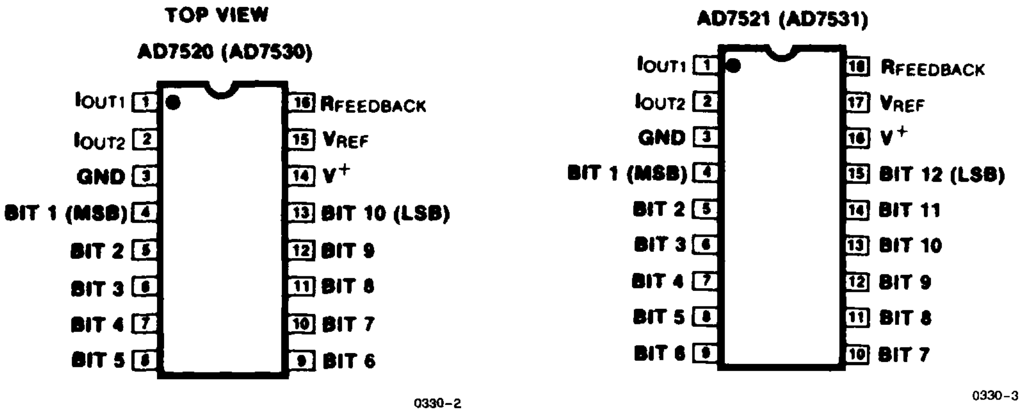

Figure 2: Pin Configurations

ELECTRICAL CHARACTERISTICS ($V+ = +15V$, $V_{REF} = +10V$, $T_A = 25°C$ unless otherwise specified)

Parameter			Test Conditions		AD7520 (AD7530)	AD7521 (AD7531)	Unit	Limit
DC ACCURACY (Note 1)								
Resolution					10	12	Bits	
Nonlinearity (Note 2)	VERSION	J S	S, T, U: over −55°C to +125°C	Fig. 3	±0.2 (8-Bit)		% of FSR	Max
		K T		Fig. 3	±0.1 (9-Bit)		% of FSR	Max
		L U	$-10V \leq V_{REF} \leq +10V$	Fig. 3	±0.05 (10-Bit)		% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)			$-10V \leq V_{REF} \leq +10V$		±2		ppm of FSR/°C	Max
Gain Error (Note 2)					±0.3		% of FSR	Typ
Gain Error Tempco (Notes 2 and 3)					±10		ppm of FSR/°C	Max

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V_{REF} = +10V$, $T_A = 25°C$ unless otherwise specified) (Continued)

Parameter	Test Conditions		AD7520 (AD7530)	AD7521 (AD7531)	Unit	Limit
Output Leakage Current (either output)	Over the specified temperature range		±200 (±300)		nA	Max
Power Supply Rejection (Note 2)		Fig. 4	±0.005		% FSR/% ΔV^+	Typ
AC ACCURACY (Note 3)						
Output Current Settling Time	To 0.05% of FSR (All digital inputs low to high and high to low)	Fig. 8	500		ns	Typ
Feedthrough Error	V_{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	Fig. 7	10		mV pp	Max
REFERENCE INPUT						
Input Resistance	All digital inputs high I_{OUT1} at ground.		5k 10k 20k		Ω	Min Typ Max
ANALOG OUTPUT						
Voltage Compliance (both outputs)	(Note 3)		See absolute max. ratings			
Output Capacitance (Note 3) I_{OUT1} I_{OUT2}	All digital inputs high	Fig. 6	120 37		pF pF	Typ Typ
I_{OUT1} I_{OUT2}	All digital inputs low	Fig. 6	37 120		pF pF	Typ Typ
Output Noise (both outputs) (Note 3)		Fig. 5	Equivalent to 10kΩ Johnson noise			Typ
DIGITAL INPUTS						
Low State Threshold	Over the specified temp range		0.8		V	Max
High State Threshold			2.4		V	Min
Input Current (V_{IN} = 0V or +15V)			±1		μA	Max
Input Coding	See Tables 1 & 2		Binary/Offset Binary			
POWER REQUIREMENTS						
Power Supply Voltage Range			+5 to +15		V	
I^+ (Excluding Ladder Network)	All digital inputs at 0V or V^+		±1		μA	Typ
	All digital inputs high or low		2		mA	Max
Total Power Dissipation (Including the ladder network)			20		mW	Typ

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design, not subject to test.
4. Accuracy not guaranteed unless outputs at GND potential.

NOTE. All typical values have been characterized but are not tested.

TEST CIRCUITS

NOTE: The following test circuits apply for the AD7520. Similar circuits are used for the AD7530, AD7521 and AD7531.

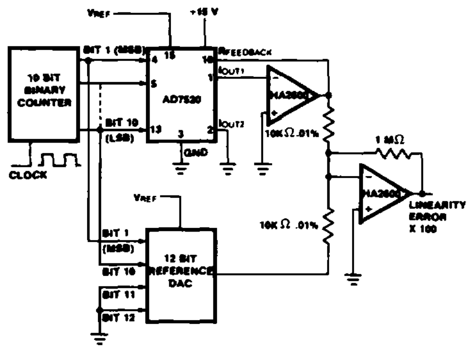

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Figure 3: Nonlinearity

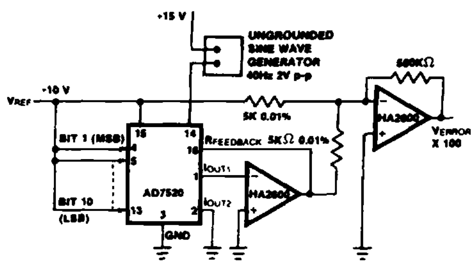

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Figure 4: Power Supply Rejection

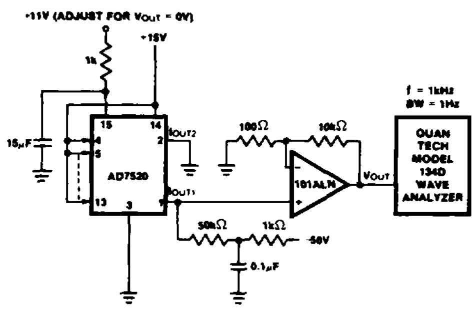

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Figure 5: Noise

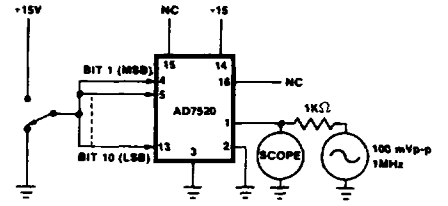

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Figure 6: Output Capacitance

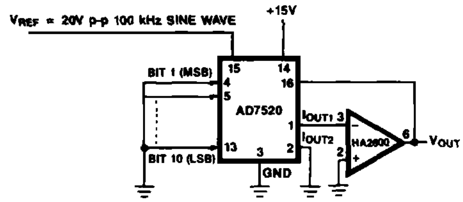

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Figure 7: Feedthrough Error

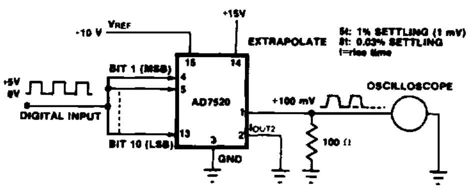

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Figure 8: Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

RESOLUTION: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-n} of the full-scale range, e.g. 2^{-n} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

SETTLING TIME: Time required for the output of a DAC to settle to within specified error band around its final value (e.g. ½ LSB) for a given digital input change, i.e. all digital inputs LOW to HIGH and HIGH to LOW.

GAIN ERROR: The difference between actual and ideal analog output values at full-scale range, i.e. all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

NOTE: All typical values have been characterized but are not tested.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

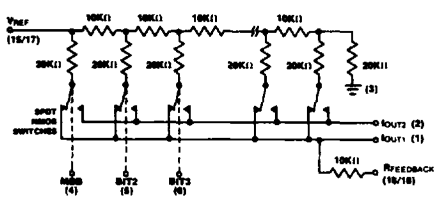
OUTPUT CAPACITANCE: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

DETAILED DESCRIPTION

The AD7520, AD7530, AD7521 and AD7531 are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held either at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



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(Switches shown for Digital Inputs "High")

Figure 9: AD7520/21/30/31 Functional Diagram

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 10). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

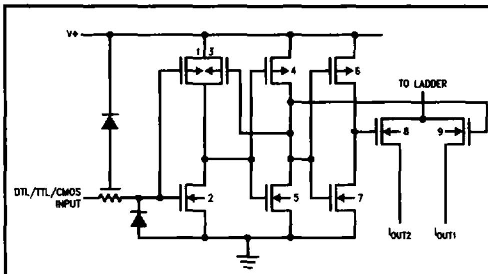

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Figure 10: CMOS Switch

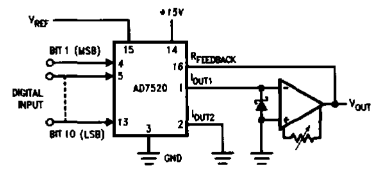

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Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

TABLE 1
CODE TABLE — UNIPOLAR BINARY OPERATION

Digital Input	Analog Output
1111111111	$-V_{REF}(1-2^{-n})$
1000000001	$-V_{REF}(1/2+2^{-n})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}(1/2-2^{-n})$
0000000001	$-V_{REF}(2^{-n})$
0000000000	0

NOTE: 1. LSB $=2^{-n}$ V_{REF}
2. n = 10 for 7520, 7530
n = 12 for 7521, 7531

APPLICATIONS

Unipolar Binary Operation

The circuit configuration for operating the AD7520 in unipolar mode is shown in Figure 11. Similar circuits can be used for AD7521, AD7530 and AD7531. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

NOTE: All typical values have been characterized but are not tested.

ZERO OFFSET ADJUSTMENT

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1\text{-}2^{-n})$ reading. (n = 10 for AD7520/30 and n = 12 for AD7521/31).
3. To decrease V_{OUT}, connect a series resistor (0 to 250Ω) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 250Ω) in the I_{OUT1} amplifier feedback loop.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7520 in the bipolar mode is given in Figure 12. Similar circuits can be used for AD7521, AD7530 and AD7531. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

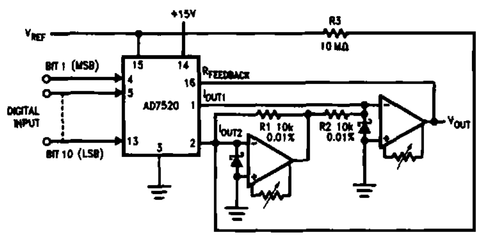

Figure 12: Bipolar Operation (4-Quadrant Multiplication)

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\,(1-2^{-(n-1)})$
1000000001	$-V_{REF}\,(2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}\,(2^{-(n-1)})$
0000000001	$V_{REF}\,(1-2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. $LSB = 2^{-(n-1)}\,V_{REF}$
2. n = 10 for 7520 and 7521
= 12 for 7530 and 7531

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2}.

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1 mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1\text{-}2^{-(n-1)})$ volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor of up to 250Ω between the reference voltage and the V_{REF} terminal.

NOTE: All typical values have been characterized but are not tested.

Analog/Digital Division

With the AD7520 connected in its normal multiplying configuration as shown in Figure 11, the transfer function is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 13, the transfer function becomes:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

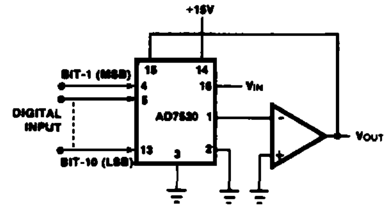

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Figure 13: Analog/Digital Divider

For further information on the use of this device, see the following Application Bulletins:

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A002 "Principles of Data Acquisition and Conversion".

A042 "Interpretation of Data Converter Accuracy Specifications".

NOTE: All typical values have been characterized but are not tested.