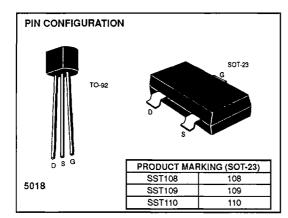
# N-Channel JFET Switch



## J108 - J110 / SST108 - SST110

#### **FEATURES**

- Low Cost
- · Automated Insertion Package
- Low Insertion Loss
- . No Offset or Error Voltages Generated by Closed Switch **Purely Resistive**
- High Isolation Resistance from Driver
- Fast Switching
- Low Noise



#### **APPLICATIONS**

- Analog Switches
- Choppers
- Commutators
- . Low-Noise Audio Ampliflers

## **ABSOLUTE MAXIMUM RATINGS**

(T<sub>A</sub> = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage	25V
Gate Current	
Storage Temperature Range55°C to +	150°C
Operating Temperature Range55°C to +	135°C
Lead Temperature (Soldering, 10sec) +	300°C
Power Dissipation	60mW
Derate above 25°C	nW/ºC

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING INFORMATION

Part	Package Package	Temperature Range
J108-110	Plastic TO-92	-55°C to +135°C
XJ108-110	Sorted Chips in Carriers	-55°C to +135°C
SST109-110	Plastic SOT-23	-55°C to +135°C

### ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise specified)

SYMBOL	PARAMETER	108		109		110		UNITS	TEGT COMPITIONS				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
lgss	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V <sub>DS</sub> = 0V, V <sub>GS</sub> = -15V	
VGS(off)	Gate-Source Cutoff Voltage	-3		-10	-2		-6	-0.5		-4	ν	V <sub>DS</sub> = 5V, I <sub>D</sub> = 1μA	
BVgss	Gate-Source Breakdown Voltage	-25			-25			-25			1 °	V <sub>DS</sub> = 0V, I <sub>G</sub> = -1μA	
loss	Drain Saturation Current (Note 2)	80			40			10			mA	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V	
D(off)	Drain Cutoff Current (Note 1)			3	-		3			3	nΑ	V <sub>DS</sub> = 5V, V <sub>GS</sub> = -10V	
rDS(on)	Drain-Source ON Resistance			8			12			18	Ω	V <sub>DS</sub> ≤0.1V, V <sub>GS</sub> = 0V	
Cdg(off)	Drain-Gate OFF Capacitance			15			15			15	pF	V <sub>DS</sub> = 0,	
C <sub>sg(off)</sub>	Source-Gate OFF Capacitance			15			15			15		Vgs = -10V (Note 3) f = 1MHz	
C <sub>dg(on)</sub> + C <sub>sg(on)</sub>	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85		V <sub>DS</sub> = V <sub>GS</sub> = 0 (Note 3)	
td(on)	Turn On Delay Time		4			4			4			Switching Time Test	
tr	Rise Time		1			1			1		ns	Conditions (Note 3) J107 J109 J110 VDD 1.5V 1.5V 1.5V	
td(off)	Turn OFF Delay Time		6			6			6				
t <sub>f</sub>	Fall Time		30			30			30			$V_{GS(off)}$ -12V -7V -5V $R_L$ 150Ω 150Ω 150Ω	

NOTES: 1. Approximately doubles for every 10°C increase in T<sub>A</sub>.
2. Pulse test duration = 300µs; duty cycle ≤3%.
3. For design reference only, not 100% tested.