T-46-07-11

National Semiconductor

100344
Low Power 8-Bit Latch with Cut-Off Drivers

General Description

The 100344 contains eight D-type latches, individual inputs (D_n), outputs (Q_n), a common enable pin ($\overline{E}$), latch enable ($\overline{LE}$), and output enable pin ($\overline{OEN}$). A Q output follows its D input when both $\overline{E}$ and $\overline{LE}$ are LOW. When either $\overline{E}$ or $\overline{LE}$ (or both) are HIGH, a latch stores the last valid data present on its D input prior to $\overline{E}$ or $\overline{LE}$ going HIGH.

A HIGH on $\overline{OEN}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

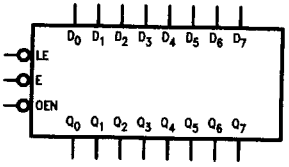
The 100344 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have 50 kΩ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol



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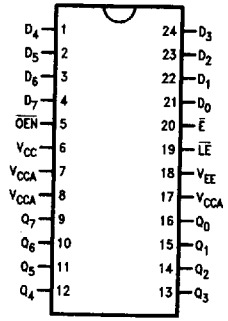
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{E}$	Enable Input
$\overline{LE}$	Latch Enable Input
$\overline{OEN}$	Output Enable Input
Q_0–Q_7	Data Outputs

Connection Diagrams

24-Pin DIP



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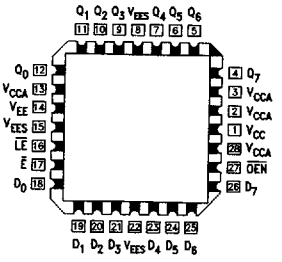
28-Pin PCC



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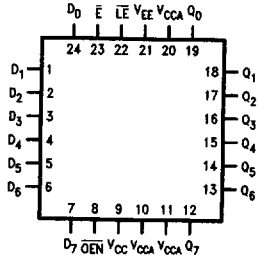
24-Pin Quad Cerpak



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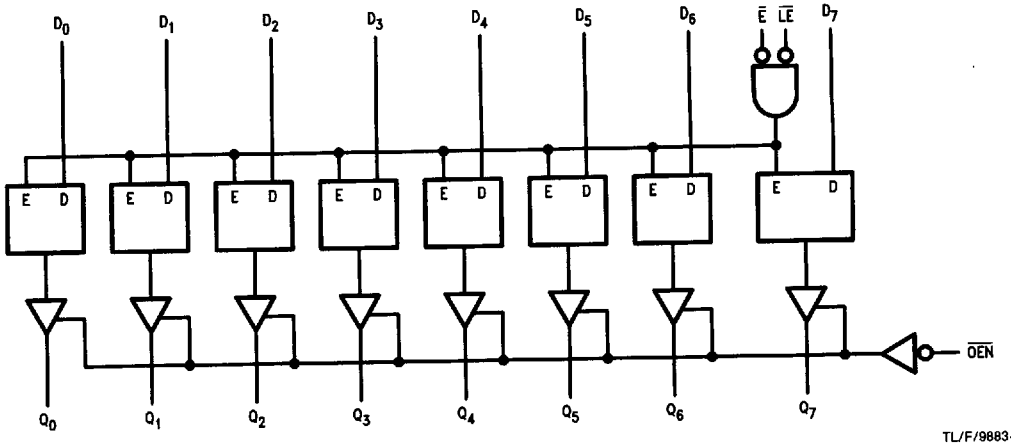
Logic Diagram



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Truth Table

Inputs				Outputs
D_n	$\overline{E}$	$\overline{LE}$	$\overline{OEN}$	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched*
X	X	H	L	Latched*
X	X	X	H	Cutoff

*Retains data present before either $\overline{LE}$ or $\overline{E}$ go HIGH.

H = HIGH Voltage level
L = LOW Voltage level
Cutoff = lower-than-LOW state
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 25Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{OLZ}	Cutoff LOW Voltage			−1950	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−178 −185		−85 −85	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.90	2.10	0.90	2.10	1.00	2.30	ns	*Figures 1, 2* (Note 1)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.60	3.10	1.60	3.10	1.80	3.40	ns	*Figures 1, 4* (Note 1)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.20 2.70	1.60 1.00	4.20 2.70	1.60 1.00	4.20 2.70	ns	*Figures 1, 2* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1, 3*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

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Commercial Version (Continued)

DIP AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_S	Setup Time D_0–D_7	1.00		1.00		1.10		ns	*Figures 1, 3*
t_H	Hold Time D_0–D_7	0.10		0.10		0.10		ns	*Figures 1, 3*
$t_{pw}(H)$	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	*Figures 1, 3*

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.90	1.90	0.90	1.90	1.00	2.10	ns	*Figures 1, 2* (Note 2)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.60	2.90	1.60	2.90	1.80	3.20	ns	*Figures 1, 4* (Note 2)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	ns	*Figures 1, 2* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 3*
t_S	Setup Time D_0–D_7	0.90		0.90		1.00		ns	*Figures 1, 3*
t_H	Hold Time D_0–D_7	0.00		0.00		0.00		ns	*Figures 1, 3*
$t_{pw}(H)$	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	*Figures 1, 3*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		230		230		230	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 25Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 25Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{OLZ}	Cutoff LOW Voltage		−1950	mV	0°C to +125°C	V_{IN} = V_{IH} (MIN) or V_{IL} (Max)	$\overline{OEN}$ = HIGH	1, 2, 3
			−1850		−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
			340	μA	−55°C			
I_{EE}	Power Supply Current	−195 −205	−65 −65	mA	−55°C to +125°C	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

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Military Version (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.50	2.60	0.70	2.60	0.70	3.10	ns	*Figures 1, 2*	1, 2, 3, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	0.80	3.30	1.00	3.30	1.10	3.80	ns	*Figures 1, 4*	1, 2, 3, 5
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.00 0.70	4.60 3.00	1.10 0.70	4.20 2.80	1.20 0.70	4.40 3.20	ns	*Figures 1, 2*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns	*Figures 1, 3*	4
t_s	Setup Time D_0–D_7	1.50		1.50		1.70		ns	*Figures 1, 3*	4
t_h	Hold Time D_0–D_7	0.60		0.60		0.60		ns	*Figures 1, 3*	4
t_{pw}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.40		2.40		2.40		ns	*Figures 1, 3*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

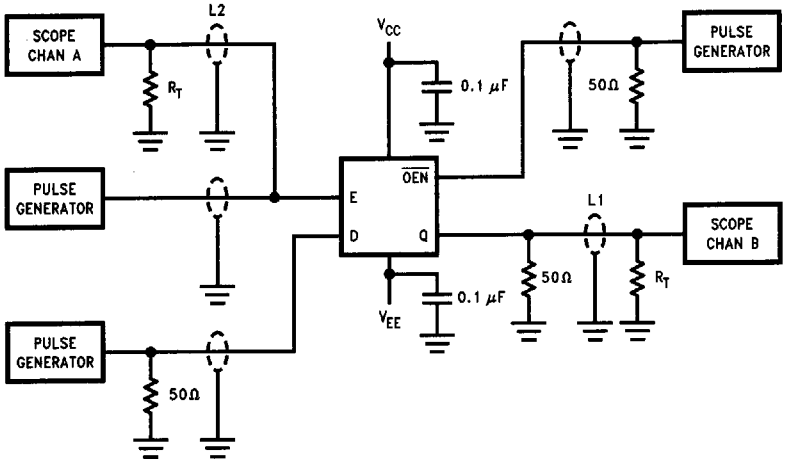

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FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms

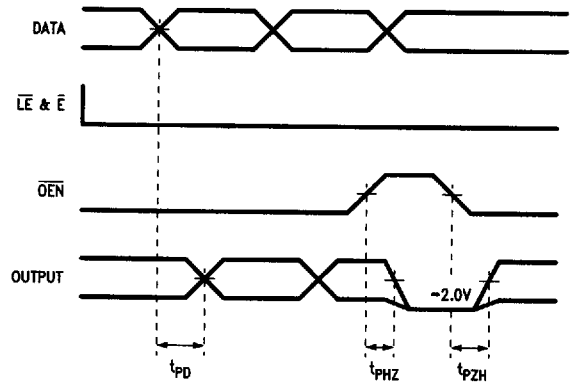

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FIGURE 2. Propagation Delay and Cutoff Times

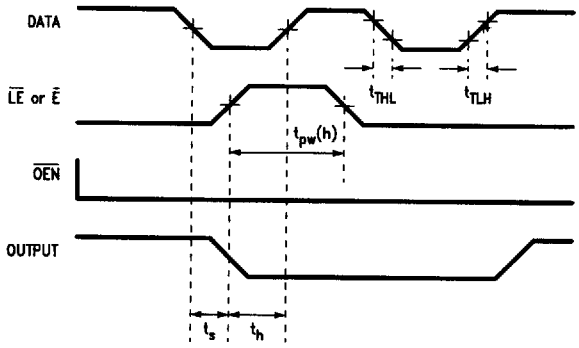

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FIGURE 3. Setup, Hold and Pulse Width Times

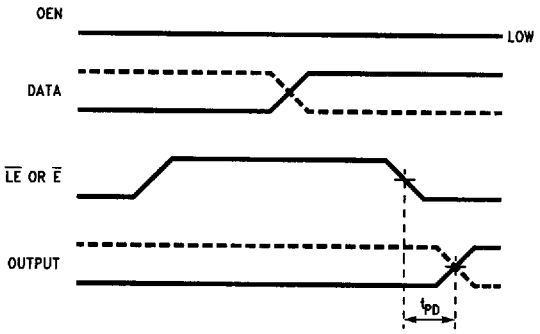

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FIGURE 4. Propagation Delay $\overline{LE}$, $\overline{E}$ to Q

2