

## 54AC/74AC74 • 54ACT/74ACT74

### Dual D-Type Positive Edge-Triggered Flip-Flop

#### Description

The 'AC/ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

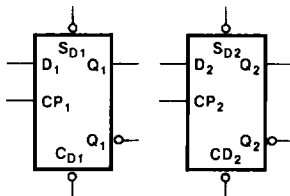
#### Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

- Outputs Source/Sink 24 mA
- 'ACT74 has TTL-Compatible Inputs

**Ordering Code:** See Section 6

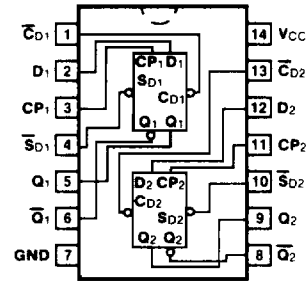
#### Logic Symbol



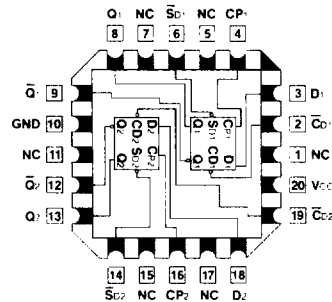
#### Pin Names

- D<sub>1</sub>, D<sub>2</sub> Data Inputs
- CP<sub>1</sub>, CP<sub>2</sub> Clock Pulse Inputs
- $\bar{C}_D$ <sub>1</sub>,  $\bar{C}_D$ <sub>2</sub> Direct Clear Inputs
- $\bar{S}_D$ <sub>1</sub>,  $\bar{S}_D$ <sub>2</sub> Direct Set Inputs
- Q<sub>1</sub>,  $\bar{Q}_1$ , Q<sub>2</sub>,  $\bar{Q}_2$  Outputs

#### Connection Diagrams



#### Pin Assignment for DIP, Flatpak and SOIC



#### Pin Assignment for LCC

#### Truth Table (Each Half)

Inputs				Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	J	H	H	L
H	H	J	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

H = HIGH Voltage Level

L = LOW Voltage Level

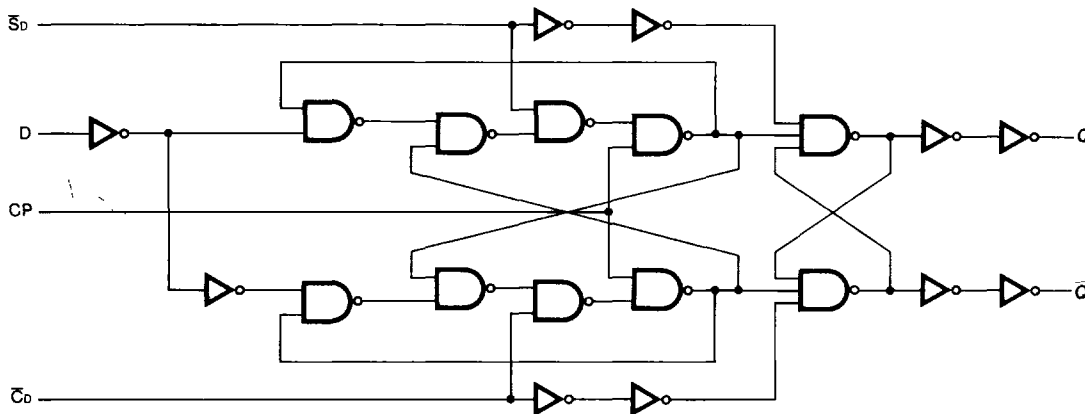
X = Immaterial

J = LOW-to-HIGH Clock Transition

Q<sub>0</sub>( $\bar{Q}_0$ ) = Previous Q( $\bar{Q}$ ) before

LOW-to-HIGH Transition of Clock

**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**DC Characteristics** (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
$I_{CC}$	Maximum Quiescent Supply Current	80	40	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$ , $T_A = \text{Worst Case}$
$I_{CC}$	Maximum Quiescent Supply Current	4.0	4.0	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$ , $T_A = 25^\circ C$
$I_{CC(T)}$	Maximum Additional $I_{CC}$ /Input ('ACT74)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$ $V_{CC} = 5.5 V$ , $T_A = \text{Worst Case}$

# AC74 • ACT74

## AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	100 140	125 160		95 95		95 125	MHz	3-3	
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	8.0 6.0	12.0 9.0	1.0 1.0	14.5 10.5	1.0 1.0	13.0 10.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	10.5 8.0	12.0 9.5	1.0 1.0	20.0 14.5	1.0 1.0	13.5 10.5	ns	3-6
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10.0	1.0 1.0	17.5 11.0	1.0 1.0	16.0 10.5	ns	3-6
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	8.0 6.0	14.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.5	ns	3-6

\*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
t <sub>s</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3 5.0	1.5 1.0	4.0 3.0		5.0 3.5		4.5 3.0	ns	3-9
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	3.3 5.0	-2.0 -1.5	0 0		0.5 0.5		0 0	ns	3-9
t <sub>w</sub>	CP <sub>n</sub> or C̄ <sub>Dn</sub> or S̄ <sub>Dn</sub> Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5		8.0 5.5		7.0 5.0	ns	3-6
t <sub>rec</sub>	Recovery Time C̄ <sub>Dn</sub> or S̄ <sub>Dn</sub> to CP	3.3 5.0	-2.5 -2.0	0 0		0.5 0.5		0 0	ns	3-9

\*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	145	210		95		125	MHz	3-3	
t <sub>PLH</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	5.0	1.0	5.5 6.5	9.5	1.0	11.5 12.8	1.0 11.8	ns	3-6	
t <sub>PHL</sub>	Propagation Delay C <sub>Dn</sub> or S <sub>Dn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	5.0	1.0	6.0	10.0	1.0	12.5 12.3	1.0 11.5	ns	3-6	
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	5.0	1.0	7.5 6.5	11.0	1.0	14.0 12.8	1.0 14.8	ns	3-6	
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	5.0	1.0	6.0	10.0	1.0	12.0 12.1	1.0 11.5	ns	3-6	

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		54ACT		74ACT		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Typ	Guaranteed Minimum						
t <sub>s</sub>	Set-up Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	1.0	3.0		4.0		3.5	ns	3-9
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP <sub>n</sub>	5.0	-0.5	1.0		1.0		1.0	ns	3-9
t <sub>w</sub>	CP <sub>n</sub> or C <sub>Dn</sub> or S <sub>Dn</sub> Pulse Width	5.0	3.0	5.0		6.5		6.0	ns	3-6
t <sub>rec</sub>	Recovery Time C <sub>Dn</sub> or S <sub>Dn</sub> to CP	5.0	-2.5	0		0		0	ns	3-9

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

## Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.5 V
C <sub>PD</sub>	Power Dissipation Capacitance	35.0	pF	V <sub>CC</sub> = 5.5 V