Integrated Device Technology, Inc.

# CMOS STATIC RAMs 64K (16K x 4-BIT) Added Chip Select and Output Controls

**IDT7198S**
**IDT7198L**

## FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS_1}$, $\overline{CS_2}$) simplify system design and operation
- High speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier, 24-pin SOJ and CERPACK
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

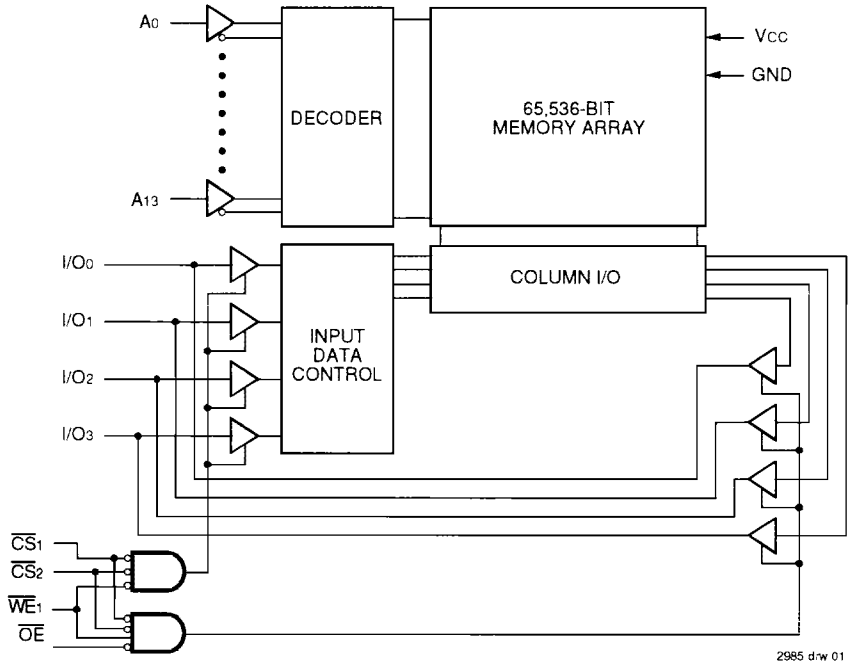
Access times as fast as 15ns are available. The IDT7198 offers a reduced power standby mode, $I_{SB1}$, which is activated when $\overline{CS_1}$ or $\overline{CS_2}$ goes high. This capability decreases power, while enhancing system reliability. The low-power version (L)also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 24-pin plastic DIP, 28-pin leadless chip carrier, 24-pin SOJ and 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM



## MEMORY CONTROL

The IDT7198 64K high-speed CEMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

The dual chip select feature ($\overline{CS}_1$, $\overline{CS}_2$) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding.

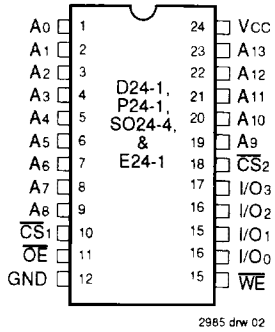
Both chip selects, Chip Select 1 ($\overline{CS}_1$) and Chip Select 2 ($\overline{CS}_2$), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

## PIN DESCRIPTIONS

| Name | Description |
|---|---|
| A0–A13 | Address Inputs |
| $\overline{CS}_1$ | Chip Select 1 |
| $\overline{CS}_2$ | Chip Select 2 |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| I/O0–I/O3 | Data I/O |
| VCC | Power |
| GND | Ground |

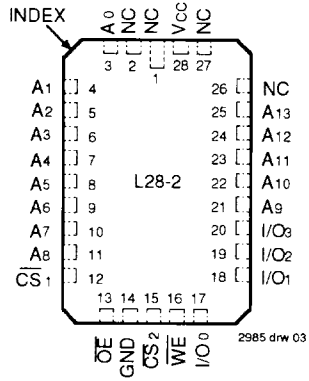
2985 tbl 01

## PIN CONFIGURATIONS




2985 drw 02

**DIP/SOJ/CERPACK**
**TOP VIEW**




2985 drw 03

**LCC**
**TOP VIEW**

## TRUTH TABLE[1]

| Mode | $\overline{CS}_1$ | $\overline{CS}_2$ | $\overline{WE}$ | $\overline{OE}$ | I/O | Power |
|---|---|---|---|---|---|---|
| Standby | H | X | X | X | High Z | Standby |
| Standby | X | H | X | X | High Z | Standby |
| Read | L | L | H | L | DOUT | Active |
| Write | L | L | L | X | DIN | Active |
| Read | L | L | H | H | High Z | Active |

**NOTE:**
1. H = VIH, L = VIL, X = don't care.

2985 tbl 02

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## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Com'l. | Mil. | Unit |
|---|---|---|---|---|
| VTERM | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| TA | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| TBIAS | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| TSTG | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| PT | Power Dissipation | 1.0 | 1.0 | W |
| IOUT | DC Output Current | 50 | 50 | mA |

**NOTE:** 2985 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz, $V_{CC}$ = 0V)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| CIN | Input Capacitance | VIN = 0V | 7 | pF |
| COUT | Output Capacitance | VOUT = 0V | 7 | pF |

**NOTE:** 2985 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| VIH | Input High Voltage | 2.2 | — | 6.0 | V |
| VIL | Input Low Voltage | –0.5(1) | — | 0.8 | V |

**NOTE:** 2985 tbl 05

1. VIL (min.) = -3.0V for pulse width less than 20ns, once per cycle.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Ambient Temperature | GND | VCC |
|---|---|---|---|
| Military | –55°C to +125°C | 0V | 5V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5V ± 10% |

2985 tbl 06

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Condition | | IDT7198S Min. | IDT7198S Max. | IDT7198L Min. | IDT7198L Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| \|ILI\| | Input Leakage Current | VCC = Max., VIN = GND to VCC | MIL. | — | 10 | — | 5 | µA |
| | | | COM'L. | — | 5 | — | 2 | |
| \|ILO\| | Output Leakage Current | VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC | MIL. | — | 10 | — | 5 | µA |
| | | | COM'L. | — | 5 | — | 2 | |
| VOL | Output Low Voltage | IOL = 10mA, VCC = Min. | | | 0.5 | — | 0.5 | V |
| | | IOL = 8mA, VCC = Min. | | — | 0.4 | — | 0.4 | |
| VOH | Output High Voltage | IOH = -4mA, VCC = Min. | | 2.4 | — | 2.4 | — | V |

2985 tbl 07

## DC ELECTRICAL CHARACTERISTICS[1]

($V_{CC}$ = 5V ± 10%, $V_{LC}$ = 0.2V, $V_{HC}$ = $V_{CC}$ - 0.2V)

| Symbol | Parameter | Power | 7198S15 7198L15 Com'l. | 7198S15 7198L15 Mil. | 7198S20 7198L20 Com'l. | 7198S20 7198L20 Mil. | 7198S25 7198L25 Com'l. | 7198S25 7198L25 Mil. | 7198S35 7198L35 Com'l. | 7198S35 7198L35 Mil. | 7198S45 7198L45 Com'l. | 7198S45 7198L45 Mil. | 7198S55/70 7198L55/70 Com'l. | 7198S55/70 7198L55/70 Mil. | 7198S85 7198L85 Com'l. | 7198S85 7198L85 Mil. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Operating Power Supply Current, $\overline{CS_1}$ and $\overline{CS_2} \le V_{IL}$, Outputs Open $V_{CC}$ = Max., f = 0[2] | S | 100 | — | 100 | 105 | 100 | 105 | 100 | 105 | — | 105 | — | 105 | — | 105 | mA |
| | | L | 75 | — | 70 | 80 | 70 | 80 | 70 | 80 | — | 80 | — | 80 | — | 80 | |
| $I_{CC2}$ | Dynamic Operating Current, $\overline{CS_1}$ and $\overline{CS_2} \le V_{IL}$, Outputs Open $V_{CC}$ = Max., f = $f_{MAX}$[2] | S | 135 | — | 130 | 160 | 125 | 155 | 125 | 140 | — | 140 | — | 140 | — | 140 | mA |
| | | L | 125 | — | 115 | 130 | 105 | 120 | 105 | 115 | — | 110 | — | 110 | — | 105 | |
| $I_{SB}$ | Standby Power Supply Current (TTL Level), $\overline{CS_1}$ or $\overline{CS_2} \ge V_{IH}$, $V_{CC}$ = Max., Outputs Open, f = $f_{MAX}$[2] | S | 60 | — | 55 | 70 | 50 | 60 | 45 | 50 | — | 50 | — | 50 | — | 50 | mA |
| | | L | 45 | — | 40 | 50 | 35 | 40 | 30 | 35 | — | 35 | — | 35 | — | 35 | |
| $I_{SB1}$ | Full Standby Power Supply Current (CMOS Level) $\overline{CS_1}$ or $\overline{CS_2} \ge V_{HC}$, $V_{CC}$= Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[2] | S | 20 | — | 15 | 25 | 15 | 20 | 15 | 20 | — | 20 | — | 20 | — | 20 | mA |
| | | L | 1.5 | — | 0.5 | 1.5 | 0.5 | 1.5 | 0.5 | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | |

**NOTES:**
1. All values are maximum guaranteed values
2. At f = $f_{MAX}$ address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

2985 tbl 06

## DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

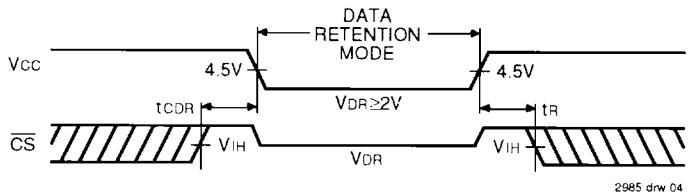
(L Version Only) $V_{LC}$ = 0.2V, $V_{HC}$ = $V_{CC}$ - 0.2V

| Symbol | Parameter | Test Condition | | Min. | Typ.[1] $V_{CC}$ @ 2.0v | Typ.[1] $V_{CC}$ @ 3.0V | Max. $V_{CC}$ @ 2.0v | Max. $V_{CC}$ @ 3.0V | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | — | | 2.0 | — | — | — | — | V |
| $I_{CCDR}$ | Data Retention Current | | MIL. | — | 10 | 15 | 600 | 900 | µA |
| | | | COM'L. | — | 10 | 15 | 150 | 225 | |
| $t_{CDR}$[3] | Chip Deselect to Data Retention Time | $\overline{CS_1}$ or $\overline{CS_2} \ge V_{HC}$ $V_{IN} \ge V_{HC}$ or $\le V_{LC}$ | | 0 | — | — | — | — | ns |
| $t_R$[3] | Operation Recovery Time | | | $t_{RC}$[2] | — | — | — | — | ns |
| $\|I_{LI}\|$[3] | Input Leakage Current | | | — | — | — | 2 | 2 | µA |

**NOTES:**
1. $T_A$ = +25°C.
2. $t_{RC}$ = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

2985 tbl 09

## LOW $V_{CC}$ DATA RETENTION WAVEFORM




2985 drw 04

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

2985 tbl 10

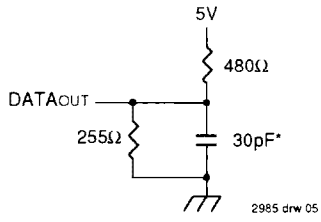



**Figure 1. AC Test Load**

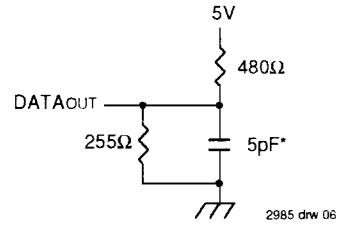



**Figure 2. AC Test Load**
**(for $t_{CLZ1,2}$, $t_{OLZ}$, $t_{CHZ1,2}$, $t_{OHZ}$, $t_{OW}$ and $t_{WHZ}$)**

*Includes scope and jig capacitances

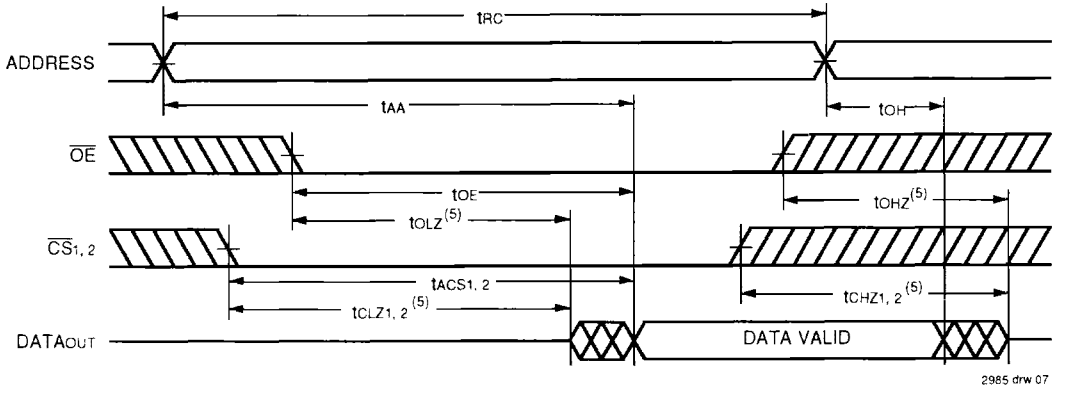
## AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

| | | 7198S15[1]/20 7198L15[1]/20 | | 7198S25 7198L25 | | 7198S35/45[2] 7198L35/45[2] | | 7198S55[2] 7198L55[2] | | 7198S70[2] 7198L70[2] | | 7198S85[2] 7198L85[2] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| **Read Cycle** | | | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 15/20 | — | 25 | — | 35/45 | — | 55 | — | 70 | — | 85 | — | ns |
| $t_{AA}$ | Address Access Time | — | 15/19 | — | 25 | — | 35/45 | — | 55 | — | 70 | — | 85 | ns |
| $t_{ACS1,2}$ | Chip Select-1,2 Access Time[3] | — | 15/20 | — | 25 | — | 35/45 | — | 55 | — | 70 | — | 85 | ns |
| $t_{CLZ1,2}$ | Chip Select-1,2 to Output in Low Z[4] | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 8/9 | — | 11 | — | 20/25 | — | 35 | — | 45 | — | 55 | ns |
| $t_{OLZ}$ | Output Enable to Output in Low Z[4] | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{CHZ1,2}$ | Chip Select 1,2 to Output in High Z[4] | — | 7/8 | — | 10 | — | 14 | — | 20 | — | 25 | — | 30 | ns |
| $t_{OHZ}$ | Output Disable to Output in High Z[4] | — | 7/8 | — | 9 | — | 15 | — | 20 | — | 25 | — | 30 | ns |
| $t_{OH}$ | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{PU}$ | Chip Select to Power Up Time[4] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$ | Chip Deselect to Power Down Time[4] | — | 15/20 | — | 25 | — | 35/45 | — | 55 | — | 70 | — | 85 | ns |

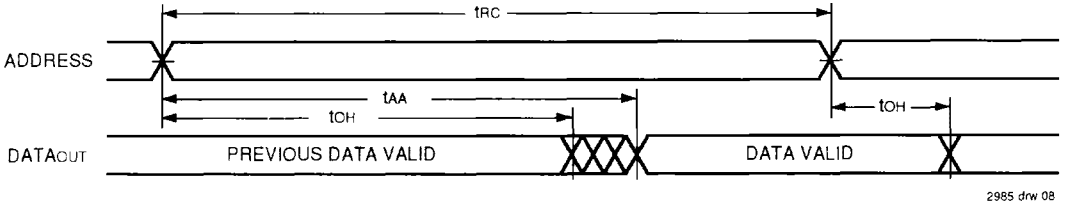
**NOTES:**
2985 tbl 11

1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter is guaranteed by device characterization but is not production tested.

## TIMING WAVEFORM OF READ CYCLE NO. 1(1)




## TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

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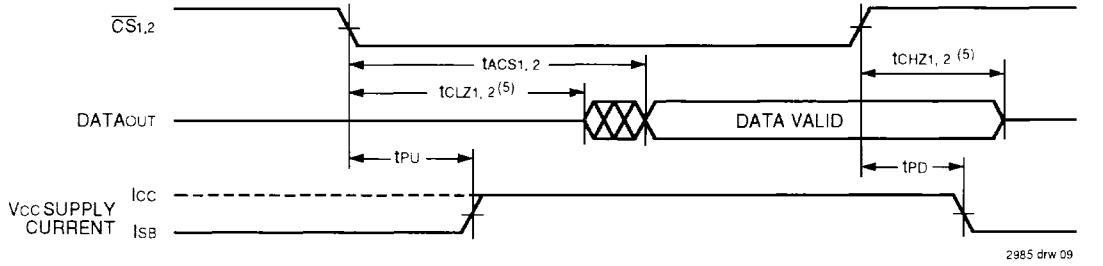
## TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)




**NOTES:**
1. $\overline{WE}$ is HIGH for READ cycle.
2. Device is continuously selected, $\overline{CS_1} = V_{IL}$, $\overline{CS_2} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS_1}$ and or $\overline{CS_2}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state voltage.

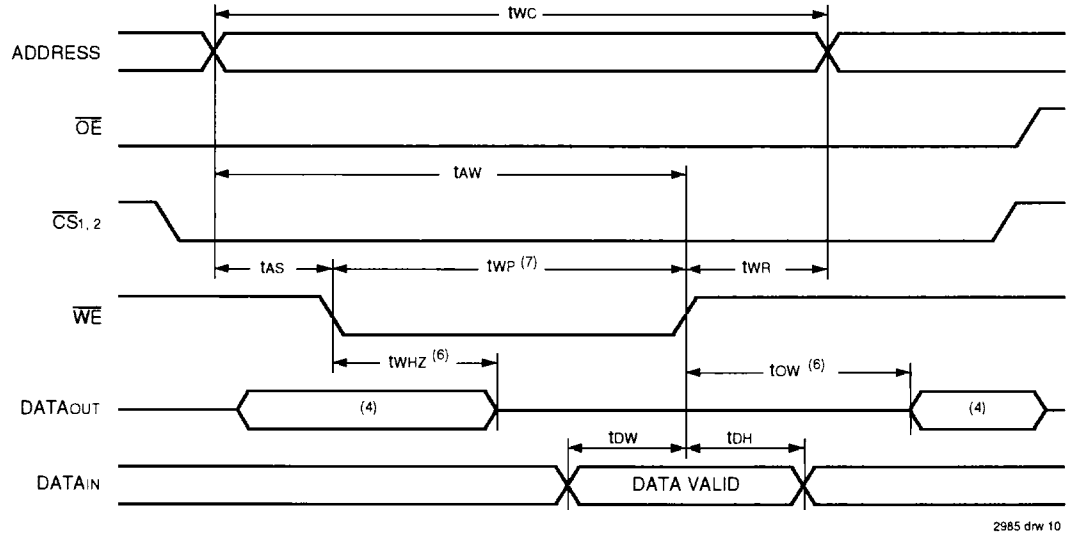
## AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 7198S15[1]/20 7198L15[1]/20 | | 7198S25 7198L25 | | 7198S35/45[2] 7198L35/45[2] | | 7198S55[2] 7198L55[2] | | 7198S70[2] 7198L70[2] | | 7198S85[2] 7198L85[2] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Write Cycle** | | | | | | | | | | | | | | |
| tWC | Write Cycle Time | 14/17 | — | 20 | — | 30/40 | — | 50 | — | 60 | — | 75 | — | ns |
| tCW1,2 | Chip Select to End-of-Write[3] | 14/17 | — | 20 | — | 25/35 | — | 50 | — | 60 | — | 75 | — | ns |
| tAW | Address Valid to End-of-Write | 14/17 | — | 20 | — | 25/35 | — | 50 | — | 60 | — | 75 | — | ns |
| tAS | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWP | Write Pulse Width | 14/17 | — | 20 | — | 25/35 | — | 50 | — | 60 | — | 75 | — | ns |
| tWR1,2 | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWHZ | Write Enable to Output in High-Z[4] | — | 5/6 | — | 7 | — | 10/15 | — | 25 | — | 30 | — | 40 | ns |
| tDW | Data Valid to End-of-Write | 10 | — | 13 | — | 15/20 | — | 25 | — | 30 | — | 35 | — | ns |
| tDH | Data Hold Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tOW | Output Active from End-of-Write[4] | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |

**NOTES:**
2985 tbl 12

1. 0° to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter is guaranteed by device characterization but is not production tested.

## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]

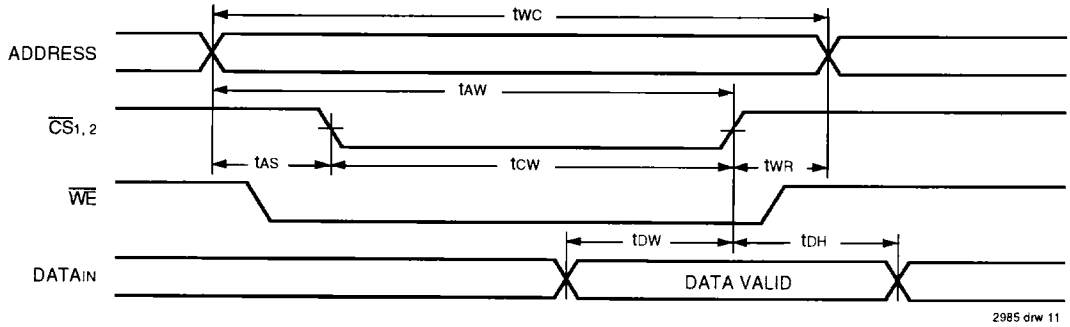



2985 drw 10

**NOTES:**

1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{WE}$, a low $\overline{CS_1}$ and a LOW $\overline{CS_2}$.
3. tWR is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1)




**NOTES:**
1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (twp) of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a LOW $\overline{CS_2}$.
3. twr is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of twp or (twhz + tdw) to allow the I/O drivers to turn off and data to be placed on the required tdw. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

## ORDERING INFORMATION