

NL27WZ06

Product Preview

Dual Inverter with Open Drain Outputs

The NL27WZ06 is a high performance dual inverter with open drain outputs operating from a 2.3 to 5.5 V supply.

The internal circuit is composed of multiple stages, including an open drain output which provides the capability to set output switching level. This allows the NL27WZ06 to be used to interface 5 V circuits to circuits of any voltage between V_{CC} and 7 V using an external resistor and power supply.

Current drive capability is 24 mA at the outputs.

- Extremely High Speed: t_{PD} 2.5 ns (typical) at $V_{CC} = 5$ V
- Designed for 2.3 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs
- LVTTTL Compatible – Interface Capability With 5 V TTL Logic with $V_{CC} = 3$ V
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements

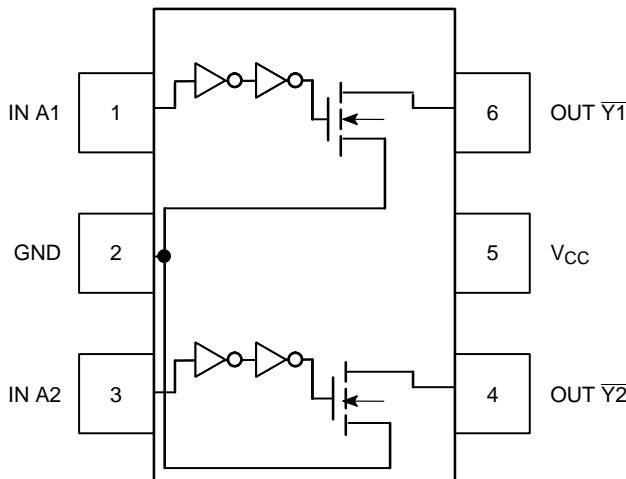


Figure 1. 6-Lead SOT-363 Pinout (Top View)

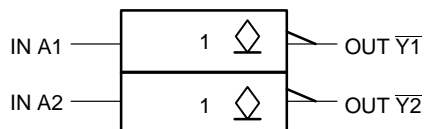


Figure 2. Logic Symbol

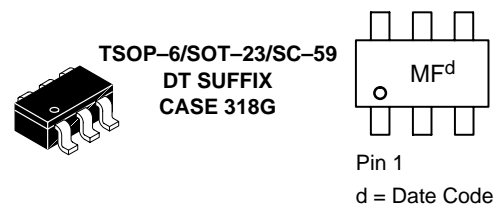
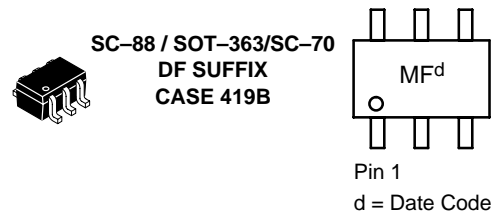
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MARKING DIAGRAMS



PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT $\bar{Y}2$
5	V_{CC}
6	OUT $\bar{Y}1$

FUNCTION TABLE

A Input	\bar{Y} Output
L	Z
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _I	DC Input Voltage		-0.5 ≤ V _I ≤ +7.0	V
V _O	DC Output Voltage	Output in HIGH or LOW State.(Note 3.)	-0.5 ≤ V _O ≤ V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	V _I < GND	-50	mA
I _{OK}	DC Output Diode Current	V _O < GND	-50	mA
		V _O > V _{CC}	+50	mA
I _O	DC Output Source/Sink Current		±50	mA
I _{CC}	DC Supply Current Per Supply Pin		±100	mA
I _{GND}	DC Ground Current Per Ground Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
P _D	Power Dissipation in Still Air SC-88, TSOP-6	per derating (Note 2.)	200	mW
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 4.)	> 2000	V
		Machine Model (Note 5.)	> 200	
		Charged Device Model (Note 6.)	> 3000	
I _{Latch-Up}	Latch-Up Performance	Above V _{CC} and Below GND at 85°C (Note 7.)	±500	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.
2. Derating — SC-88 Package: -3 mW/°C from 65° to 125°C
— TSOP-6 Package: -5 mW/°C from 65° to 125°C
3. I_O absolute maximum rating must be observed.
4. Tested to EIA/JESD22-A114-A
5. Tested to EIA/JESD22-A115-A
6. Tested to JESD22-C101-A
7. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Supply Voltage	Operating	2.3	5.5	V
		Data Retention Only	1.5	5.5	
V _I	Input Voltage	0	5.5	V	
V _O	Output Voltage (HIGH or LOW State)	0	V _{CC}	V	
I _{OH}	HIGH Level Output Current	V _{CC} = 4.5 V - 5.5 V		-32	mA
		V _{CC} = 3.0 V - 3.6 V		-24	
		V _{CC} = 2.7 V - 3.0 V		-12	
		V _{CC} = 2.3 V - 2.7 V		-8	
I _{OL}	LOW Level Output Current	V _{CC} = 4.5 V - 5.5 V		+32	mA
		V _{CC} = 3.0 V - 3.6 V		+24	
		V _{CC} = 2.7 V - 3.0 V		+12	
		V _{CC} = 2.3 V - 2.7 V		+8	
T _A	Operating Free-Air Temperature	-40	+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate	V _{CC} = 2.5 V ±0.2 V	0	20	ns/V
		V _{CC} = 3.0 V ±0.3 V	0	10	
		V _{CC} = 5.0 V ±0.5 V	0	5	

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The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

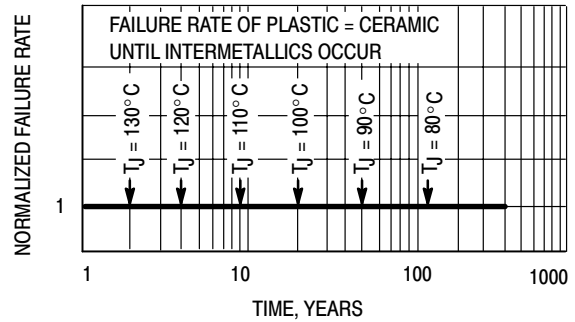


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		V
V _{IL}	Maximum Low-Level Input Voltage		2.3 to 5.5			0.3 V _{CC}		0.3 V _{CC}	V
I _{LKG}	Maximum Low-Level Output Leakage Current	V _{IN} = V _{IL} and V _{OUT} = V _{CC} or GND	2.3 to 5.5			±5.0		±10.0	μA
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3 to 5.5			0.1		0.1	V
		I _{OL} = 8 mA	2.3		TBD	0.3		0.3	
		I _{OL} = 12 mA	2.7		TBD	0.4		0.4	
		I _{OL} = 16 mA	3.0		TBD	0.4		0.4	
		I _{OL} = 24 mA	3.0		TBD	0.55		0.55	
		I _{OL} = 32 mA	4.5		TBD	0.55		0.55	
I _{IN}	Maximum Input Leakage Current	V _{IN} or V _{OUT} = V _{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I _{OFF}	Maximum Off-State Leakage Current	V _{OUT} = 5.5 V	0			1		10	nA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PZL}	Maximum Output Enable Time Input A to Y Figure 4. and 5.	R _L = R ₁ = 500 Ω, C _L = 50 pF	2.5 ± 0.2	0.8	3.0	3.6	0.8	4.1	ns
		R _L = R ₁ = 500 Ω, C _L = 50 pF	3.3 ± 0.3	0.8	2.4	3.2	0.8	3.7	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	5.0 ± 0.5	0.5	2.4	3.0	0.5	3.5	
t _{PLZ}	Maximum Output Disable Time Input A to Y Figure 4. and 5.	R _L = R ₁ = 500 Ω, C _L = 50 pF	2.5 ± 0.2	0.8	2.5	3.6	0.8	4.1	ns
		R _L = R ₁ = 500 Ω, C _L = 50 pF	3.3 ± 0.3	0.8	2.1	3.2	0.8	3.7	
		R _L = R ₁ = 500 Ω, C _L = 50 pF	5.0 ± 0.5	0.5	1.2	3.0	0.5	3.5	

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CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance (Note 8.)	10 MHz, $V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	25	pF

8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

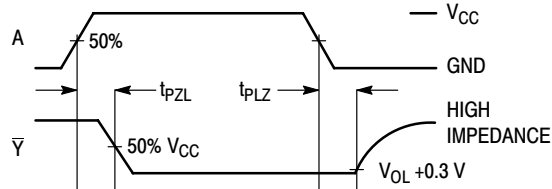


Figure 4. Switching Waveforms

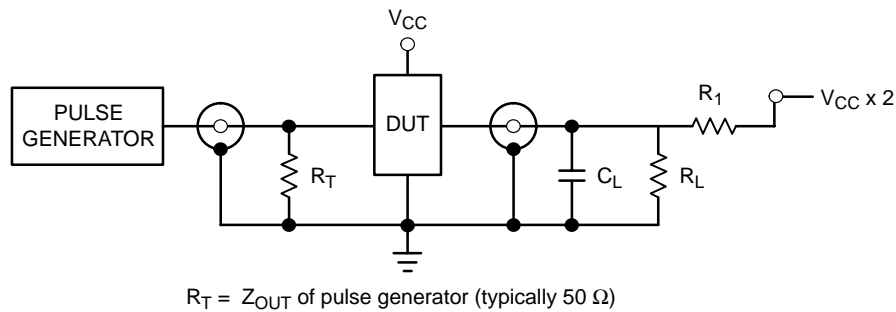


Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NL27WZ06DFT2	NL	2	7	WZ	06	DF	T2	SC-88 / SOT-363 / SC-70	178 mm (7") 3000 Unit
NL27WZ06DFT4	NL	2	7	WZ	06	DF	T4	SC-88 / SOT-363 / SC-70	330 mm (13") 10000 Unit
NL27WZ06DTT1	NL	2	7	WZ	06	DT	T1	TSOP-6 / SOT-23 / SC-59	178 mm (7") 3000 Unit
NL27WZ06DTT3	NL	2	7	WZ	06	DT	T3	TSOP-6 / SOT-23 / SC-59	330 mm (13") 10000 Unit

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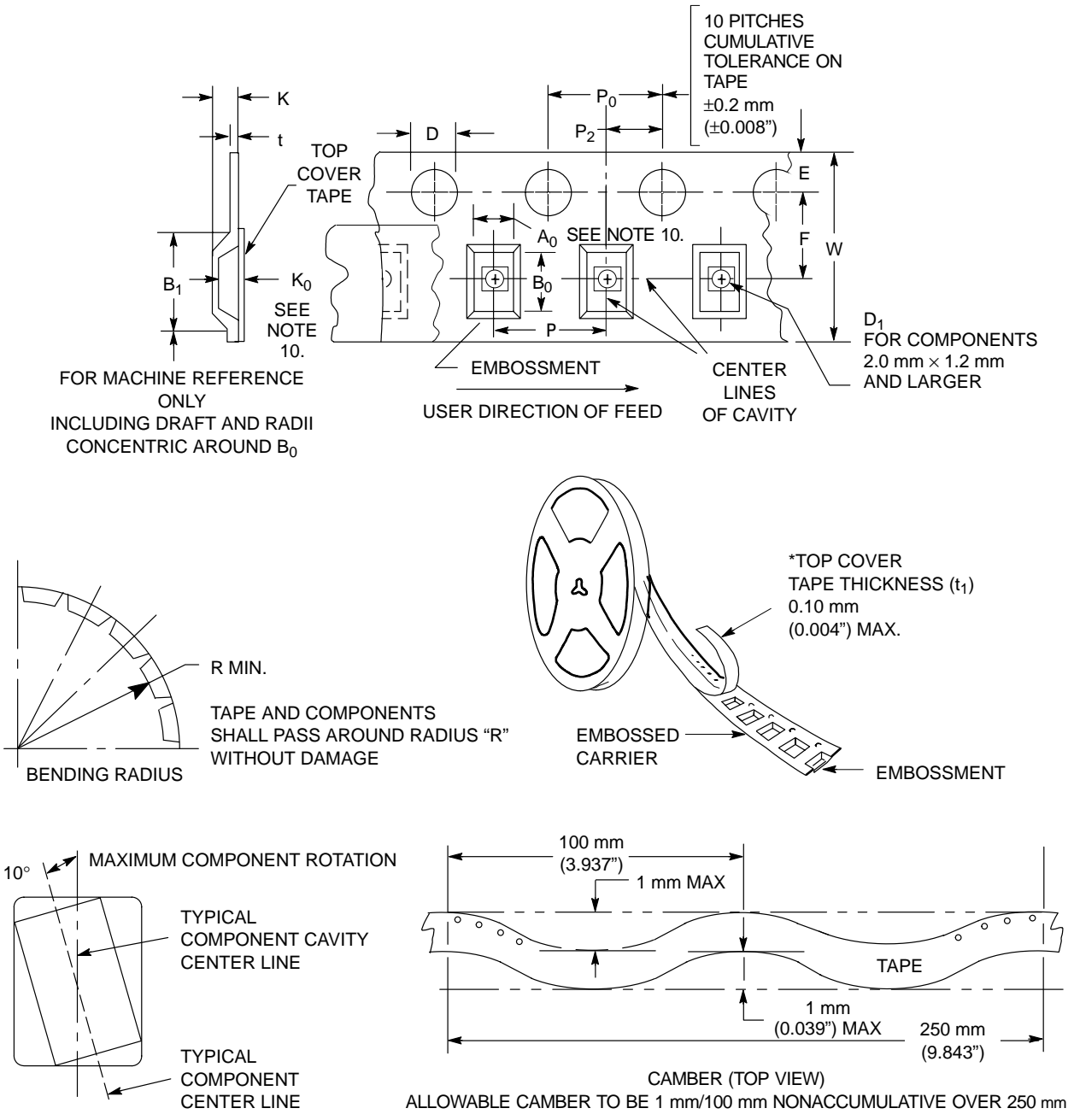


Figure 6. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 9. and 10.)

Tape Size	B ₁ Max	D	D ₁	E	F	K	P	P ₀	P ₂	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/ -0.0 mm (0.059 +0.004/ -0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ -0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

9. Metric Dimensions Govern—English are in parentheses for reference only.

10. A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

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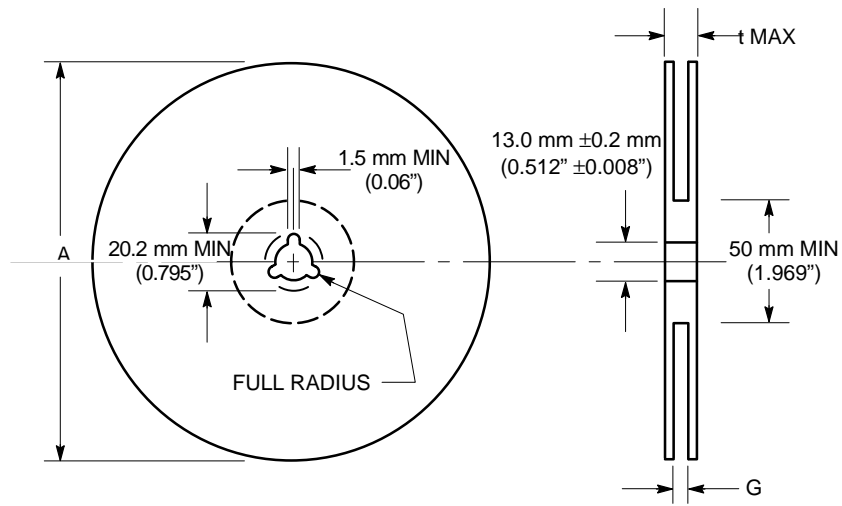


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
8 mm	T3, T4	330 mm (13")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")

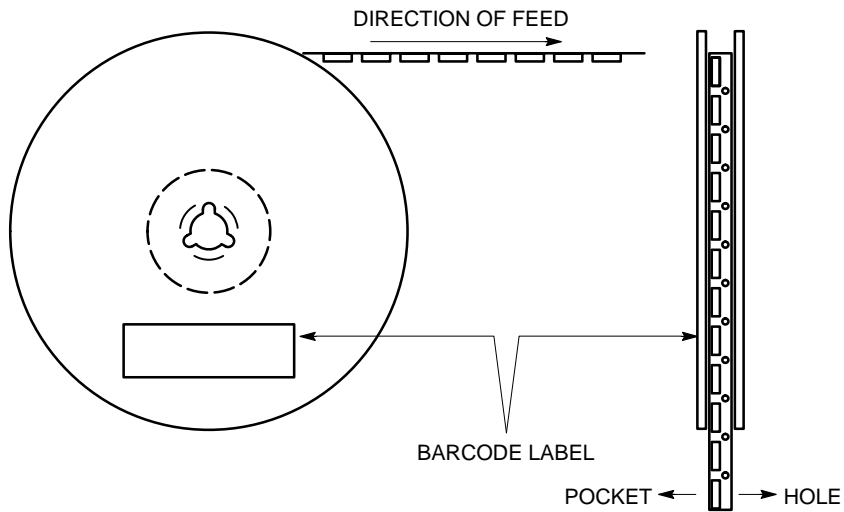


Figure 8. Reel Winding Direction

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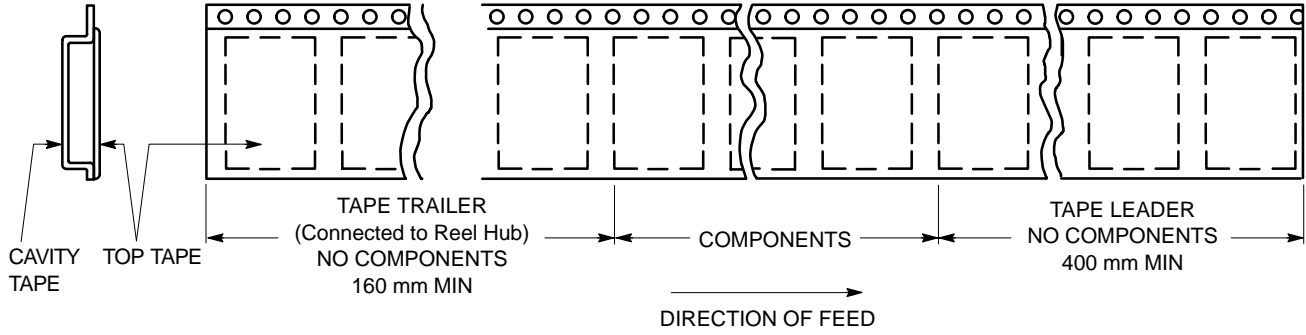


Figure 9. Tape Ends for Finished Goods

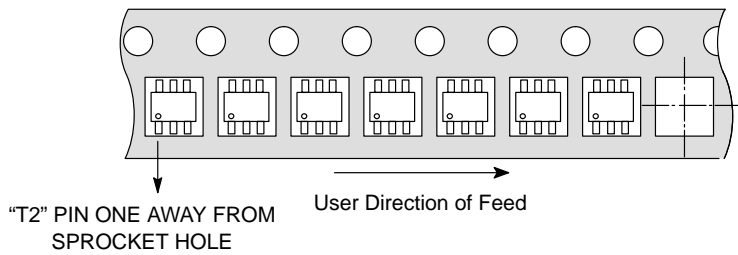


Figure 10. DFT2 and DFT4 (SC88) Reel Configuration/Orientation

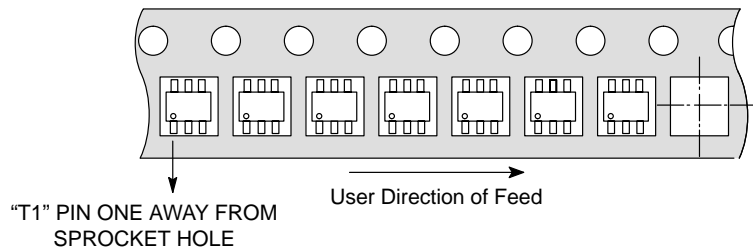


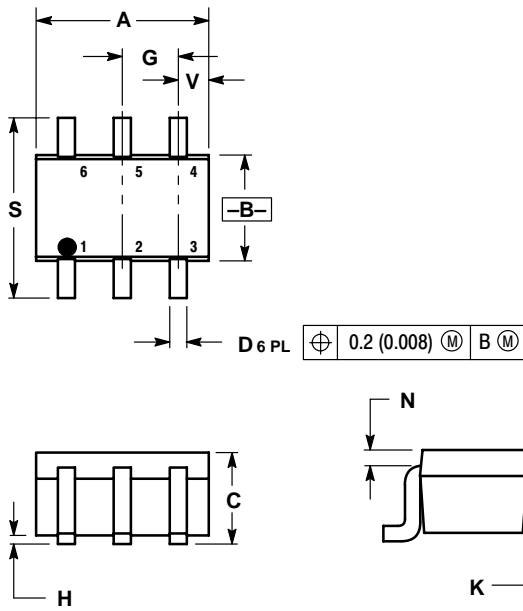
Figure 11. DTT1 and DTT3 (TSOP6) Reel Configuration/Orientation

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PACKAGE DIMENSIONS

SC-88/SOT-363/SC-70
 DF SUFFIX
 CASE 419B-01
 ISSUE G

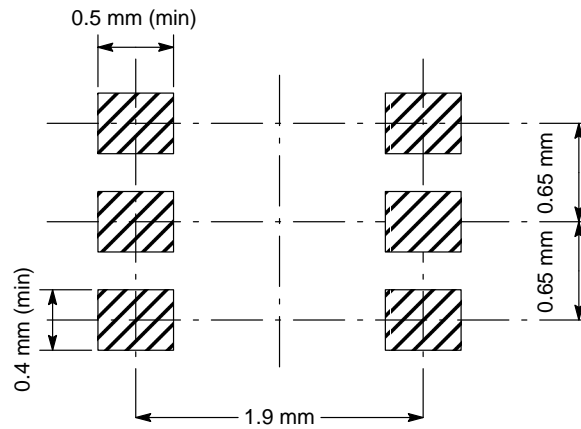
SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

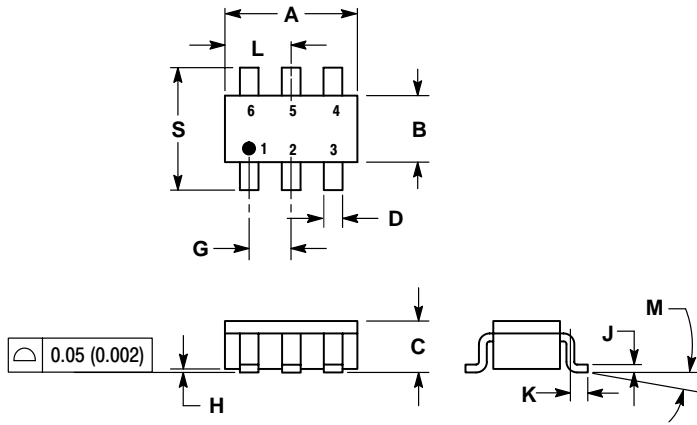


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PACKAGE DIMENSIONS

TSOP-6/SOT-23/SC-59
DT SUFFIX
CASE 318G-02
ISSUE G

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

STYLE 1:

- PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:

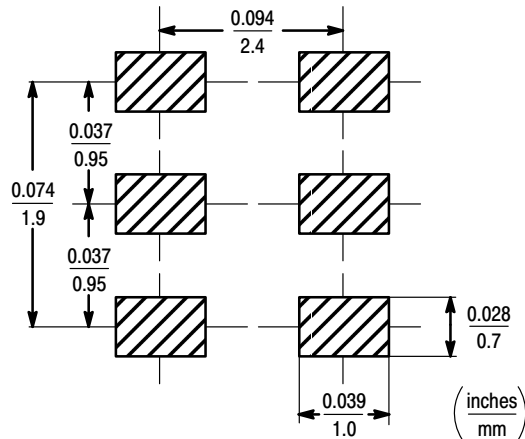
- PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:

- PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out


STYLE 4:

- PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD



Notes

Notes

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