

SN55ALS161, SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

SLLS019E – JUNE 1986 – REVISED NOVEMBER 1999

SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)[†]

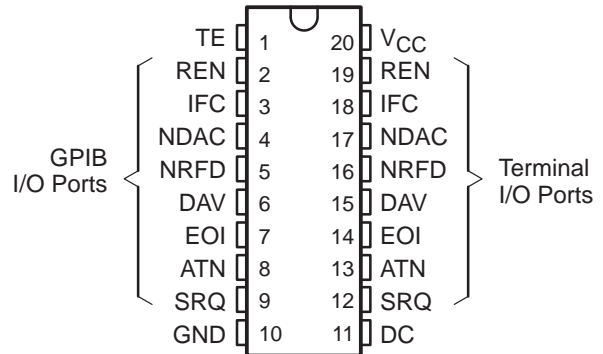
- 8-Channel Bidirectional Transceivers
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation:
SN55ALS161 . . . 59 mW Max Per Channel
SN75ALS161 . . . 46 mW Max Per Channel
- Fast Propagation Times:
SN55ALS161 . . . 25 ns Max
SN75ALS161 . . . 20 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis:
SN55ALS161 . . . 550 mV Typ
SN75ALS161 . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)
- Power-Up/Power-Down Protection (Glitch Free)

description

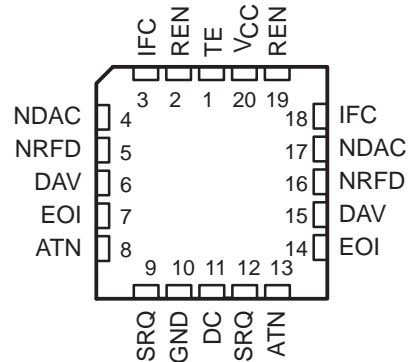
The SN55ALS161 and SN75ALS161 eight-channel general-purpose interface bus transceivers are high-speed, advanced low-power Schottky-process devices designed to provide the bus-management and data-transfer signals between operating units of a single-controller instrumentation system. When combined with the SN55ALS160 and SN75ALS160 octal bus transceivers, these devices provide a complete 16-wire interface for the IEEE 488 bus.

The SN55ALS161 and SN75ALS161 devices feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the direction-control (DC) and talk-enable (TE) signals.

SN55ALS161 . . . J OR W PACKAGE
SN75ALS161 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS161 . . . FK PACKAGE
(TOP VIEW)



CHANNEL-IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC TE	Direction Control Talk Enable	Control
ATN SRQ REN IFC EOI	Attention Service Request Remote Enable Interface Clear End or Identify	Bus Management
DAV NDAC NRFD	Data Valid Not Data Accepted Not Ready for Data	Data Transfer



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] The transceivers are suitable for IEEE Standard 488 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description (continued)

The driver outputs general-purpose interface bus (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when $V_{CC} = 0$. The drivers are designed to handle sink-current loads up to 48 mA. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV on the commercial part, 250 mV on the military part, minimum, for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN55ALS161 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75ALS161 is characterized for operation from 0°C to 70°C .

**FUNCTION TABLE
RECEIVE/TRANSMIT**

CONTROLS			BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS			
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(CONTROLLED BY DC)					(CONTROLLED BY TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.

Data transfer is noninverting in both directions.

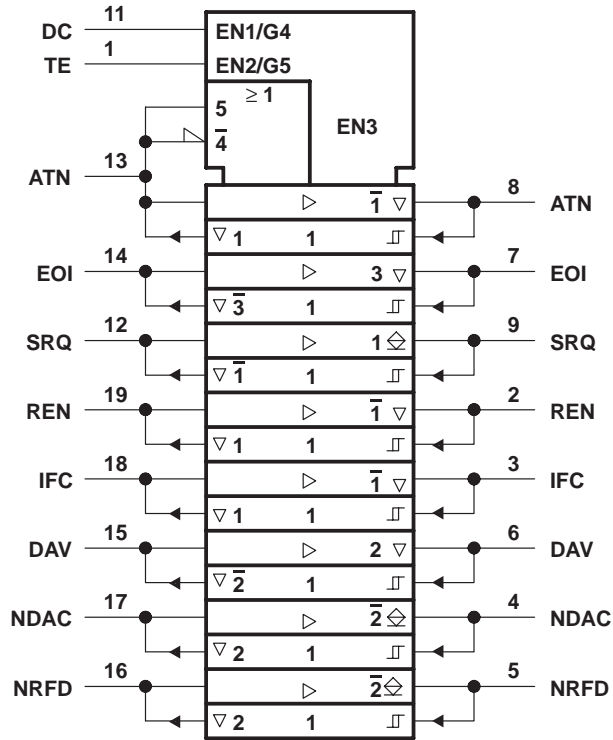
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.



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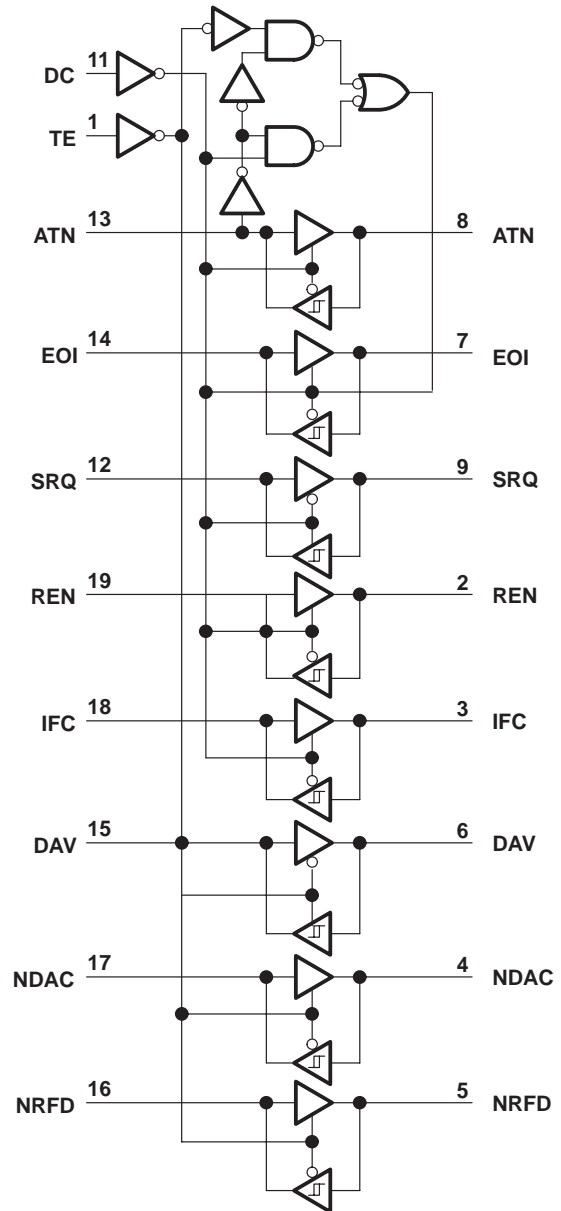
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

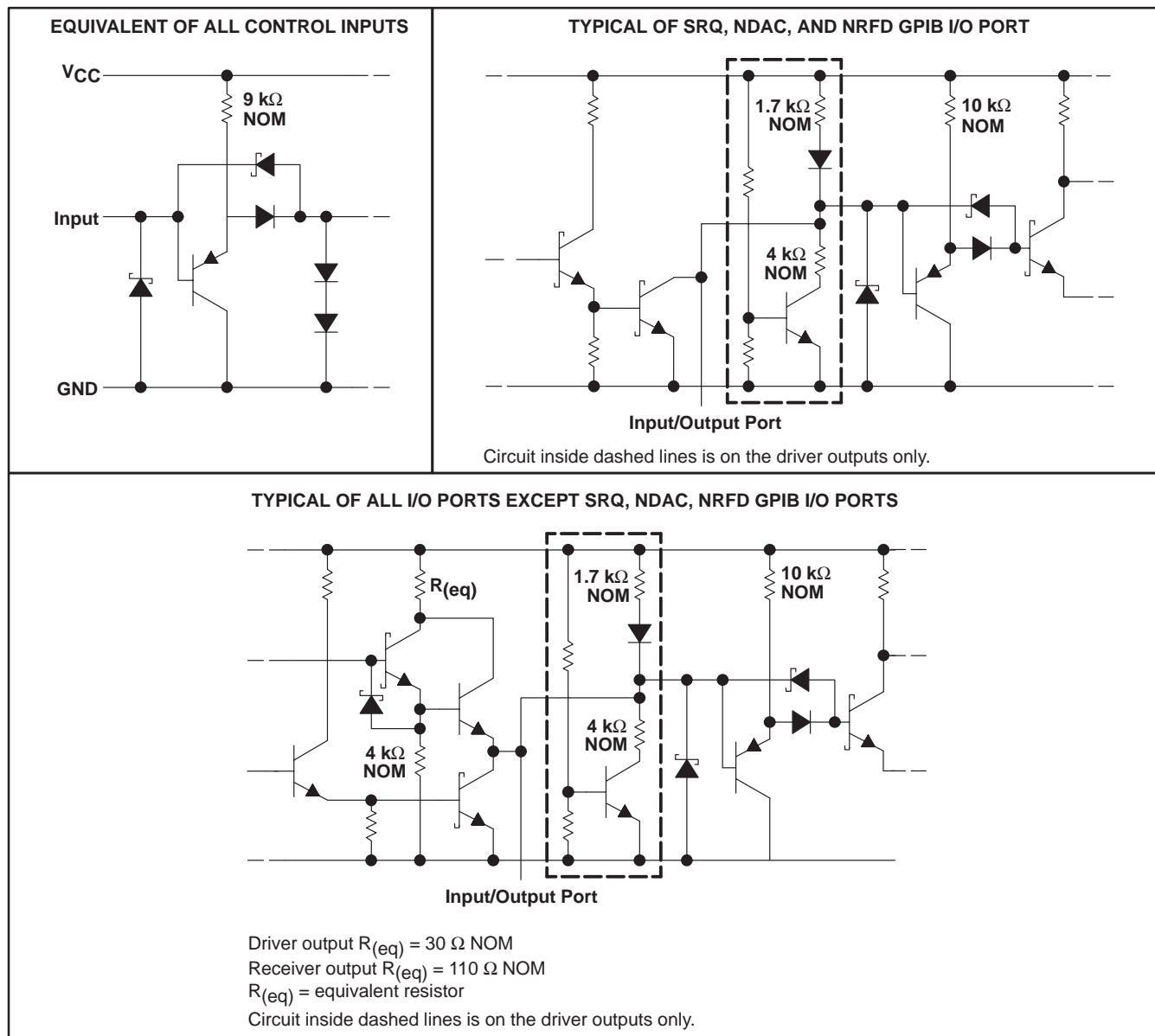
logic diagram (positive logic)



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schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Low-level driver output current, I_{OL}	100 mA
Continuous total dissipation	See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
Case temperature for 60 seconds: FK package, T_C	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

SN55ALS161 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and DC at $T_A = -55^\circ\text{C}$ to 125°C	2			V
	Bus and terminal at $T_A = 25^\circ\text{C}$ to 125°C	2			
	Bus and terminal at $T_A = -55^\circ\text{C}$	2.1			
Low-level input voltage, V_{IL}	TE and DC at $T_A = -55^\circ\text{C}$ to 125°C	0.8			V
	Bus and terminal at $T_A = 25^\circ\text{C}$ to -55°C	0.8			
	Bus and terminal at $T_A = 125^\circ\text{C}$	0.7			
High-level output current, I_{OH}	Bus ports with pullups active ($V_{CC} = 5\text{ V}$)	–5.2			mA
	Terminal ports	–800			μA
Low-level output current, I_{OL}	Bus ports	48			mA
	Terminal ports	16			
Operating free-air temperature, T_A		–55		125	°C



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SN75ALS161 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}		0.8			V
High-level output current, I_{OH}	Bus ports with pullups active	-5.2			mA
	Terminal ports	-800			μ A
Low-level output current, I_{OL}	Bus ports	48			mA
	Terminal ports	16			
Operating free-air temperature, T_A		0	70		$^{\circ}$ C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONST		SN55ALS161			SN75ALS161			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$		-0.8	-1.5		-0.8	-1.5	V	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus					0.4	0.65	V	
		Bus	$V_{CC} = 5 \text{ V}$, $T_A = -55^\circ\text{C}$ and 25°C	0.4	0.55					
$V_{OH}\S$	High-level output voltage	Terminal	$I_{OH} = -800 \mu\text{A}$, $V_{CC} = \text{MIN}$	$T_A = 25^\circ\text{C}$ and MAX	2.7	3.5	2.7	3.5	V	
				$T_A = \text{MIN}$	2.5	3.5	2.7	3.5		
		Bus	$I_{OH} = -5.2 \text{ mA}$, $V_{CC} = \text{MIN}$	$T_A = 25^\circ\text{C}$ and MAX	2.2		2.2			
				$T_A = \text{MIN}$	2.0		2.2			
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16 \text{ mA}$, $V_{CC} = \text{MIN}$	0.3	0.5	0.3	0.5	V		
		Bus	$I_{OL} = 48 \text{ mA}\P$, $V_{CC} = \text{MIN}$	0.35	0.5	0.35	0.5			
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5 \text{ V}$, $V_{CC} = \text{MAX}$	0.2	100	0.2	100	μA		
I_{IH}	High-level input current	Terminal and control inputs	$V_I = 2.7 \text{ V}$, $V_{CC} = \text{MAX}$	0.1	20	0.1	20	μA		
I_{IL}	Low-level input current		$V_I = 0.5 \text{ V}$, $V_{CC} = \text{MAX}$	-30	-100	-10	-100	μA		
$V_{I/O}$	Voltage at GPIB I/O port	Driver disabled, $V_{CC} = 5 \text{ V}$ (SN55')	$I_I(\text{bus}) = 0$	2.5	3	3.7	2.5	3	3.7	V
			$I_I(\text{bus}) = -12 \text{ mA}$			-1.5			-1.5	
$I_{I/O}$	Current into GPIB I/O port	Power on	Driver disabled, $V_{CC} = 5 \text{ V}$ (SN55')	$V_I(\text{bus}) = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3		-1.3		mA	
				$V_I(\text{bus}) = 0.4 \text{ V to } 2.5 \text{ V}$	0	-3.2	0	-3.2		
				$V_I(\text{bus}) = 2.5 \text{ V to } 3.7 \text{ V}$		2.5		2.5		
				$V_I(\text{bus}) = 3.7 \text{ V to } 5 \text{ V}$	0	2.5	0	2.5		
				$V_I(\text{bus}) = 5 \text{ V to } 5.5 \text{ V}$	0.7	2.5	0.7	2.5		
		Power off	$V_{CC} = 0$	$V_I(\text{bus}) = 0 \text{ to } 2.5 \text{ V}$		40		40		μA
$I_{OS}\S$	Short-circuit output current	Terminal	$V_{CC} = \text{MAX}$	-15	-35	-75	-15	-35	-75	mA
		Bus		-25	-50	-125	-25	-50	-125	
I_{CC}	Supply current	No load, TE and DC low, $V_{CC} = \text{MAX}$		55	90	55	75	mA		
$C_{I/O}$	GPIB I/O port capacitance	$V_{CC} = 0 \text{ to } 5 \text{ V}$, $V_{I/O} = 0 \text{ to } 2 \text{ V}$, $f = 1 \text{ MHz}$		30		30		pF		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ V_{OH} and I_{OS} apply to 3-state outputs only.

¶ For SN55', $I_{OL} = 24 \text{ mA}$ at -55°C .



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SN55ALS161 switching characteristics, $V_{CC} = 5\text{ V}$ and $C_L = 50\text{ pF}$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A^\dagger	MIN	TYP ‡	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (Except SRQ, NDAC, and NRFD)	See Figure 1	25°C		10	17	ns
					Full range			20	
t _{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			18	
t _{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (NRFD, SRQ, NDAC)	See Figure 2	25°C			25	ns
					Full range			37	
t _{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			19	
t _{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	See Figure 2	25°C		10	15	ns
					Full range			22	
t _{PHL}	Propagation delay time, high- to low-level output				25°C		10	15	
					Full range			24	
t _{PZH}	Output enable time to high level	TE or DC	Bus (ATN, REN, IFC, and DAV)	See Figure 3	25°C		20	30	ns
					Full range			52	
t _{PHZ}	Output disable time from high level				25°C		8	14	
					Full range			18	
t _{PZL}	Output enable time to low level				25°C		16	28	
					Full range			44	
t _{PLZ}	Output disable time from low level				25°C		10	19	
					Full range			30	
t _{PZH}	Output enable time to high level	TE or DC	Bus (EOI)	See Figure 3	25°C		24	30	ns
					Full range			64	
t _{PHZ}	Output disable time from high level				25°C		13	19	
					Full range			30	
t _{PZL}	Output enable time to low level,				25°C		21	35	
					Full range			54	
t _{PLZ}	Output disable time from low level				25°C		13	20	
					Full range			40	
t _{PZH}	Output enable time to high level	TE or DC	Terminal	See Figure 4	25°C		24	36	ns
					Full range			70	
t _{PHZ}	Output disable time from high level				25°C		12	20	
					Full range			40	
t _{PZL}	Output enable time to low level				25°C		20	34	
					Full range			56	
t _{PLZ}	Output disable time from low level				25°C		13	24	
					Full range			43	

† Full range is -55°C to 125°C .

‡ All typical values are at $V_{CC} = 5\text{ V}$.



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SN75ALS161 switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V}$

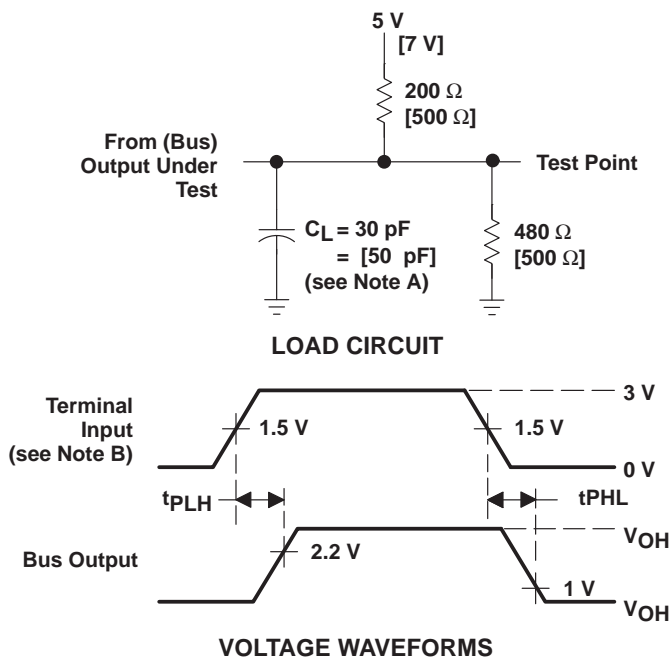
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C _L = 30 pF, See Figure 1	10	20	ns	
t _{PHL}	Propagation delay time, high- to low-level output				12	20		
t _{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C _L = 30 pF, See Figure 2	5	10	ns	
t _{PHL}	Propagation delay time, high- to low-level output				7	14		
t _{PZH}	Output enable time to high level	TE or DC	Bus (ATN, EOI, REN, IFC, and DAV)	C _L = 15 pF, See Figure 3		30	ns	
t _{PHZ}	Output disable time from high level					20		
t _{PZL}	Output enable time to low level					45		
t _{PLZ}	Output disable time from low level					20		
t _{PZH}	Output enable time to high level	TE or DC	Terminal	C _L = 15 pF, See Figure 4		30	ns	
t _{PHZ}	Output disable time from high level					25		
t _{PZL}	Output enable time to low level					30		
t _{PLZ}	Output disable time from low level					25		

† All typical values are at T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION



[] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

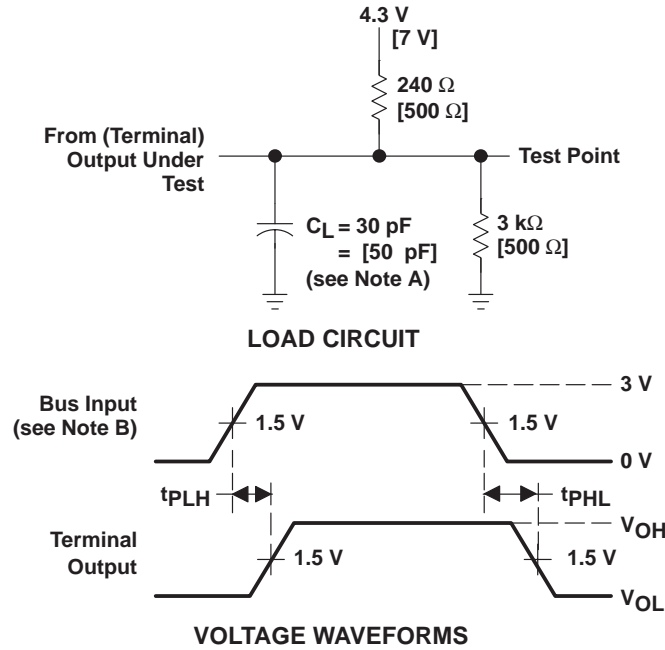
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



[] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

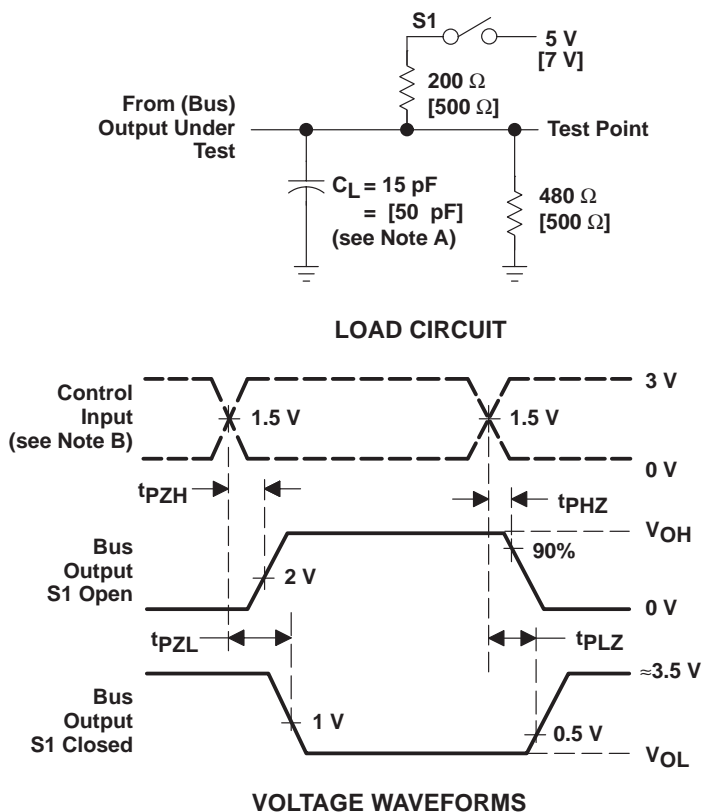
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



[] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

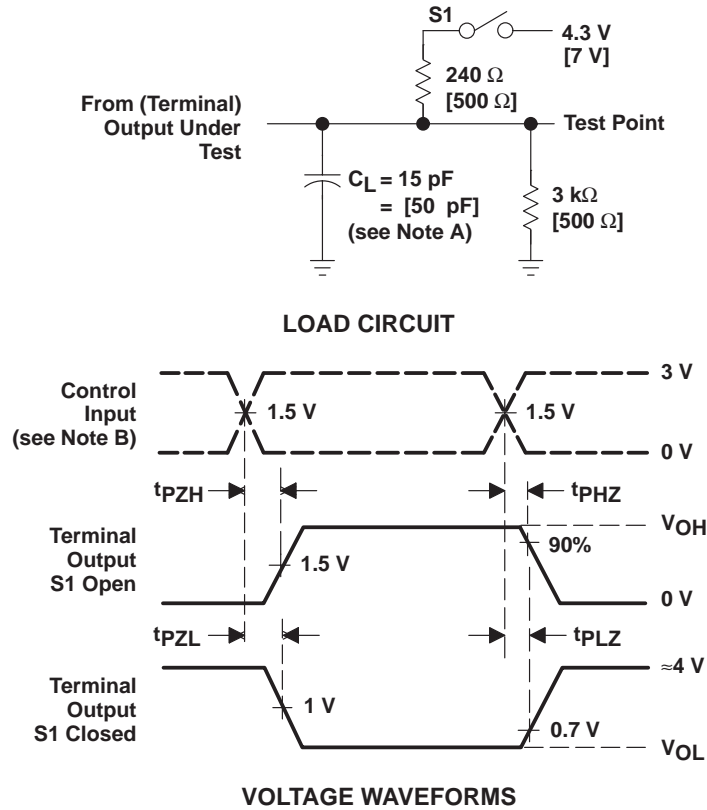
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Bus Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



[] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 4. Terminal Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS†

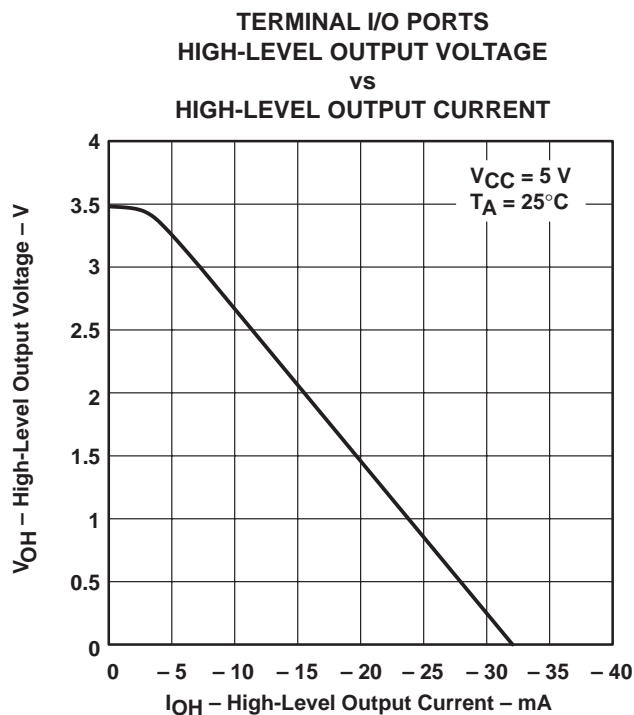


Figure 5

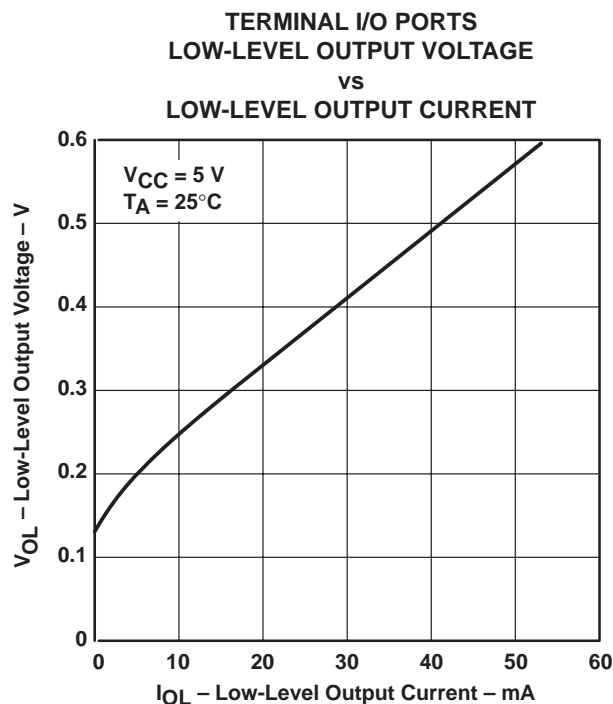


Figure 6

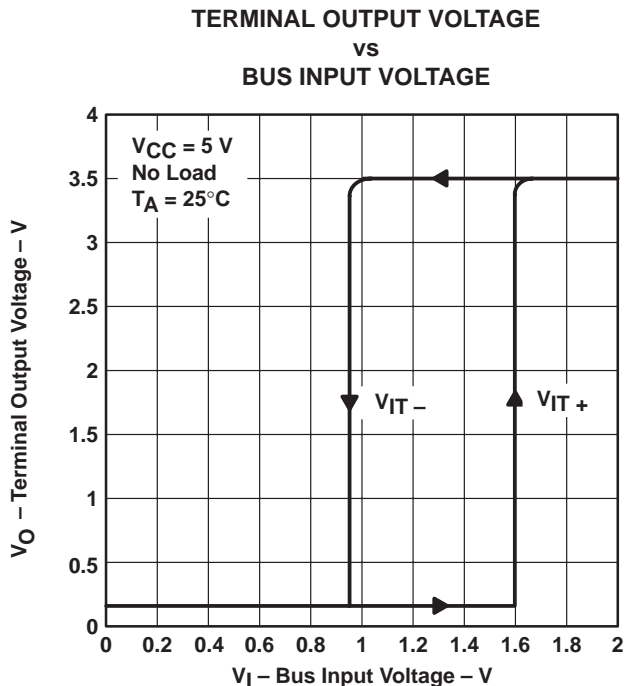


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS†

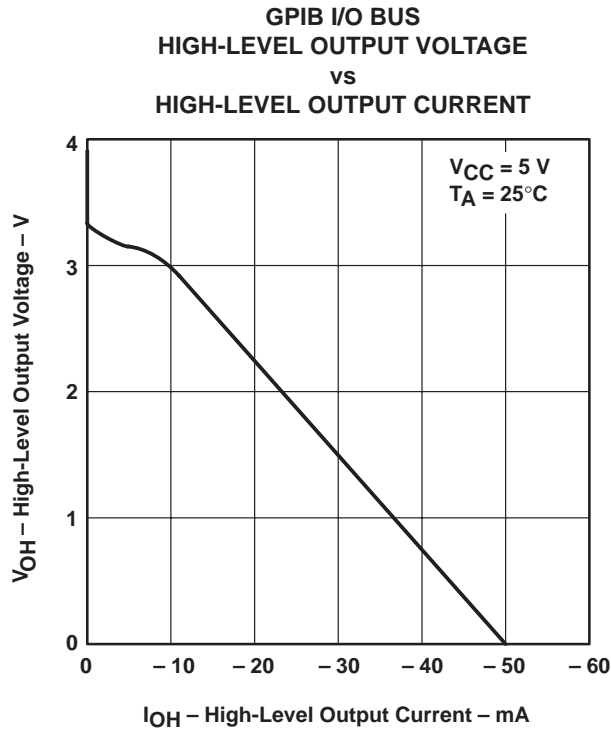


Figure 8

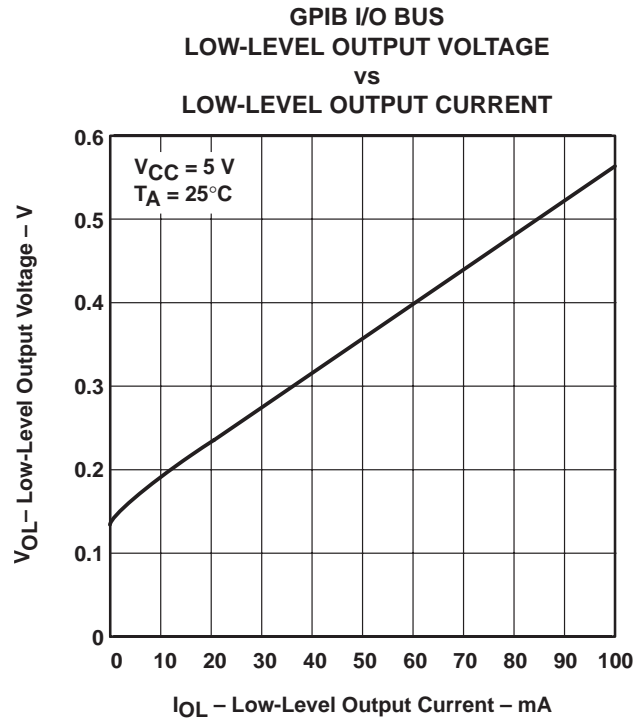


Figure 9

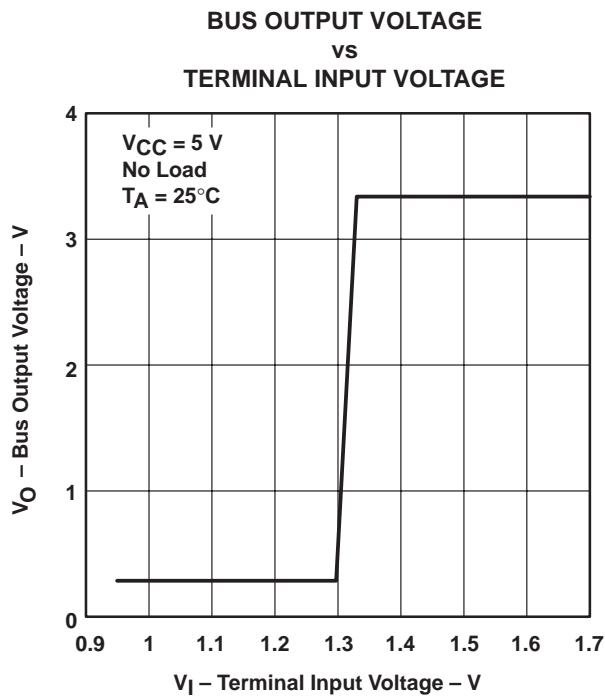


Figure 10

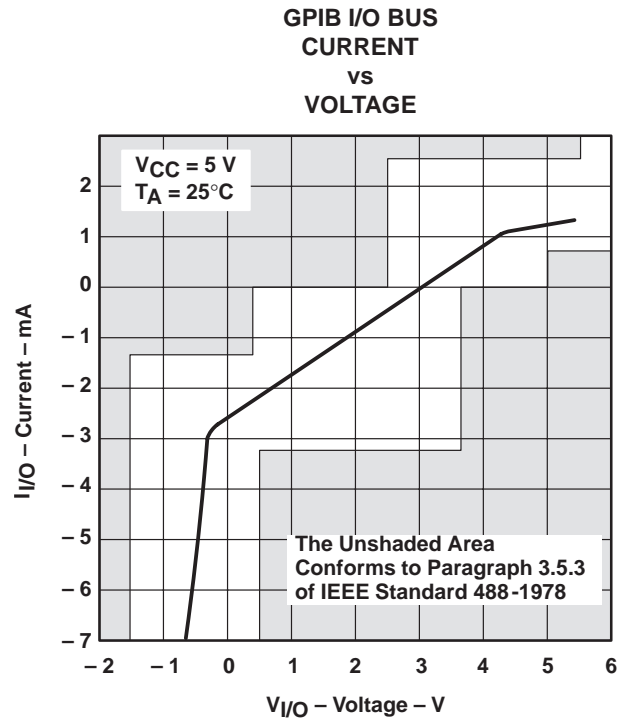


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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