mosaic
semiconductor, inc.

512K x 8 SRAM

MSM8512-025/35/45/55

Issue 4.1 : March 1996

Description

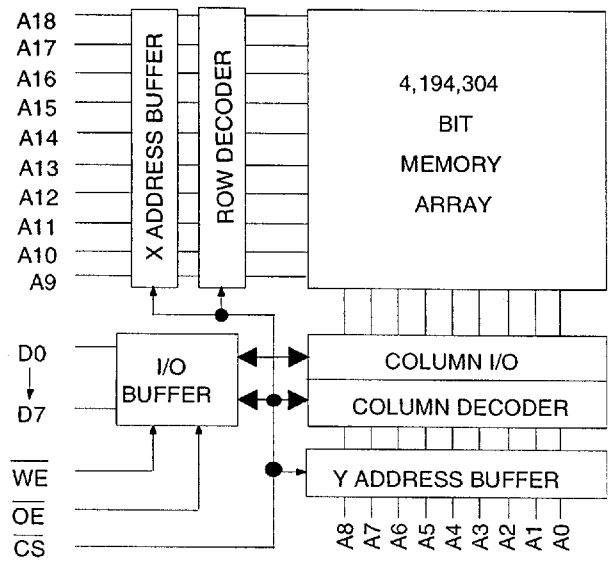
The MSM8512 is a 4Mbit monolithic High Speed SRAM organised as 512K x 8 with access times from 25 to 55ns. This is the next generation upgrade from the MSM8128 1 Mbit monolithic. The device features completely static operation with all common inputs and outputs directly TTL compatible. It has a low power standby option with 2V data retention capabilty.
May be screened in accordance with MIL-STD-883.

524,288 x 8 CMOS High Speed Static RAM

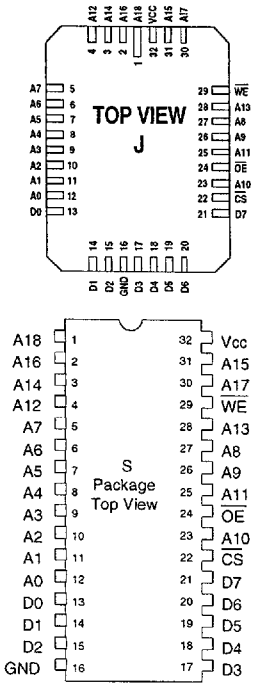
Features

- Fast Access Times of 25/35/45/55 ns
- Average Operating Power 990 mW (max)
- Standby Power -L version 3.85 mW (max)
- Completely Static Operation
- Directly TTL compatible common data inputs & outputs.
- JEDEC Standard 32 pin DIL footprint
- Common data inputs & outputs
- May be processed in accordance with MIL-STD-883

Block Diagram



Pin Definition



Pin Functions

A0-A18	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
GND	Ground

Package Details

Pin Count	Descripion	Package Type
32	Extended 'J' Leaded Chip Carrier (JLCC)	J
32	Dual in Line (DIL)	S

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{cc} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I suffix)
	T_{AM}	-55	-	125	°C (M, MB suffix)

Note:- VIL (min) = - 3.0V for less than 10ns.

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-2	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V to V_{CC}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	-2	-	2	µA
Average Supply Current	I_{CC1}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, min cycle, duty=100%	-	-	180	mA
Standby Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}	-	-	60	mA
-L version only	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC} -0.2V or 0.2V≥V_{IN}	-	-	700	µA
Output Voltage	V_{OL}	I_{OL}=8 mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4 mA	2.4	-	-	V

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance:	C_{IN}	V_{IN} = 0V	-	6	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$ = 0V	-	8	pF

Note: This parameter is sampled and not 100% tested.

Operation Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DATA PINS	SUPPLY CURRENT	MODE
H	X	X	High Impedance	I_{SB}, I_{SB1}	Standby
L	L	H	Data Out	I_{CC1}	Read
L	X	L	Data In	I_{CC1}	Write
L	H	H	Data In	I_{CC1}	Output Disable

Notes : H = V_{IH} : L = V_{IL} : X = V_{IH} or V_{IL}

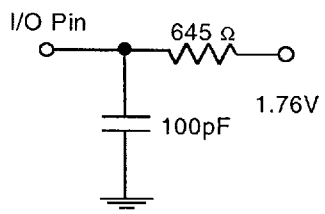
Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$≥V_{CC}-0.2V	2.0	-	5.5	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS}$≥V_{CC}-0.2V,	-	-	400	µA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

AC Test Conditions

* Input pulse levels: 0 V to 3.0 V
* Input rise and fall times: 3ns
* Input and Output timing reference levels: 1.5V
* Output load: See Load Diagram
* V_{cc}=5V±10%

Output Load



AC OPERATING CONDITIONS

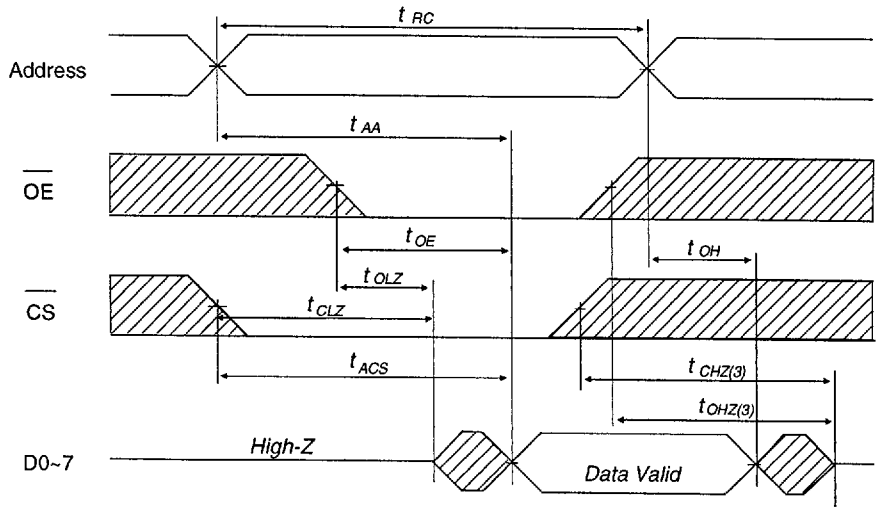
Read Cycle

		25		35		45		55		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Units*
Read Cycle Time	t_{RC}	25	-	35	-	45	-	55	-	ns
Address Access Time	t_{AA}	-	25	-	35	-	45	-	55	ns
Chip Select Access Time	t_{ACS}	-	25	-	35	-	45	-	55	ns
Output Enable to Output Valid	t_{OE}	-	12	-	14	-	16	-	18	ns
Output Hold from Address Change	t_{OH}	5	-	6	-	7	-	8	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	13	0	17	0	21	ns
Output Disable to Output in High Z	t_{OHZ}	0	10	0	13	0	17	0	21	ns

Write Cycle

		25		35		45		55		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	25	-	35	-	45	-	55	-	ns
Chip Selection to End of Write	t_{CW}	15	-	18	-	22	-	27	-	ns
Address Valid to End of Write	t_{AW}	15	-	18	-	22	-	27	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	15	-	18	-	22	-	27	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	10	0	10	0	12	0	12	ns
Data to Write Time Overlap	t_{DW}	10	-	11	-	12	-	13	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	6	-	7	-	8	-	ns

Read Cycle Timing Waveform (1,2,3)



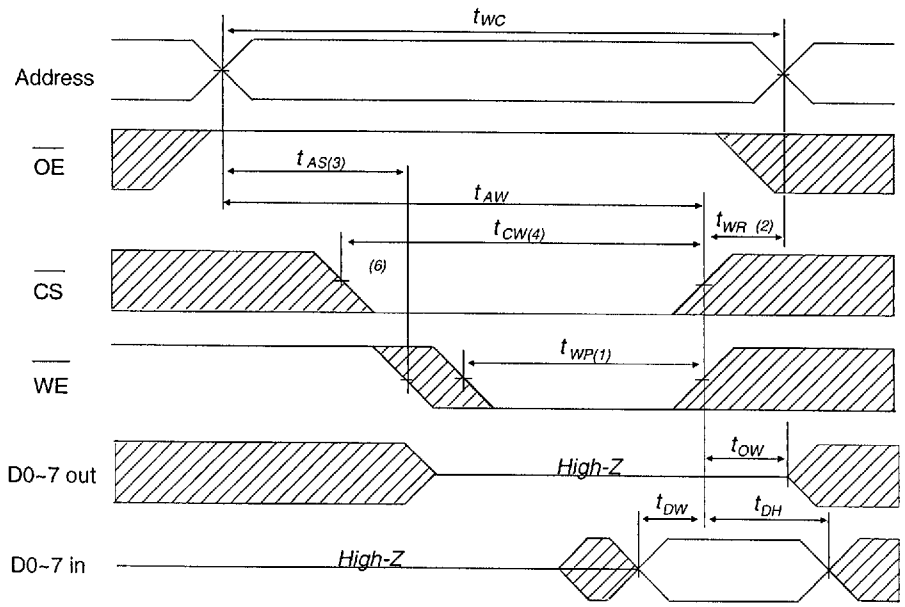
Notes:

(1) During the Read Cycle, $\overline{WE}$ is high.

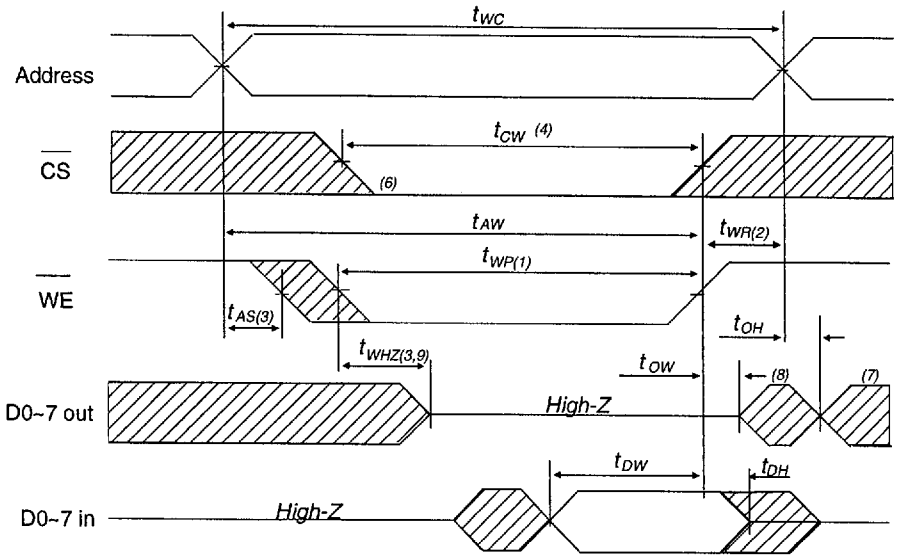
(2) Address valid prior to or coincident with $\overline{CS}$ transition Low.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})

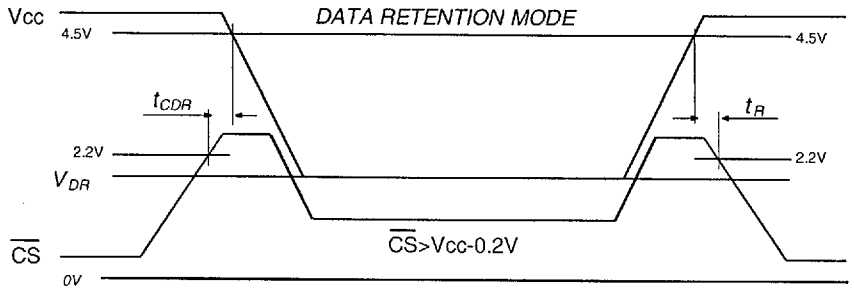
(6) D_{OUT} is in the same phase as written data of this write cycle.

(7) D_{OUT} is the read data of next address.

(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied.

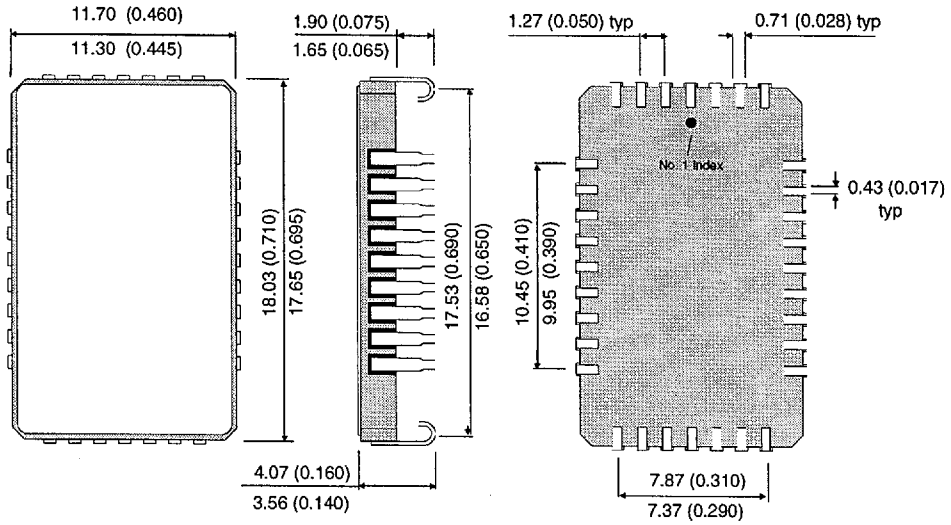
(9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Low V_{CC} Data Retention Timing Waveform

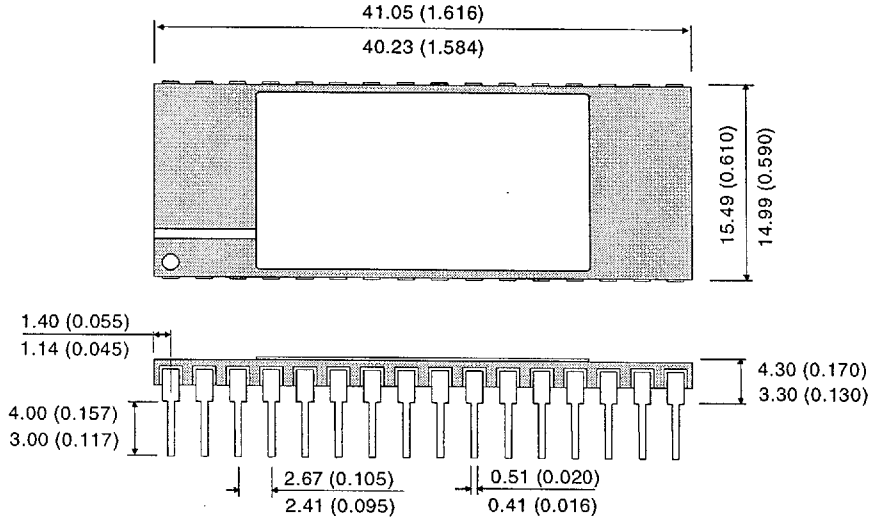


PACKAGE DETAILS

32 pin Extended 'J' Leaded Chip Carrier (JLCC) - 'JX' Package



32 pin 0.6" Dual-in-Line (DIL) - 'S' Package



SCREENING

Military Screening Procedure

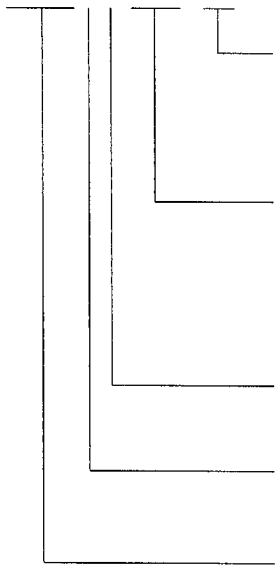
Screening Flow for high reliability product in accordance with MIL-STD-883 method 5004 is shown below.

MB COMPONENT SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM8512JLMB-45



Speed	
25	= 25 ns
35	= 35 ns
45	= 45 ns
55	= 55 ns
Temp. range/screening	
Blank	= Commercial
I	= Industrial
M	= Military
MB	= May be processed in accordance with MIL-STD-883
Power Consumption	
Blank	= Standard Power
L	= Low Power
Package	
J	= 32 pin JLCC
S	= 32 pin DIL
Memory Type	
8512	= 512K x 8 SRAM