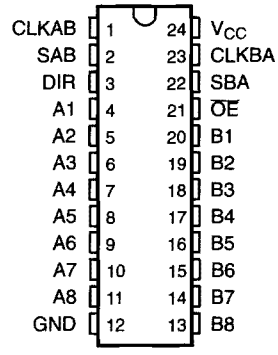
- **Space-Saving Package Option: Shrink Small-Outline Package (DB) Features EIAJ 0.65-mm Lead Pitch**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74LVC646 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVC646 is characterized for operation from −40°C to 85°C.

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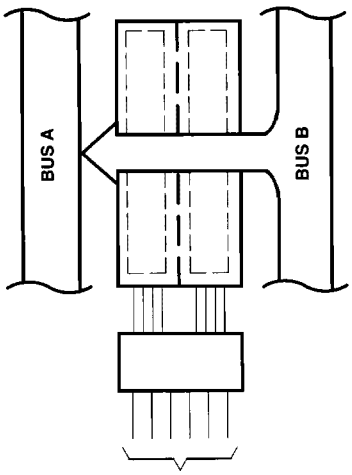
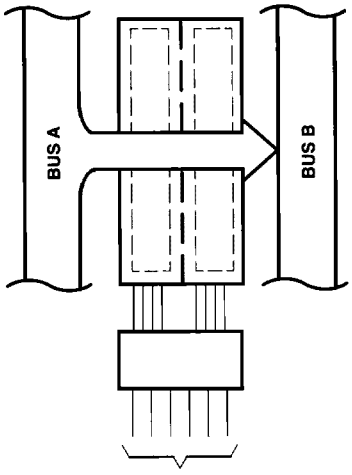
EPIC is a trademark of Texas Instruments Incorporated.



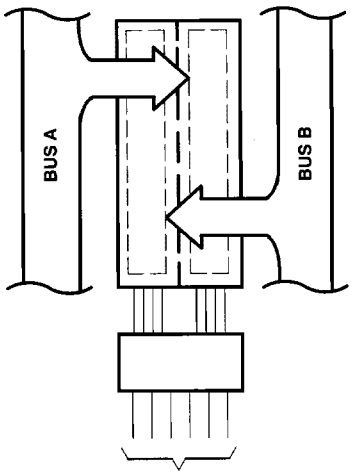
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



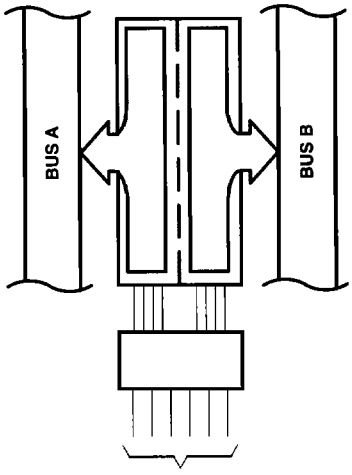
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

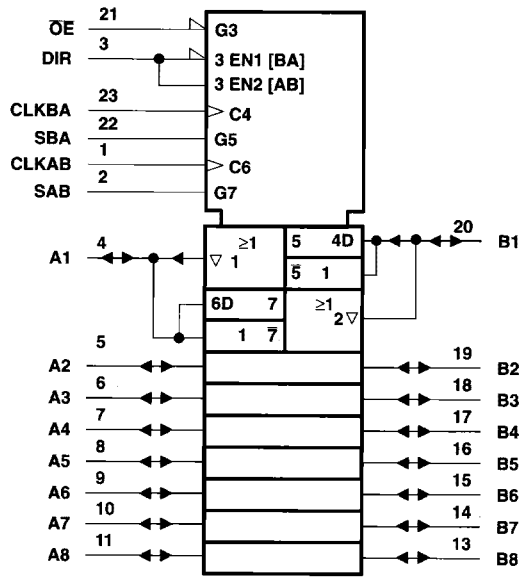
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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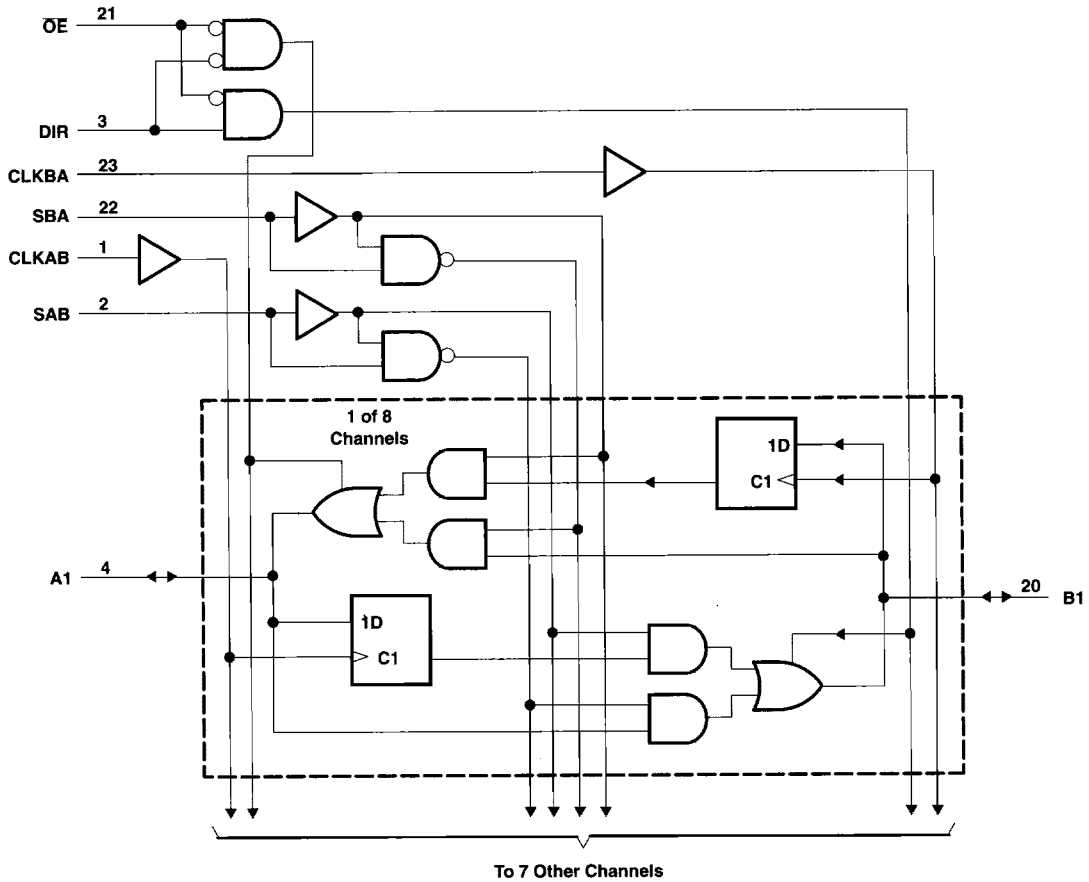
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.5 W
DW package ..... 0.85 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24‡	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24‡	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.
‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	TYP	MAX	UNIT
V_{IK}		I_I = −18 mA	2.7 V			−1.2	V
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2			V
		I_{OH} = −12 mA	2.7 V	2.2			
			3 V	2.4			
		I_{OH} = −24 mA	3 V	2			
V_{OL}		I_{OL} = 100 μA	MIN to MAX			0.2	V
		I_{OL} = 12 mA	2.7 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
I_I		V_I = V_{CC} or GND	3.6 V			±5	μA
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V			20	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				500	μA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		TBD		pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V		TBD		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

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